IMPROVE PERFORMANCE OF LOW POWER AND LOW VOLTAGE DOUBLE TAIL COMPARATOR BY CLOCK GATING

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Abstract:- The requirement of A/D converter that is highly-low power, efficient in area & higher in speed is pushed towards implementing in the dynamic comparators that are regenerative type to enhance the efficiency of power & speed. In the last paper [19], an assessment over delay in the dynamic comparators will be provided & derivations of analytical expressions are performed. From these analytical expressions, designers are able to get an idea regarding major contributors for delay in comparators & perform exploration about tradeoffs completely in design of dynamic comparators. On the basis of provided assessments a latest dynamic comparator is suggested, in which some transformations ar e made to circuitry of traditional double tail comparator for low power & faster operations even when supply voltage is limited. The feedback is strengthened in the regeneration process by not even complicating the structure & invading some more transistors. The outcomes from post simulation help the 0.18-µm CMOS technology to confirm the outcome of the analysis. It is presented from base document that consumption of power & delay are reduced to a great extent in dynamic comparator. In this document we tend to enhance the performance of system by making use of clock gating. As the clock gating is applied, the delay & consumption of power will also get reduced. The suggested system gives the outcome for 1.2V VDD. The length of channel is 130nm. As from the outcomes, it is observed that clock gating helps in minimizing the delay & power in contrast to circuitries presented in previous paper.

Index Terms—*Clock gating, Double-tail comparator, dynamic clocked comparator, high-speed analog-to-digital converters (ADCs), low-power analog design.*

I. INTRODUCTION

In the branch of electronics, comparator is considered to be a device that makes comparisons of two different currents or voltages & gives a digital signal as outcome that indicates which one is having higher value. It is having two analog input terminals V+ & V- and a binary digital outcome Vo. The outcome is expressed as

$$V0 = \begin{cases} 1, if\ V_+ > V_- \\ 0, if\ V_+ < V_- \end{cases} \quad \dots (1)$$

The comparator is comprised of specialized differential amplifier with high gain value. They are generally implanted in the devices that compute & digitize the signals of analog form like ADCs (analog to digital converters) and relaxation oscillators.

A. Differential Voltage

The differential voltages must remain in the specified limits made by the designer. The earlier integrated comparators such as LM111 & some comparators with higher speed such as LM119 need the differential voltage to range below than power supply voltage (±15 V vs. 36 V) [1] Rail-to-rail comparators permits any of the differential voltages in the range of power supply. As they are powered from bipolar supply,

$$V_{S-} \le V_+ , V_- \le V_{S+} \quad \dots (2)$$

or, when through a uni-polar TTL/CMOS power supply:

$$0 \le V_+ , V_- \le V_{cc} \quad \dots (3)$$

Particular rialto-rail comparators having p-n-p input transistors, such as LM139 family permits input potential tp drop the voltage to 0.3 V below the negative supply rail input don't permits it to go on the side of positive rail [2]. Particular ultra-fast comparators such LMH7322 leads to swinging of the input signal below the negative rail & also above positive rail though this is by a very small margin of 0.2V only [3]. Differential input voltage (voltage incur in the two inpus) of a latest rail-to-rail comparator is confined by full swing supply of power.

B. Op - Amp Voltage Comparator

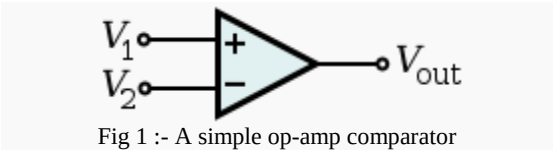

Fig 1 :- A simple op-amp comparator

An op-amp (operational amplifier) possesses a balanced difference input & higher gain. It follows the attributes of comparators and this can be incorporated in the applications which are having requirements of low performance [4].

Theoretically, a general op-amp that works in an open-loop design (without any negative feedback) can be applied like low-performance comparator. As non-inverting input (V+) works at higher levels of voltage than inverting input (V-), high level gain of op-amp leads to saturation of outcome over maximum positive voltage that can be taken as output. As the value of V+ falls down than the V-, saturation of outcome takes place over maximum negative value. The output voltage of op-amp is confined by the supply voltage. An op-amp that works in linear mode having negative feedback, making use of a balanced, split-voltage power supply, (that is supported by ± VS) has the transfer function described as: $V_{out} = A_0 (V_1 - V_2)$. Though, this equation may not be applied over a comparator that is non-linear type & functions over open-loop (with no negative feedback).

As per application, there are various disadvantages of applying operational amplifiers like a comparator in contrast to a dedicated comparator [5].

- The designing of Op-amps is done in a way to make them work under linear mode & negative feedback. Thus, the time of recovery in op-amp is more from the point of saturation. Generally, most of the op-amps are having integrated compensation capacitor press the disadvantages related to

slew rate for the signals having higher levels of frequency. Additionally, op-amp produces a sloppy comparator having delays in propagation for period of around tens of microseconds.

- As op-amps are not having an integrated hysteresis, there is an absolute need for external hysteresis network for input signals with slow speed.
- The quiescent specification for current is considered to be valid when the feedback is in active state. Few op-amps present higher levels of quiescent current when the value of inputs is not equal.
- The comparators are designed for purpose of producing limited outcome voltages that are able to interface with digitized logics very easily. It is mandatory to verify the digital logic when op-amp is used like a comparator.
- Some of the op-amps having multiple regions may present extreme levels of channel-to-channel integration when applied as comparator.
- Various op-amps are incorporated with back-to-back diodes in their inputs. It is fine as the op-amps generally follow one another. But the inputs of comparator are not similar. Such diodes can lead to unexpected form of currents by the inputs.

C. Working

The working of a committed voltage comparator will be fast than a basic operational amplifier which is put in function like a comparator. The committed voltage comparator may comprise of various auxiliary attributes like integrated voltage reference, accuracy, adjustable hysteresis & input which is clock gated.

A devoted chip of voltage comparator is generated in a way so that it can fit along with the interface of digital logic (like a CMOS or TTL). The outcome generated is a binary state that is applied for interfacing with the signals of practical world do a digitized circuitry (such as A/D converter). If the source of voltage is definite, such as DC adjustable components in the path of signal, a comparator is equivalence to the amplifier's cascade. When the value of voltages is almost same the voltage of outcome will not come into one of the logic levels. Hence, the analog signals will all under the digitized domain having unpredictable outcomes. In order o make this range minimal, the value of gain in cascade of amplifiers is kept high. This circuitry is comprised of transistors of bipolar type. On the higher frequencies, input impedance for stages is kept on low level. By this, it minimizes the saturation of bigger & slow P-N junction bipolar transistors that may lead ti longer recovery periods. The smaller sized Schottky diodes are applied like as in binary logic structures, enhance the performance though they still are behind the circuitries consisting amplifiers & using analog signals. There is no terms like slew rate in suck kind of circuitries. The applications like in flash ADCs, distributed signals across the eight ports gets equalized to voltage & current gain as every amplifier & resistors act like level-shifters.

The LM339 accomplishes this with an open collector output. When the inverting input is at a higher voltage than the non inverting input, the output of the comparator connects to the negative power supply. When the non inverting input is higher than the inverting input, the output is 'floating' (has a very high impedance to ground). The gain of op amp as comparator is given by this equation V(out)=V(in).

D. Conventional Dynamic Comparator

The architecture of conventional dynamic comparator that is implemented in the A/D converters on a vast scale, along the rail-to-rail output swing, higher impedance & no such consumption of static power is resented in figure 2.[1], [17]. The working of comparator is described below. In the reset phase, as CLK = 0) & Mtail is deactivated, both of the nodes Ounp & Outn are pulled down to VDD by the reset transistors (M7, M8). This will provide a condition to start & gaining a genuine logic in the reset phase. In the phase of comparison, as CLK = VDD, transistors M7 & M8 are deactivated while Mtail is activated (on).

Output voltages (which are termed as Outp, Outn) that are pre-charged to VDD, begin to discharge over different rates as per the relative input voltage (INN/INP). A case in which VINN<VINP, rate of discharging for Ontp is more than Outn (getting discharged through M2 drain current), comes to VDD-|Vthp| prior to Outn (which is discharged through transistor M1 drain current), the relative (M5) PMOS transistor will triggered the process of regeneration of latch occurred because of back-to-back inverters (M3,M5) & (M4,M6). Hence, Outn equates VDD while Outp gets discharged to ground. if the VINN>VINP, the function of circuitry will be in vice-versa manner. As per the figure 2, delay in a comparator is consisting of two time delays that are termed as tlatch & t0.

The delay (t0) signifies the capacitive discharging of load capacitance CL till the initial p-channel transistor (M5/M6) gets activated. In a scenario, where value of INP node is higher than INN i.e. VINN < VINP, the Outp node has a fast rate of discharging because of drain current incurred in transistor M2 (I2) in contrast to Outn node, which is driven through M1 with small amount of current.

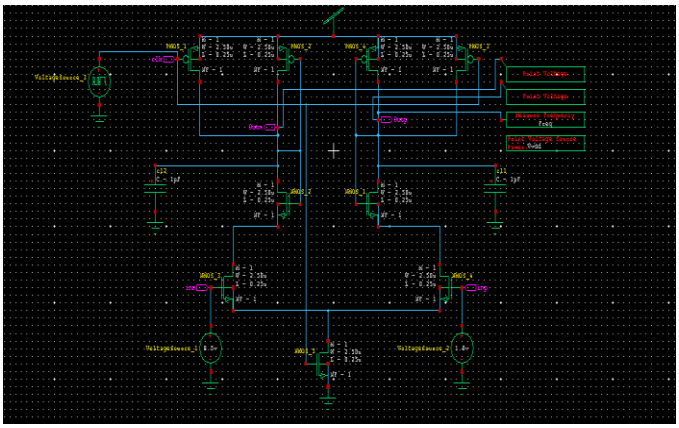

Fig 2 :- Conventional Dynamic Comparator

As per consideration, this design possess several advantages for higher input impedance, so such consumption of static power, rail-to-rail output swing & high level of robustness confronting mismatching & noise [1]. Because of the statement that the speed of switching of nodes giving outcome has no effect of parasitic capacitances, there is a possibility of designing bigger sized input transistor for minimizing the offset. On the contrary part, the disadvantage is that because of various stacked transistors, sufficient supply of voltage is required for genuine delay in time.

The reason is that, at the beginning of the decision, only transistors M3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5 or M6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors M3 and M4, where the gate source voltage of M5

and M6 is also small; thus, the delay time of the latch becomes large due to lower trans conductance.

Another important drawback of this structure is that there is only one current path, via tail transistor Mtail, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better Gm/I ratio, a large tail current would be desirable to enable fast regeneration in the latch [10]. Besides, as far as Mtail operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration.

E. Conventional Double-Tail Dynamic Comparator

A traditional double-tail comparator is presented in Figure 3[10]. There is low stacking in this topology and because of this it is able to work over low voltage supply in contrast to traditional dynamic comparator. It also enables both of the huge current in state of latching & wide Mtail2 fast latching that is not dependent over input common-mode voltage (Vcm) and small amount of current in input state (small Mtrail1) for less offset [10].

The functioning of the comparator is described in the below text. In the reset phase (CLK = 0, Mtail1 & Mtail2 are deactivated), the fp & fn nodes get pre-charged to VDD by transistors M3-M4, that leads to discharging the nodes of output to ground though MR1 & MR2 transistors. N the phase of decision making (CLK = VDD, Mtil1 & Mtail2 are activated), M3-M4 are deactivated & there is a drop in the voltages of nodes fp & fn that is defined by IMtail1/Cfn(p). Above this, a differential voltage that is dependent over input Vfn(p) will start building up. The Vfn(p) is passed to cross coupled inverters by the intermediate stage that is generated by MR1 & MR2. It provides a fine shield in the outcome & input that leads to reduction in the value of kickback noise [10].

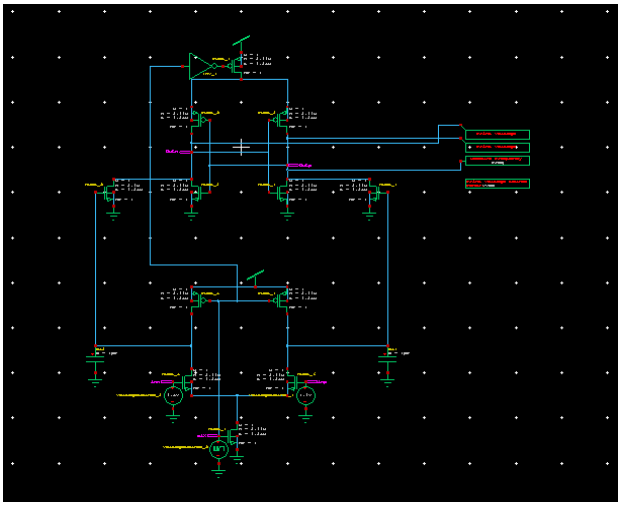

Fig 3 :- Conventional Double-Tail Dynamic Comparator

As per the traditional dynamic comparator, delay occurring in this comparator comprises of two major portions, t0 & tlatch. The delay of t0 presents the capacitive charging going in load capacitance Clout (over latch stage output nodes, Outp & Outn) till the time initial n-channel transistor (M9/M10) is activated. After this, regeneration of latch is initiated. Hence, value is t0 is attained from where IB1 is termed as drain current of M9 (presuming that VINN < VINP) and it is around 50% of tail current (Itail2). As the first n-channel transistor of latch is activated (taking it to be M9), discharging of the relative outcome (Outn) takes place that leads front p-channel transistor (e.g. M8) to get activated, while charging other output (Outp) to voltage supplied (VDD).

F. Double-Tail Dynamic Comparator

The suggested comparator is designed on the basis of double-tail structure by keeping the efficiency of double tail architecture in terms of performance & applications based over low-voltage in mind. The goal behind the suggested comparator is to raise Vfn/fp to further increase the speed of regeneration of latch. To achieve this, two control transistors (Mc1 & Mc2) are added to the initial level going parallel to M3/M4 transistors which are cross coupled.

- *Operation of Comparator*

In the reset phase (CLK = 0, Mtail1 & Mtail2 are deactivated, that avoids the condition of static power), M3 & M4 pulls both fn & fp nodes to VDD, Therefore, transistor Mc1 & Mc2 gets cut off. The inter-mediate stage transistors MR1 & MR2 reset the outcome of latch to ground.

In the phase of decision making (CLK = VDD, Mtail1 & Mtail2 are activated), where M3 & M4 are deactivated. Further, in the initial stage of the phase, control transistors remain in deactivated state (till the time fp & fn are near VDD). Hence, the fp & fn start discharging at different rates as per the voltage provided as input. It is presumed that VINN < VINP, so the rate of dropping of fn is more than fp, (as more amount of current is provided to M2 that M1). Till the time fn is under falling state, associated PMOS control transistor (i.e. Mc1 here) gets activated, that pulls the node of fp to VDD where other control transistor (Mc2) remains deactivated so that fn gets completely discharged. Or else, in different wording, not similar to the traditional double till dynamic comparator, where Vfn/fp is a function of input transistors trans conductance & difference of input voltage (9), in the design as the comparator identifies that for instance node, rate of discharging for fn is more, PMOS transistor (Mc1) is activated where it pulls the other fp node to VDD.

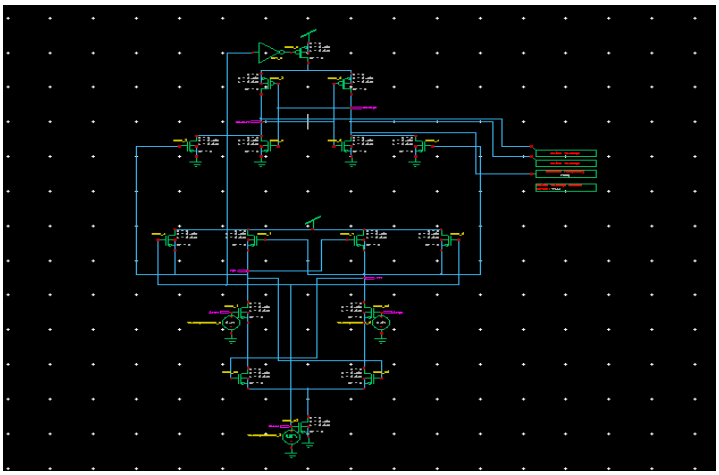

Fig 4 :- Double Tail Comparator

Hence, with the passage of time, there is a rise observed in fn & fp nodes (Vfn/fp) in exponential form that leads to deduction in time of

regeneration of latch. In spite of the impact of suggested technique, one point must be taken into consideration in this circuitry, as one of the control transistors (Mc1) gets activated and current from VDD gets drawn to ground through tail transistor & input (such as Mc1, M1 & Mtail1), that leads to consumption of static power. To deal with this issue two of the NMOS switches are applied as input transistors Msw1 & Msw2.

Initially in the phase of decision making, as per the fact that both of the nodes of fp & fn are pre-charged to VDD (in the period of reset phase), as both of switches are closed, a significant dropping is observed in fp & fn over different rates of discharging. As he comparator identifies the issue of faster discharging of either fn or fp node, control transistors will work out to raise the difference in voltages. It is presumed that fp pulls up to VDD and fn must get discharged completely. Thus, switch applied in the way of fp gets opened (for preventing the current to be drawn out from VDD) but the other switch linked to fn is put to closed state for discharging oh fn node completely. Or else, operation of control transistor comprising the switches imitates the function of latch.

II. PROBLEM STATEMENT

We are working over enhancing the performance of double tail comparator for consumption of power & delay. As per the suggested circuitry in base paper, there consumption of power by the circuitry is very high. We are able to minimize this consumption. Presently dynamic regenerative comparators are being applied because of the requirement of Analog to Digital converts that are efficient in terms of area, ultra-low power & higher speed. In the document, we present an assessment over delay in the dynamic comparators and deriving analytical expressions. From these analytical expressions, designers will be able to get some hint about the causes of delay & identify the tradeoffs completely in structure of dynamic comparator. On the basis of the presented assessments, a latest dynamic comparator is suggested, in which some changes are made to circuitry of traditional double tail comparator for less consumption of power & fast operational speed even when the amount of voltage supplied is less.

III. PROPOSED METHODOLOGY

Clock Gating is termed to be famous technology in various synchronous circuitries for minimizing the dissipation of dynamic power. The technique of clock gating helps in saving the power by incorporating more logical operations to a circuitry for pruning of clock tree. Pruning helps in disabling of some regions of circuitry in order to prevent the switching of states in a flip flop as switching the states leads to consumption of power. In a case they are not switched, the consumption of power in switching tends to be zero where the leakage currents are incurred there.

The function of clock gating is performed by considering the enable conditions that are linked to registers & applying them to gate the clocks. Hence, it is essential that a design structure must comprise of the enable states to gain the best out from clock gating. The process of clock gating provides a presentable die section & the power, as it helps in removal of muxes and gets them replaced by logics of clock gating. The logics of clock gating occur in the format of "ICG (Integrated clock gating) cells. Though, it is to be noted that these logics may create some variations in the design of clock tree as it will be incorporated into the clock tree.

There are a lot of methods for invasion of clock gating logics into the design:

- By coding in the RTL code in the form of enable conditions that are translated to clock gating logic automatically by the synthesis tools (i.e. fine grain clock gating).
- Incorporated into the structure by manual methods by the designers of RTL (generally like module level clock gating) by giving n illustration of ICG cells for gating the clocks of a particular registers or modules.
- Incorporated into RTL by semi-automated means through automatic tools of clock gating. Such tools may invade ICG cells into RTL or enable conditions to RTL code. This also helps in optimizing sequential clock gating.

Any RTL transformations for enhancing the clock gating will led to functional variations to the structure (as the registers will be accumulating distinctive values) that must be re-evaluated.

The process of extraction/ propagation of enable conditions to the sequential components of downstream or upstream in order for clock gating the substantial registers.

Even though, an asynchronous circuitry is said to be not having 'clock' by definition. The terminology of perfect clock gating is applied to present the various ways in which methodologies of clock gating are general probabilistic over the behavior of data dependency that is represented by an asynchronous circuitry. As the granularity over which the clock of a synchronous circuitry attains the value of zero, consumption of power of the circuitry becomes as that of an asynchronous circuitry. It means that circuitry will produce logical transitions when it starts computing in an active manner.

Chip sets like OMAP3, comprising a cell phone heritage assists various types of clock gating. On one side, the clocks are gated manually by using software where a driver works out to disable or enable several clocks that are required by a provided controller in an idle stage. While on the other phase, the clock gating is done on the automated basis, where hardware is made to search for any pending tasks & turn the clock off when there is no need of it. Such types generally communicate with each other & it may be a portion of an enable tree. As an illustration, a bus or integrated bridge may be using an automated gating in order to gate off till a DMA engine or CPY try to use it, where as various peripherals on the bus may be gated off on a permanent basis if they remain unused on the board.

Around more than half (50%) of the dynamic power is consumed by Clock tree. The constituents of power are:

- Amount of power absorbed by combinational logic whose values vary on every edge of clock.
- Power absorbed by FFs.
- The power absorbed by clock buffer tree in the structure.

It seems to be a good suggestion of turning the clock to off state when it has no requirement. The latest tools of EDA assists the automated clock gating. They tend to recognize those circuitries in which it is ea. They tend to recognize those circuitries in which it is eas to incorporate clock gating.

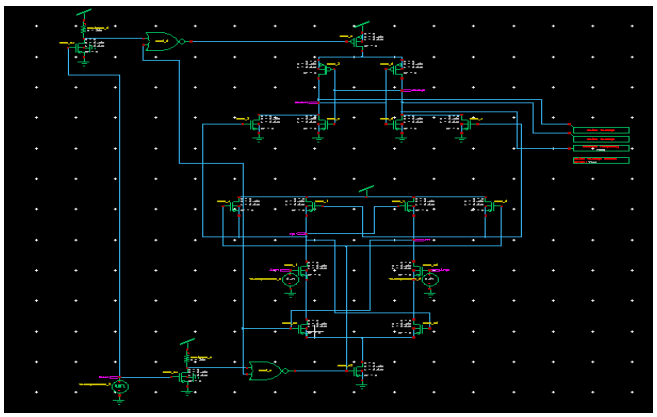

Fig 7 :- Proposed design double tail comparator

The working of RTL clock gating is by recognizing the set of FFs that are sharing a general control signal. Conventional methodologies makes use of the enable term for controlling of the select over a multiplexer that is linked to D port of FF or controlling the clock enable pin over a FF having the abilities of clock enable. This enable signal is applied by RTL clock gating for controlling of clock gated circuitry that is linked to clock ports of each FF having a general enable term. Hence, as a set of the FFs which shares a general enable term will be having an implemented RTL clock gating. The FFs will intake the zero dynamic power till the time enable signal remains in false state.

In the suggested design, clock gating is applied over each phase of clock. The clock gating helps in minimizing the consumption of power from the whole circuitry. As from the outcomes, it is obtained that there is a significant reduction in power along with the delay.

IV. RESULTS

A. Conventional Dynamic Comparator

The conventional dynamic comparator is a structure where two voltages are put in contrast. Input voltage provided is 1.2 V & the outcomes of Vp & Vn voltages are compared. Initially, we assume that Vn < Vp. And Vn = 0.5V & Vp = 1.0 V.

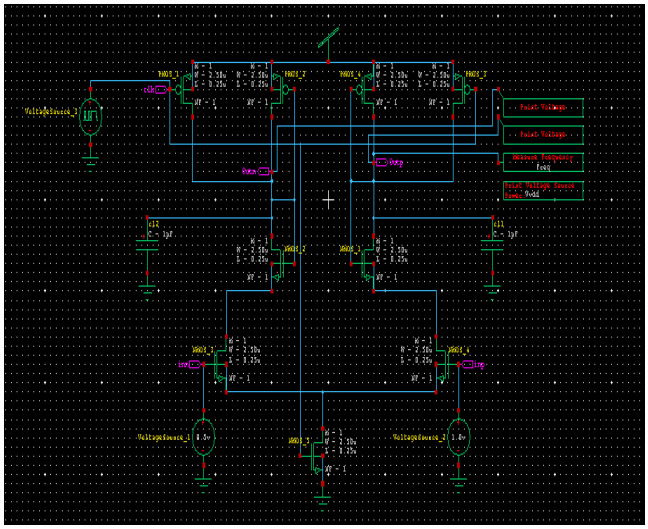

Fig 8 :- Conventional dynamic comparator

Coming from the traditional dynamic comparator waveform, it is observed that rate of discharging in out_p is more than out_n . The consumption of power from dynamic comparator is 6.990047e-009 watts.

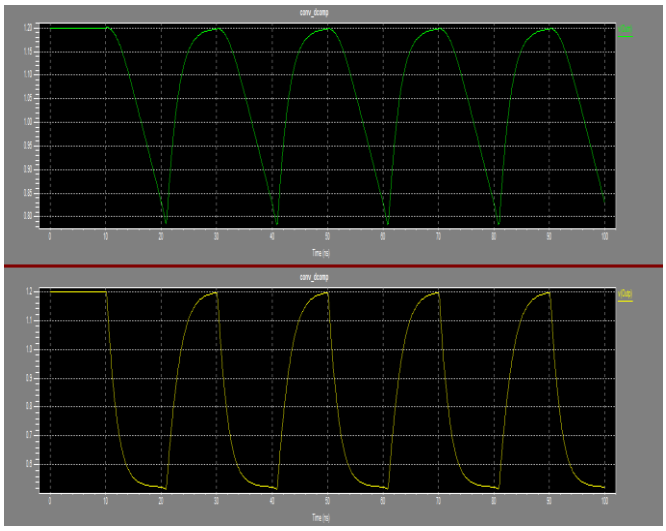

Fig 9:- Waveform for Conventional dynamic comparator

B. Conventional Double-Tail Dynamic Comparator

Clock gating double tail dynamic comparator is referred as a structure which is applied for making comparisons of two different voltages. The input voltage provided is 1.2V & we tend to make comparisons of VP & Vn voltages. Initially the Vp>Vn is obtained. Vn = 0.5V and Vp = 1.0V. In this structure some of the substantial transistors are applied. The absorption of power for traditional Double-Tail dynamic comparator is 8.170468e-008 watts.

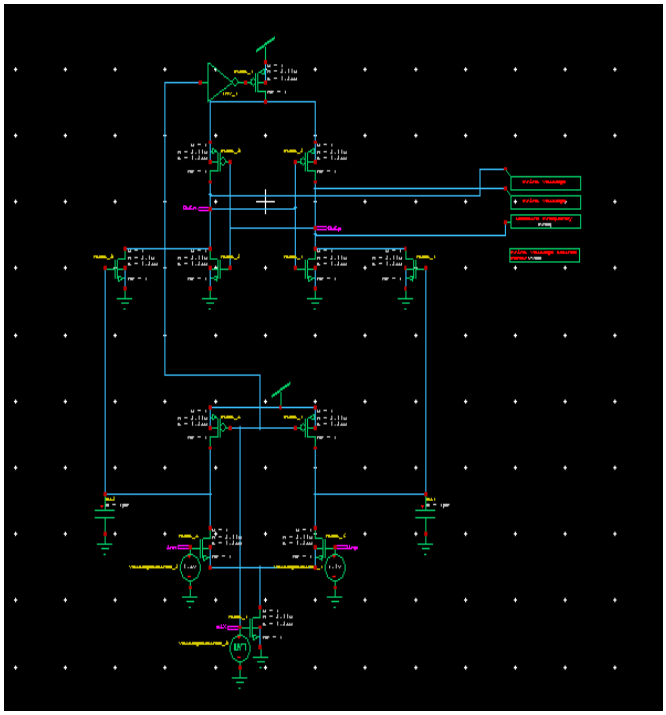

Fig 10 :- Conventional Double-Tail Dynamic Comparator

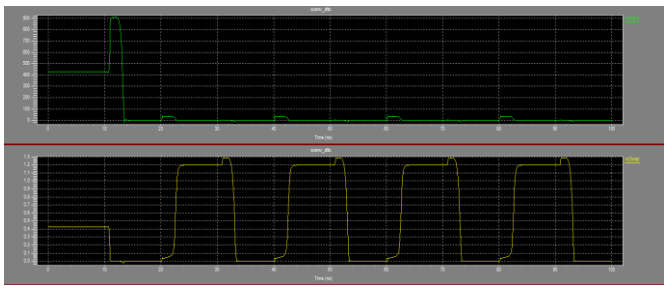

Fig 11:- Waveform for Conventional Double-Tail dynamic comparator

C. Double-Tail Dynamic Comparator

Clock gating double tail dynamic comparator is referred as a structure which is applied for making comparisons of two different voltages. The input voltage provided is 1.2V & we tend to make comparisons of VP & Vn voltages. Initially the Vp>Vn is obtained. Vn = 0.5V and Vp = 1.0V. In this structure some of the substantial transistors are applied. The absorption of power for traditional Double-Tail dynamic comparator is 1.036178e-008 watts.

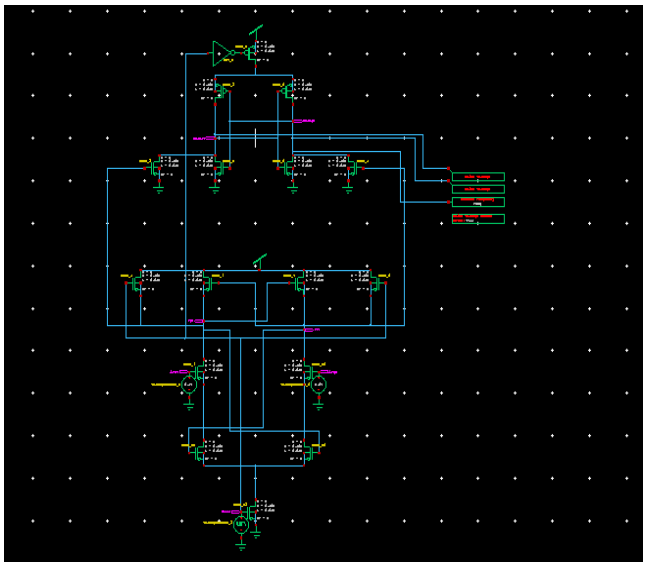

Fig 12 :- Double-Tail Dynamic Comparator

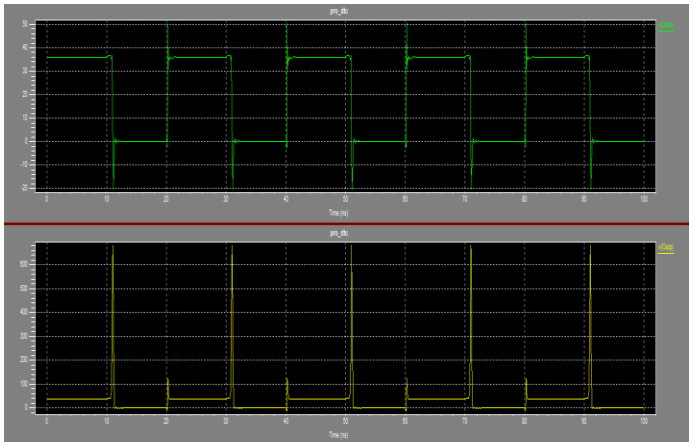

Fig 13 :- Waveform of Double-Tail Dynamic Comparator

D. Proposed Double Tail Comparator

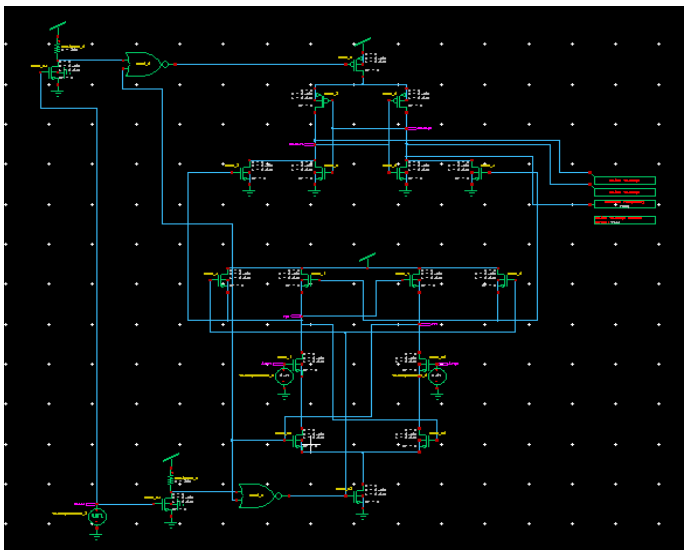

Fig 14 :- Proposed double tail comparator

Clock gating double tail dynamic comparator is referred as a structure which is applied for making comparisons of two different voltages. The input voltage provided is 1.2V & we tend to make comparisons of VP & Vn voltages. Initially the Vp>Vn is obtained. Vn = 0.5V and Vp = 1.0V. in this structure some of the substantial transistors are applied. The absorption of power for traditional Double-Tail dynamic comparator is 6.642184e-010 Watts.

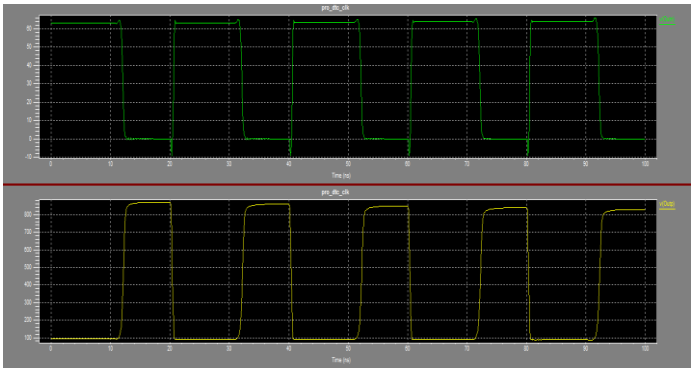

Fig 15 :- Waveform of Proposed double tail comparator

Design & base paper	Power Consumption
Paper [2]	12 e-006 watts
Paper [3]	9 e-006 watts
Conv_dacomp	6.990047e-009 watts
Conv_dtc	8.170468e-008 watts
Pro_dtc(base paper)	1.036178e-008 watts
Proposed method	6.642184e-010 watts

Table 4.1 :- Comparison table

V. CONCLUSION AND FUTURE SCOPE

In this research, a comprehensive delay assessment if provided for the clock gated dynamic comparators & expressions that were generated. Two basic designs of a traditional dynamic comparator & double-tail dynamic comparator were also evaluated. On the basis of theoretical evaluations, another dynamic comparator having minimal voltage & power ability is suggested for enhancing the efficient performance of comparator. The simulations from post-layout leads to 0.13-μm CMOS

technique which assures that there is a significant reduction in the energy per conversion & delay of suggested comparator in contrast to traditional dynamic comparator & double-tail comparator.

Further, we are working over for enhancement of the system by applying GDI & modified GDI methodology, GDI has the ability for minimizing the absorption of power in the circuitry. GDI can be implemented in clock gated circuitries for minimizing the power.

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