LOW POWER SHIFT REGISTER USING NAND GATE WITH 130NM CMOS DESIGN

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Abstract :- **Shift registers are some sort of sequential logic circuitries that are majorly deployed to store data in digital format. In the previous paper , the implementation of a Four bit Serial Input Serial Output (SISO) Shift Register using combination of Activity-Driven Optimized Clock-gating (ADOC) scheme and Run Time Power Gating (RTPG). They had proposed Activity-Driven Fine-Grained CG and RTPG integration. First, they introduce an Activity-Driven Optimized Clock-Gating scheme to improve traditional XOR-based CG. It chooses only a subset of Flip-Flops to be gated selectively, then they introduce RTPG which is applied to each and every Flip Flop. The clock enable signal generated by ADOC scheme is used as the sleep signal to all the PG cells. In this paper , we enhance the performance of circuit by designing the XOR gate from support of NAND gate. NAND gate absorbs less power. We proposed a fine-grained CG and RTPG based 4 bit SISO by apply improved XOR gate with NAND logic gate .**

Keywords— Power Gating; Clock Gating; Activity-Driven Optimized Clock-gating; Run Time Power Gating; Serial Input Serial Output Shift Register.

I. INTRODUCTION

In the circuitries formed in a digital form, a cataract of the flip flops is termed as shift register where the outcome of a FF is considered as input for the succeeding FFs of the link where all of them shares a single cock. It presents a circuitry in which bit array is shifted by one state, also shifting the information of an input & the extreme bit of array on every transistor of clock's input. Eventually, the shift register can be multidimensional so that the stage outcomes & data in are the bit arrays in it: which is basically executed by the implementation of various shift registers in parallel having the same length of bits.

The shift registers may be comprised of the serial & parallel inputs & outcomes. Such are generally termed as SIPO (serial in & parallel out) or PISO (parallel in & serial out). There are some other forms as well that are comprised of both parallel & serial inputs & outcomes. Some registers are bidirectional as well like R ✳ L or L✳ R. The extreme outcome & serial input can be tied together to form a circular shift register.

Shift registers are some sort of sequential logic circuitries that are majorly deployed to store data in digital format. Those are categorized as a set of flip flops in a link so the outcome produced by a flip flop will act as input for the succeeding one. There is no functional integral sequence in states lies in many of the registers. A lot of the registers possess no characteristic internal sequence of states. Single clocks drive all the FFs & they are put in state of reset & set respectively.

In some of the theories, a research is carried on standard form of shift registers like SISO (serial in; serial out), SIPO (serial in; parallel out), PISO (parallel in; serial out), PIPO (parallel in; parallel out) & bidirectional shift registers. A distinctive type of counter i.e. shift register is objectified.

A. Register

- Group of n number of FFs.
- Every FF accumulates a single bit
- Performs two main functions: movement & storage of data.

B. Shift Register

- This register permits the FF to shift the accumulated data to succeeding flip flops.
- The figure presets a regular transfer if information in shift register.

C. Counter

This register undergoes the defined series of states.

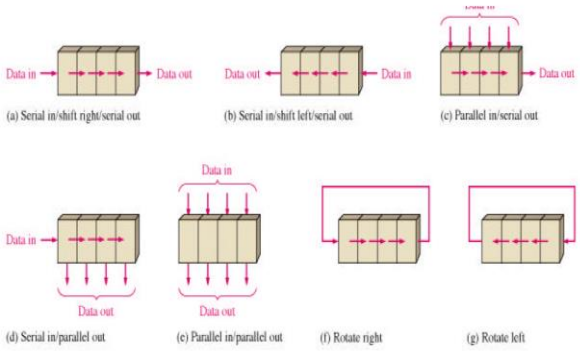

Fig 1:- General movement of data in shift registers

D. Serial In And Serial Out(SISO)

These are considered as most basic form of shift registers. On the Data in, data string is provided & it is shifted by one step on the right side when Data Advance is raised. On every advance, bit on the extreme left side of Data In gets transferred to outcomes of initial outcomes.

Therefore bit present on extreme right as Data Out gets transferred & is lost.

The information is accumulated after every FF on output Q & there are four slots available in this architecture. This is why it is termed as 4 bit register. The pattern of shifting can e demonstrated as by an illustration, with a supposition that register accumulates 0000 which means all the slots for storage are free. By the Data In, 1, 0,1,1,0,0,0,0 are presented in this order along a pulse that is termed as Data Advance for every instance & this is termed as storing or clocking. This is considered as outcome of register. The output pin of extreme left FF is relative to the column on the left hand side & it goes on.

Thus the outcome attainted in serial manner is 10110000.

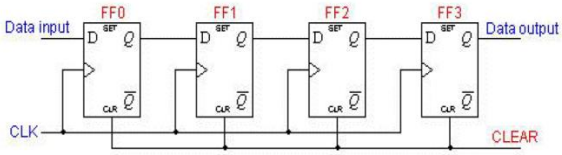

Figure 2:- Serial In & Serial Out

E. Serial In Parallel Out (SIPO)

This structure is helpful in transformation of data from serial to parallel type. In this, data is invaded in a serial manner as mentioned in the section of SISO. The data can either be shifted or read off once it has been clocked.

In such registers, bits are invaded in serial manner as explained in the previous section. The main difference occurs on extraction of bits from register. As the data gets accumulated in it, every bit is presented on the regarded lines of outputs & so whole of the bits are made available respectively. The diagram presents the architecture of 4-bit SIPO register:

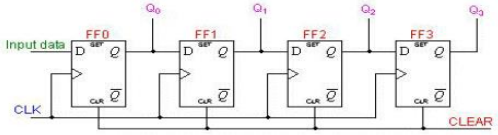

Fig 3:- Serial in & Parallel Out

The table presents the shifting pattern of the 1001 i.e. a 4-bit binary number which is transferred to Q output of register.

Clear	FF0	FF1	FF2	FF3
1001	0	0	0	0
	1	0	0	0
	0	1	0	0
	0	0	1	0
	1	0	0	1

Table 1:- Transfer of bit in SIPO

F. Parallel In Serial Out (PISO)

In this architecture, data input on the lines D1-D4 are of parallel type & D1 is carried to MSB. For writing the data onto register, write or shift CL should be kept as LOW. For shifting the data, W/S CL is raised to high & clocking of register is performed. This system works like SISO shift register & D1 is considered as Data Input. While, the Data Output will be stated as Q till the time cock cycles don't exceed the length of data string & the order will be parallel data read off.

A 4-bit PISO shift register is presented beneath. This circuitry makes use of D- FFs & NAND gates to invade the data into register.

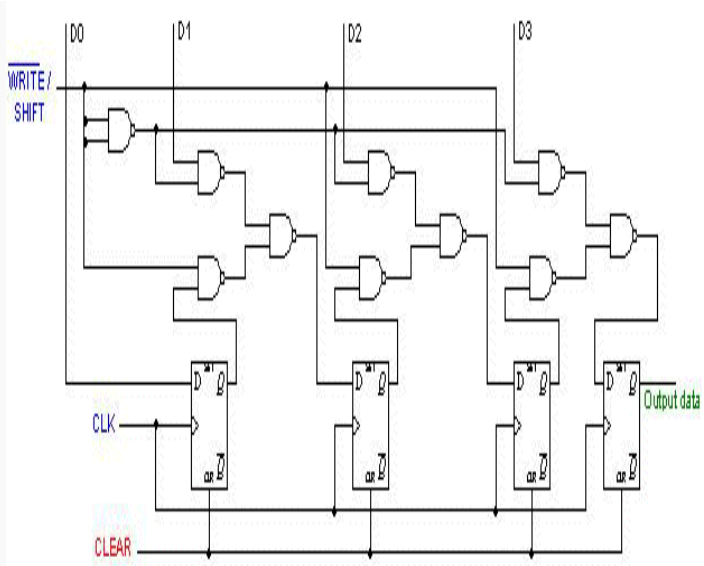

Fig 4:- 4-Bit PISO Shift Register

Here D0, D1 & D3 are considered as parallel inputs & here D0 bit is most significant while D3 bit is the least significant. Mode CL is considered as LOW for writing the data & also data is clocked in. This data might be transferred when mode CL & shift is kept HIGH.
The register performs right shift operation on the application of a clock pulse, as shown in the table below. The diagram presents write & shift sequence while considering internal stage of register. The main implementation of register is the transformation of information from serial to parallel interface & vice versa. It is more advantages for the circuitries in which the registers are grouped in parallel while the formulation of a serial interface is more convenient. The shift registers can be implied as basic delay circuitries. There are a lot of bidirectional shift registers that are also hooked up in parallel for the purpose of implementation of hardware in a stack.

II. PREVIOUS WORK

A. Structure And Design Of Shift Register Using Integration Of ADOC & RTPG

The flip flop D keep a check on input, do the transmissions with those which are equivalent to D input. The FF accumulates the value present on the data line. It can be termed as a simple cell of memory. The diagram presents the internal schema of D flip flop by making use of NAND gates [3].

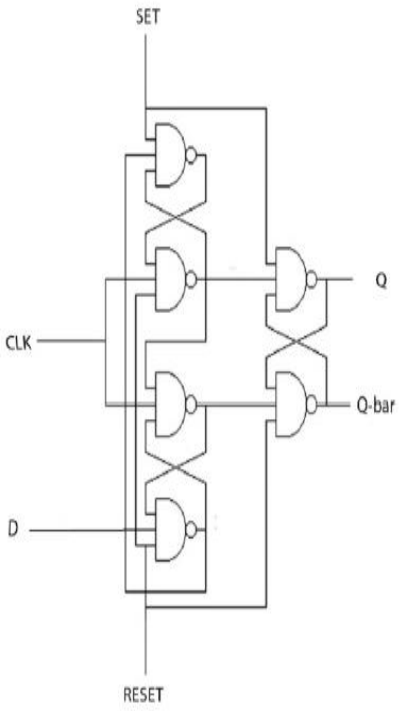

Fig. 5 :- Schematic of D Flip-Flop using NAND Gate

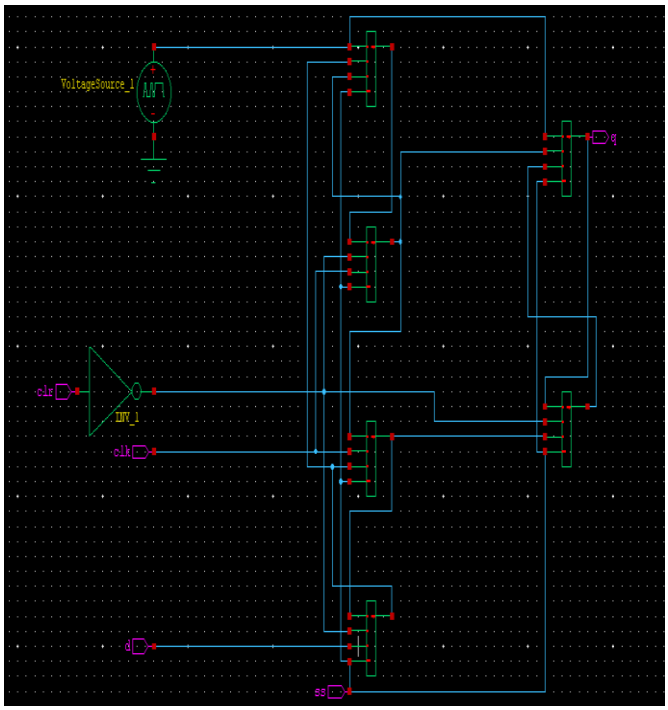

Fig 6 :- Schematic of D Flip-Flop using NAND Gate tanner design

The provided diagram presents several internal constituents of CMOS NAND gate that is implemented in a D flip flop.

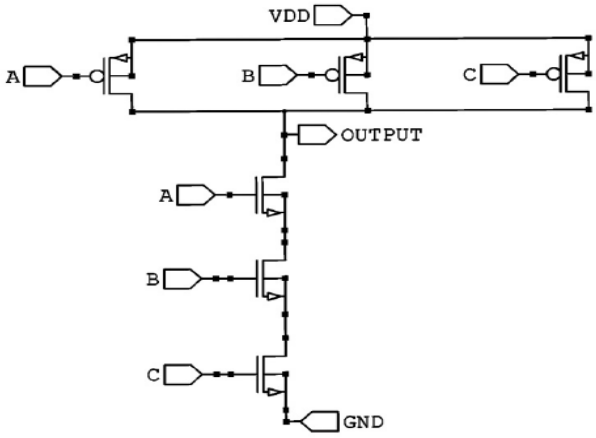

Fig. 7 :- CMOS NAND Schematic

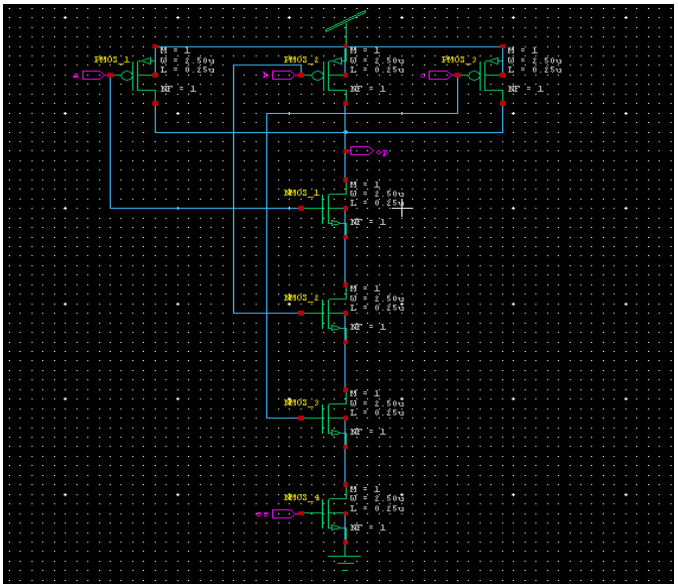

Fig 8 :- CMOS NAND gate design by tanner tool

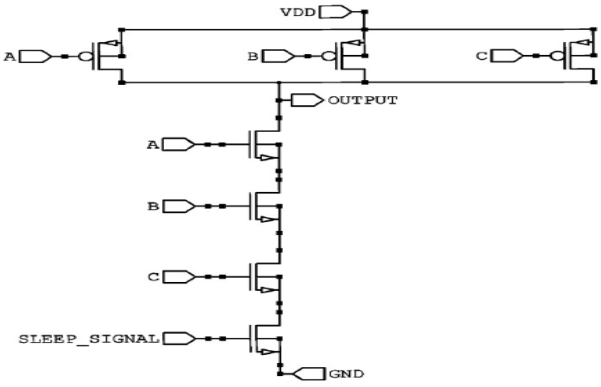

Fig. 9 :- CMOS NAND Schematic with Single footer PG scheme

B. 4 Bit Serial Input Serial Output Shift Register

The shift register is considered as cataract of FFs that share a single clock & the outcome of every FF becomes the input for the succeeding FFs in a chain. And it gets transferred by one position in the array of bits by shifting the data located on the input side & shifting the last bit in array on every transition takes place of clock input

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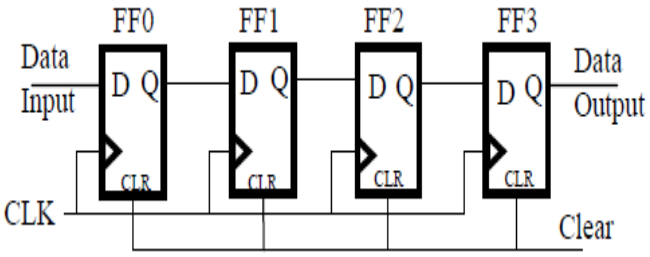

Fig. 10 :- Four bit SISO Shift Register

Basically, CG is implemented to all the FFs which are SCG circuitry. The absorption of power is also evaluated in SISO shift register, SCG circuitry of shift register without any PG schema & SCG circuitry of shift register with single or double footer PG schema. The signals of clock enable are produced & termed as sleep signals to whole of PG cells.

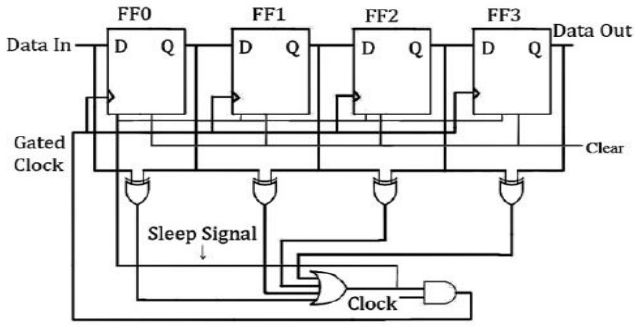

Fig. 11 :- Four bit SISO Shift Register with SCG & RTPG

The suggested PSCG circuitry is implemented for minimization of power in dynamic fashion. Basically, a single FF is selected & CG is implemented & RTPG is involved later on. This similar process takes place again by selecting the two FFs accompanied by three FFs. Both of the PG schemas were implemented to the described circuitries.

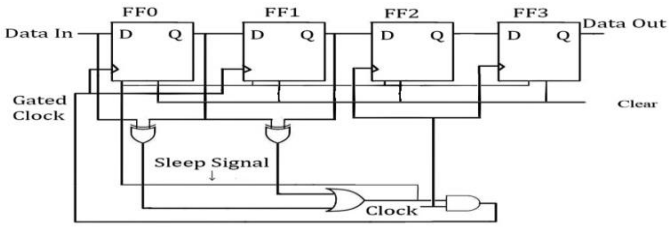

Fig. 12 :- Four bit SISO Shift Register with ADOC & RTPG applied to only two FFs

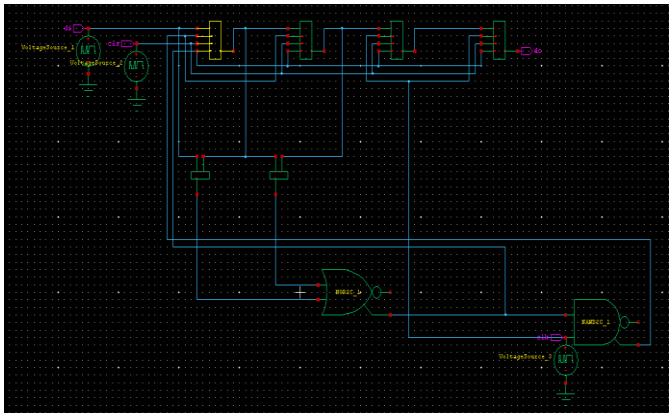

Fig. 13:- Four bit SISO Shift Register tanner design

III. PROBLEM STATEMENT

The execution of 4-bit SISO shift register along the amalgamation of ADOC schema & RTPG is suggested. They also suggested integration of RTPG & activity driven fine grained CG. Initially, an activity driven optimized clock gating schema is presented for improvisation in the conventional CG that are based on XOR. It selects a subset of FFs that are gated accordingly. Then RTP is implemented to every single FF. The signal of clock enable that is formulated by ADOC schema is implemented as sleep signal to all the cells of PG. They work at a basic gate of XOR that absorbs high power. it is also presented from the diagram the a basic gate of XOR is applied in the circuitry of SISO along the RTPG & ADOC. There is a scope of improvisation in the performance of outcome if the XOR gate is able to reduce its absorption of power.

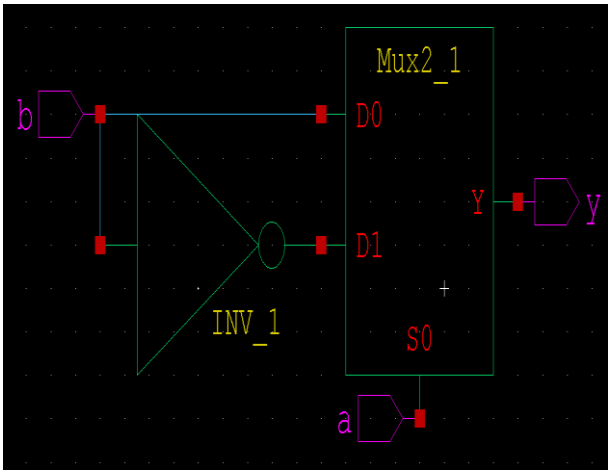

Fig 14:- XOR gate design in TANNER

IV. PROPOSED METHODLOGHY

The throughput circuit can be enhanced by designing the XOR gate by support of NAND gate. NAND gate absorbs much less power. so as per design, the implementation of XOR along the NAND gate is presented.

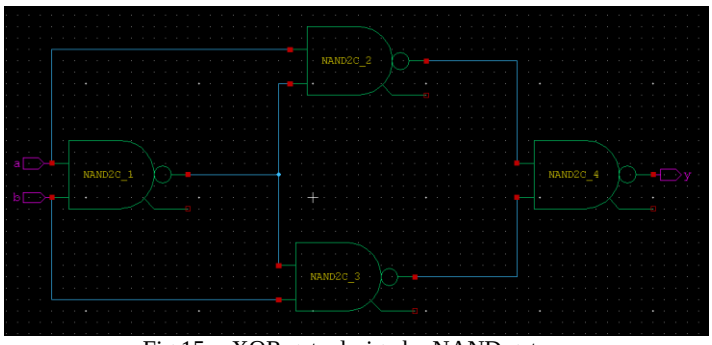

Fig 15 :- XOR gate design by NAND gate

In this design, four NAND gate transistors are applied where a,b are the inputs & outcome is obtained from y. So, the XOR gate makes use of NAND gate. And it will absorb less amount of power.

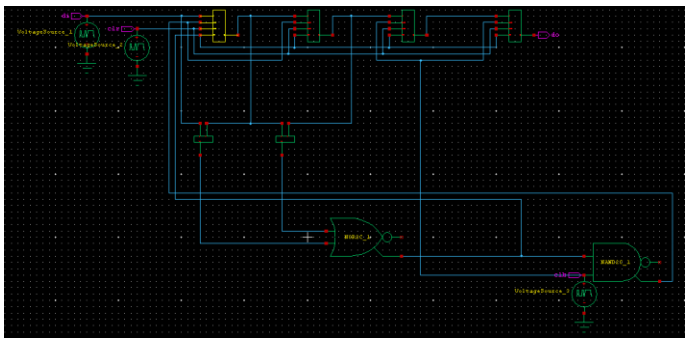

Fig 16:- Proposed SISO with NAND gate based design XOR gate

A new SISO system is designed by the suggested XOR & NAND gates. Here the XOR gate is applied for two numbers of times. In this circuitry, clear & di are inputs of the design of SISO while do is the outcome.

V. RESULTS

In the previous design, the 4-bit SISO is formulated. In such circuitries, a basic XOR gate is provided that absorbs higher amount of power. As per the outcomes, the power is 1.75138e-004 that is obtained from the outcomes of T-Spice. The presented 4-bit SISO design has a delay of 1.72 ns on the output wave form that is presented in the diagram.

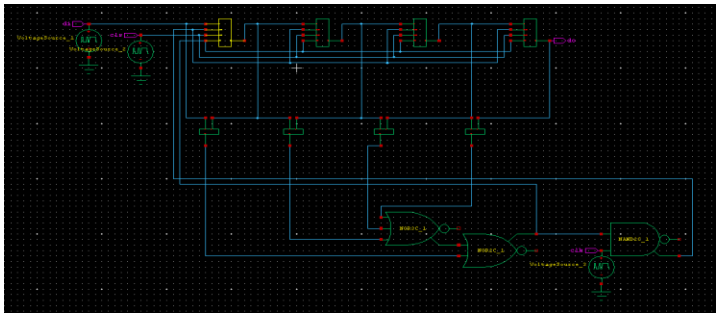

Fig 17 :- 4 bit SISO existing design

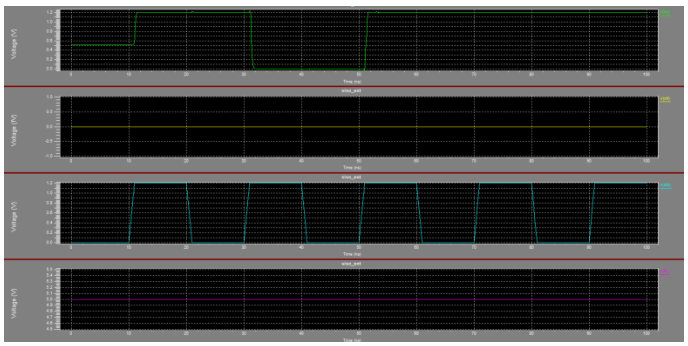

Fig 18 :- Output waveform of the existing SISO circuit

As from the diagram of output waveform, it presents that three types of inputs are there that are clk, di & clr. It is seen that value of input is 5V that says that it is logic 1. On the outcome of do as presented in diagram of waveform, it is observed that output logic 1 takes place after completion of the three cycles.

In the presented design, the 4-bit SISO is formulated. In such circuitries, a basic NAND gate constituted on XOR gate is provided that absorbs less amount of power than the above mentioned design. As per the outcomes, the power is 2.518672e-005 that is obtained from the outcomes of T-Spice. The presented 4-bit SISO design has a delay of 1.20 ns on the output wave form that is presented in the diagram

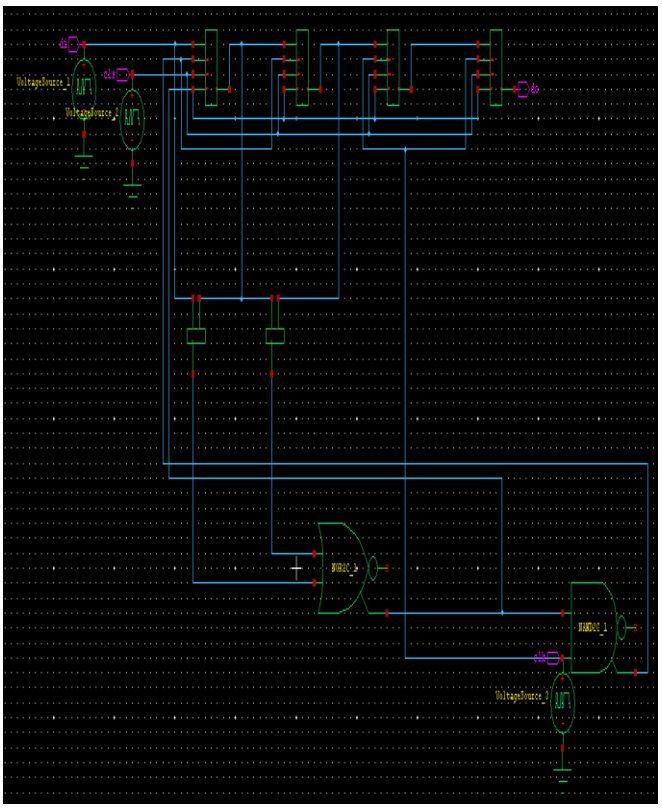

Fig 19 :- Proposed 4 bit SISO design with NAND gate based XOR gate

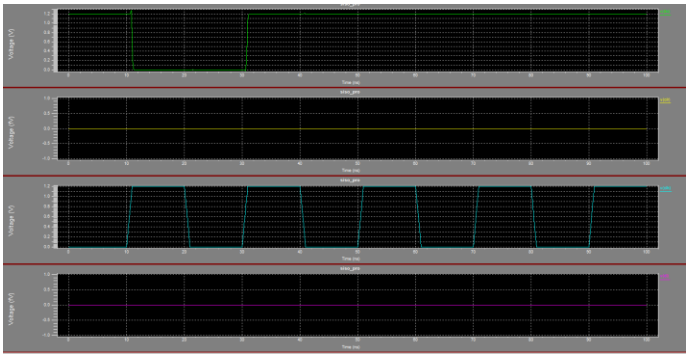

Fig 20 :- Proposed design SISO output waveform

As from the diagram of output waveform, it presents that three types of inputs are there that are clk, di & clr. It is seen that value of input is 5V that says that it is logic 1. On the outcome of do as presented in diagram of waveform, it is observed that output logic 1 takes place.

	Power(W)	Delay
Existing Design	1.752138e-004	1.72 ns
Proposed Design	2.518672e-005	1.20 ns

Table 2 :- Comparison Table

VI. CONCLUSION AND FUTURE SCOPE

Here RTPG & fine grained CG is suggested that is constituted over a 4-bit SISO that is implemented for improvised XOR & NAND logic gates. The fine ADOC methodology is initially applied that choose the subset of FFs to gate. Furthermore, the clock enable signal that is produced in ADOC circuitry can be applied as sleep signal in RTPG. A design of NAND of minimal power is applied for designing of XOR gate. It is observed from the outcomes that the power as outcome is 1.752138e-004 W for a basic XOR gate. For the furtherance, the performance of 4 bit SISO is also enhanced & the NAND gate composed over XOR gate is applied. By the outcomes, it is observed that the suggested methodology can deduce the absorption of power. So the power gained as outcome will be 2.518672e-005W with the suggested technique.

In future, the GDI techniques can be applied for improvisation of outcomes along with the gating of clock. GDI i.e. Gate Diffusion Input is a latest technology emerged for minimal power digitized circuitries. This methodology helps in deduction of delay, absorption of power & area of the circuitry & also minimizes complexity of the design. The throughput of system can be improvised of designed systems by the implementation of gating of clocks. The clock gating is such methodology that can leads to deduction in the absorption of power produced as outcome. So the provided techniques are helpful in deduction of quantity of transistors & absorption of power.

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