ISSN No :- 2456- 2165

Design of Miller Encoder using 32nm UMC CMOS Technology at 5 GHz

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***Abstract*—In this paper, we have designed Miller Encoder circuit with the best optimized design of T-flip flop, using 32nm UMC CMOS technology. Different designs of T-Flip Flop has been designed using different techniques like CMOS inverters, HLFF method, NMOS switches, Transmission Gates & GDI (Gate Diffusion Input). Each circuit structure has been designed utilizing 32nanometre UMC CMOS technology as well as compared at 5GHz clock frequency. These designs are simulated in HSPICE software leading to correct behavior up to 5GHz. Best optimized design of T-flip flop is selected and Miller Encoder is formed with the combination of D-flip flop and T-flip flop. Miller Encoder is being widely used in the complex optical communication systems and frequently employed in Radio Frequency Identification Systems (RFID).The crucial advantage of this design is to utilize a clock signal functioning in the similar frequency domain of applied data. Output changes on the rising and falling edges of the clock.**

Keywords*— *RFID, Miller Encoder, Optical Communication System.

I. INTRODUCTION

In 1963, Armin Miller suggested a scheme for recording and / or reproducing system for digital information having the following US patent No: 3,108,261, is also known as "Miller code" after his name [1]. Previously magnetic medium such as magnetic tapes, drums, etc. were normally employed to store data. Digital information was generally documented on magnetic medium as either of two magnetic flux configurations which consecutively happen at distinct points along its length [2].

Similarly, in 1968 George V. Jacoby suggested a scheme for magnetic recording and reproducing of digital information having the following US patent No: 3,414,894 [2]. The scheme was analogous to what Armin Miller proposed. It was an enhanced form. In some literature it is also known as "Delay Modulation" [3]. It is also known as "Miller code". The data format is represented as follows: transition occurs at mid-bit of the data whenever binary bit "1" occurs, whereas transition occurs at the boundary when consecutive binary bit "0" occurs. In this way usually signals were recorded on a magnetic medium.

Key features are:

- Two levels
- No DC component
- Good synchronization

Doubling-up of bit rate, compared to data rate, leads to higher bandwidth.

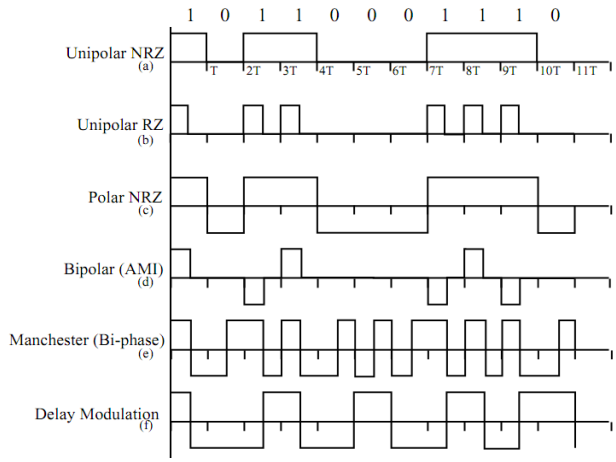

Figure 1.1: Output Waveforms for Various Encoding techniques, including Miller Encoding technique (Delay Modulation)

A. Advantages of Miller Encoding

Advantages of Miller Encoding technique make it very efficient to use in high speed optical communication systems at very high frequencies of the order of GHz. The benefits of Miller Encoding can be envisaged by analyzing the graph as shown in Figure 1.2 [4]. It shows that Miller code is superior to NRZ as the spectral density at ω=0 is slightly low, also superior to bi-phase as Miller code has its power more intense at lower frequency compared to bi-phase. As a consequence, the bandwidth requirement is lesser, permitting a lower recording speed and allowing additional data to be recorded on the same length of recording medium resulting in higher packing density.

B. Applications of Miller Encoder

Application of Miller code was restricted to magnetic recording medium. But with change of time it is now inquired into other fields such as RFID's and also in optical domain respectively. The benefits of the code are being explored in the said applications. In RFID (Radio Frequency Identification) system, [5] in order to decrease error rate and increase efficiency, the data is encoded ahead of modulation and is transmitted between the tag and reader [6].Generally, Manchester and Miller codes can be utilized in telecommunication and are frequently employed in RFID system. Miller code is an automatic regulating cipher since it comprises 'timing' information inside the data, which can be extracted at the receiver side. Hence, Miller code has improved operation against error delay and noise interference.

ISSN No :- 2456- 2165

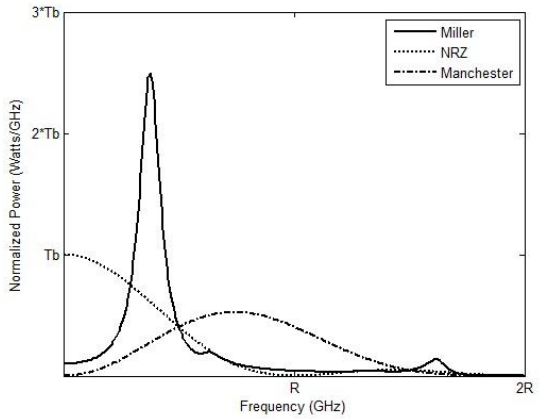

Figure 1.2: One-sided spectral densities of Miller code, NRZ and Manchester waveforms

II. LITERATURE REVIEW

In this section we will discuss about the previous work done on Miller Encoder. Previous work was done by Yu-Cherng Hung, Min-Ming Kuo, Chiou-Kou Tung, and Shao-Hui Shieh in paper "High-Speed CMOS Chip Design for Manchester and Miller Encoder" [6] in 2009.In previous works, used Miller Encoder design is as shown in Figure 2.1:

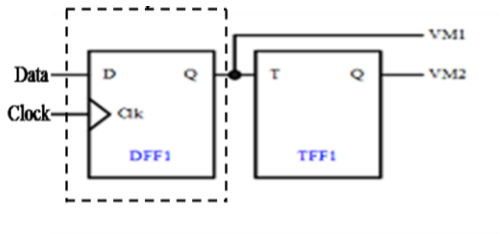

Figure 2.1: Miller Encoder block Diagram

Miller encoder layout constitutes of an edge triggered D-Flip Flop and a T-Flip Flop as shown in Figure 2.1. In this configuration, firstly Data and Clock are applied to D-Flip Flop. Also D-Flip Flop works as a Manchester Encoder. Then this coded signal is passed through a T-Flip Flop to generate the Miller encoded data. The T-Flip Flop has been designed so that it may not require the different clock; given output of D-flip flop is used as a clock.

D-Flip Flop and T-Flip Flop design has been constructed by using CMOS inverters and NMOS digital switches [7] [8] [9]. This design used TSMC CMOS 0.35-µm 2P4M technology, operated at 200 MHz under 3.3V supply voltage and number of transistors used was 94.

III. PROPOSED WORK

In our proposed work, as we have mentioned in section 1, that Miller Encoder constitutes of combination of D-Flip Flop and T-Flip Flop, so we have used D-Flip Flop design using CMOS inverters and NMOS digital switches and for T-Flip Flop design, different circuits of T-Flip Flop using CMOS inverters, NMOS digital switches, HLFF technique, pass transistors and GDI (Gate Diffusion Input) cell [7] [8] [9], have been compared on the basis of parameters like duty cycle, power consumed and time delay. Each circuit structure has been designed using 32nm UMC CMOS technology. All the designs have been simulated in HSPICE and correct results have been obtained at clock frequency 5GHz with supply voltage Vdd= 1V and 25 degree centigrade temperature. Best optimized design of T-flip flop is selected and Miller Encoder is formed with the combination of D-flip flop and T-flip flop.

A. Edge Triggered D-Flip Flop Design

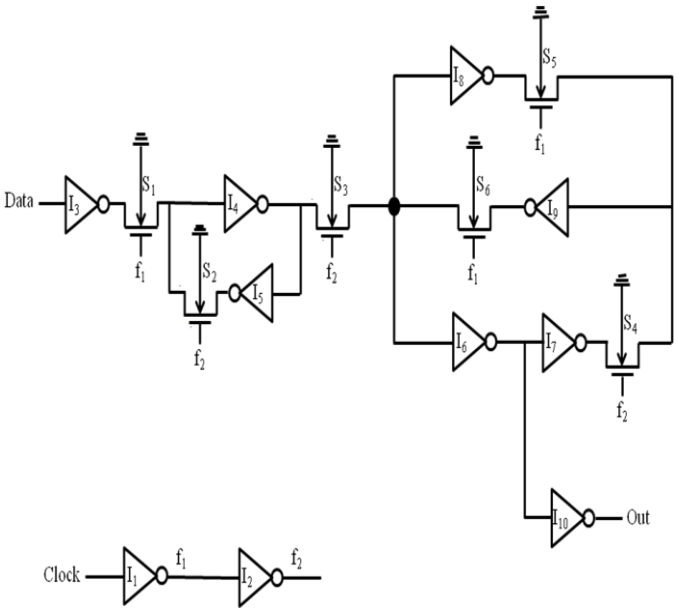

Figure 3.1: Edge Triggered D-Flip Flop Design

This D-Flip Flop design [7] [8] has been constructed by using CMOS inverters and NMOS digital switches. In this circuit an inverting latch (I8, I9) is following a non- inverting latch (I3, I4, I5). When phase f1 occurs, input signal is passed through inverter I4. When phase f2 occurs, inverters I4 and I5 latch the input data along with surpass this into output knob (Output) by means of inverters I6 and I10, at this stage inverter I9 produces the inverse value of Out. When the next f1 phase occurs, inverters I8 and I9 latch the previously inverted output and pass it to the inverters I6 and I10 afterwards into output.

B . T-Flip Flop Design

We have designed T-Flip Flop by using four different techniques [9]:

1. Using CMOS inverters
2. Using NMOS digital switches
3. Using HLFF (Hybrid Latch Flip Flop) technique
4. Using GDI (Gate Diffusion Input) technique

Best optimized design of T-Flip Flop is selected on the basis of various factors like duty cycle, power consumed, propagation delay and used in Miller Encoder design with the D-Flip Flop.

C. T-Flip Flop Design-I (Using CMOS Inverters)

In this design I3, I4 are forming master latch and I5, I6 are forming slave latch. In k2 phase master latch stores the previous output and passes it to output through I5, I6 & I8. In k1 phase slave latch works and passes signal to output. When clock is low (k1 phase) output is same as the previous one. When clock is high (k2 phase) output gets inverted.

ISSN No :- 2456- 2165

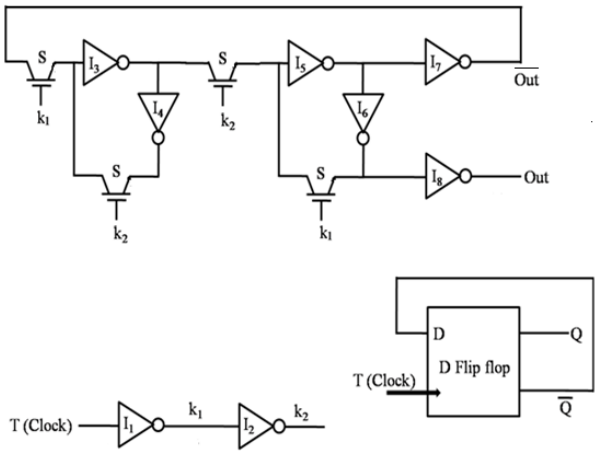

Figure 3.2: T-Flip Flop Design-I

D. T-Flip Flop Design- II (Using NMOS Digital Switches)

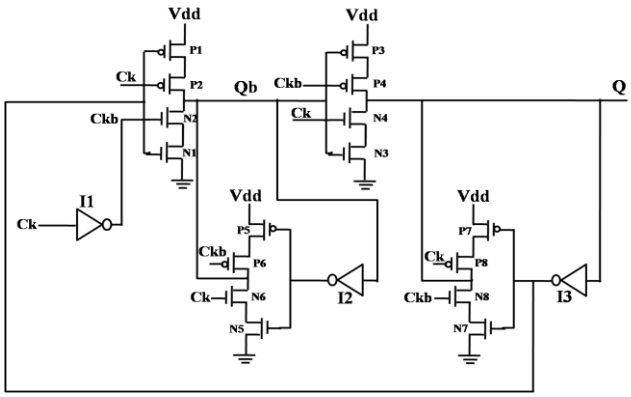

Figure 3.3: T-Flip Flop Design-II

In this circuit, when ck (clock) signal is low, N1 and N2 are on and gives '0' output i.e. Qb = '0'. This value does not pass to Q therefore previous value of Q does not change and we get the same data. When ck (clock) signal is high, P3 and P4 will be on and Vdd passes to the Q therefore we get the inverted output.

E. T-Flip Flop Design-III (HLFF Technique)

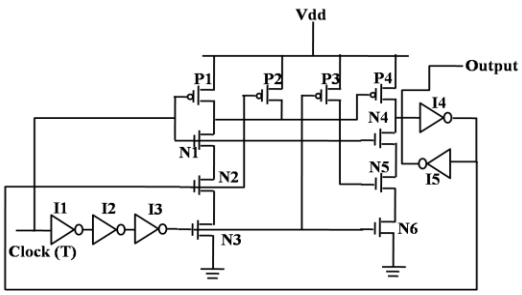

Figure 3.4: T-Flip Flop Design-III

In this circuit when clock (T) signal is low, P1 and N3 gets on, output of I4 switches N2 on, N1,P2,P3,P4 are off. Since N4 and P4 are off therefore output will remain same as the previous one because the cross – coupled inverters at the output are used to maintain the stored value. When clock (T) signal is high, N1, N2, N4, N5 and P4 gets on but P1, P2, P3, N3 and N6 are off therefore we get the inverted output.

F. T-Flip Flop Design-IV (Using GDI Technique)

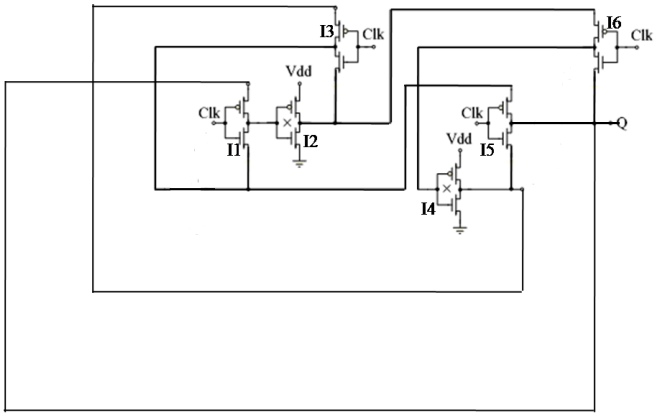

Figure 3.5: T-Flip Flop Design-IV

In this circuit when clock (clk) signal is low, PMOS of all inverters get switched on and gives same output as input. When clock (clk) signal is high, NMOS of all inverters get switched on and gives inverted output.

G. Miller Encoder Design

Miller Encoder is formed by connecting output of D-flip flop to T-flip flop [6]. Comparison between the mentioned 4 different T-Flip Flop designs have been made with the help of HSPICE simulation and on the basis of simulation results, T-Flip Flop Design- III have been selected the best optimized design of T-Flip Flop. Therefore T-Flip Flop Design- III, has been implemented in Miller Encoder. Thus Miller Encoder is designed by using the combination of edge triggered D-Flip Flop Design and , T-Flip Flop Design- III.

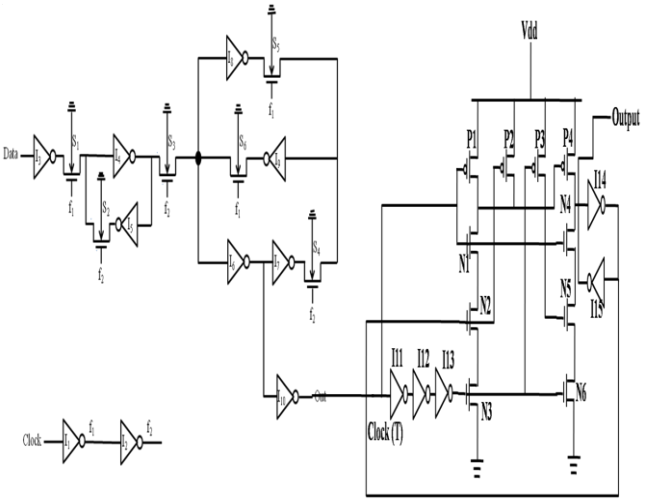

Figure 3.6: Miller Encoder Circuit Diagram

This design is formed by connecting output of D-flip flop to T-Flip flop. Output of D-flip flop is the value produced by inverter I10. T-Flip Flop takes D-flip flop output as a clock and gives Miller encoded signal. Value produced by inverter I15 is the Miller output code.

ISSN No :- 2456- 2165

Working of D-flip flop and T-flip flop has already been discussed in the previous sections.

IV. SIMULATION RESULTS

The Miller Encoder has been designed in a 32 nanometer UMC CMOS technology and the design has been simulated in software HSPICE. Correct behavior and results have been obtained at clock frequency 5 GHz with supply voltage Vdd= 1V and 25 degree centigrade temperature.

Simulation result of output waveform of Miller Encoder has been given in Figure 4.1.

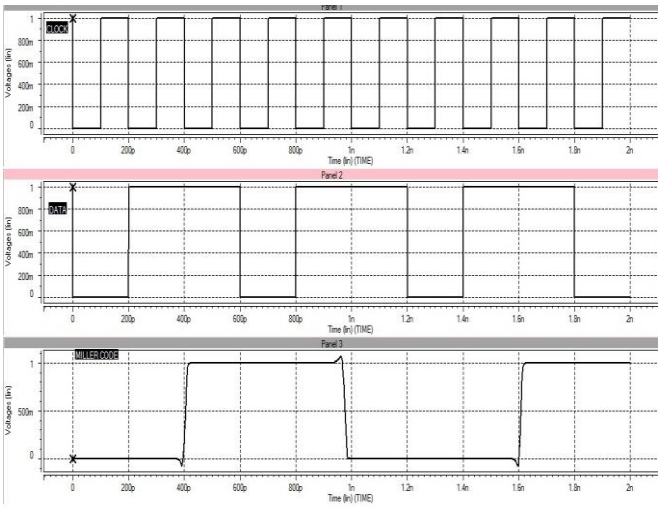

Figure 4.1: Simulated Output Waveform of Miller Encoder at Clock frequency 5 GHz

Simulation result of power consumed by Miller Encoder has been given in Figure 4.2.

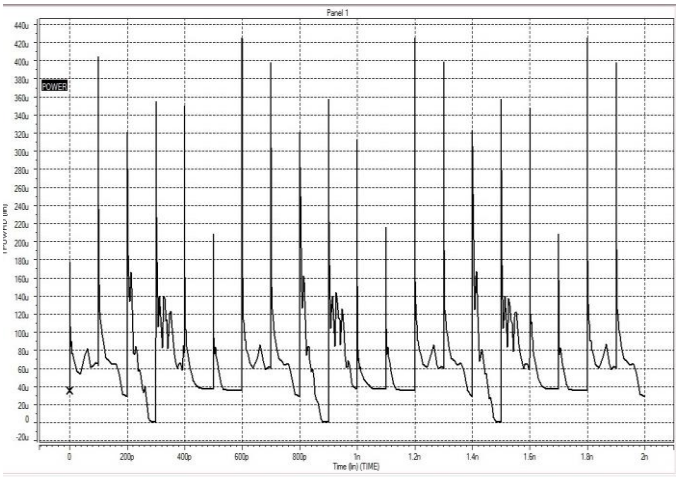

Figure 4.2: Simulated result of power consumed by Miller Encoder

V. RESULTS AND COMPARISON

Comparison between 4 different designs of T-Flip Flop at 32nm working at 5GHz has been given in Table 5.1. T-Flip Flop Design-III (HLFF Technique) is considered to be the best optimized design of T-flip flop at 5GHz with average power = 188.18µW and power delay product (PDP) = 11.546 fJ.

Clock Frequency(5GHz) & L=32nm				
Design No.	**No. of Transistors used**	**Propagation Time (ps)**	**Average Power (µW)**	**PDP (fJ)**
1	26	760.67	304.56	231.66
2	9	1004.5	276.82	27.806
3	10	61.358	188.18	11.546
4	18	233.75	659.06	154.05

Table 5.1: Comparison between different T-flip flop designs

Simulation results of proposed Miller Encoder design is given in Table 5.2.

Frequency (GHz)	**Propagation Time (ps)**	**Average Power (µW)**	**Power Delay Product (fJ)**
5	589.55	65.57	38.656

Table 5.2: Simulation Results of Miller Encoder

Comparison between proposed work and previous work (High-Speed CMOS Chip Design for Manchester and Miller Encoder) [6] is given in Table 5.3:

FUNCTION	**PREVIOUS WORK**	**PROPOSED WORK**
PROCESS TECHNOLOGY	0.35 micro m TSMC CMOS Technology	32 nm UMC CMOS Technology
Number Of Transistors	94	46
Supply Voltage	3.3 V	1 V
Average Dynamic Power	549 micro watt	65.57 micro watt
Operation Frequency	200 MHz	5 GHz

Table 5.3: Comparison between Proposed & Previous Work

VI. CONCLUSION & FUTURE SCOPE

In this paper, we have designed Miller Encoder circuit with the best optimized design of T-flip flop. We have also designed different circuits of T-Flip Flop using CMOS inverters, NMOS digital switches, HLFF technique, pass transistors and GDI cell. Each circuit structure has been designed using 32nm UMC CMOS technology. All the designs have been simulated in HSPICE and correct results have been obtained at clock frequency 5GHz with supply voltage Vdd= 1V and 25 degree centigrade temperature. The average power consumption of designed Miller Encoder circuit is 65.57 µW and power delay product (PDP) is 38.656 fJ. Comparison between different designs of T-flip flop has been studied in detail. Thus for high speed communication systems this best optimized design can be used.

In future Miller encoder can be designed at above 5GHz. As technology is getting advanced, 22nm & 16nm UMC CMOS libraries are also available, therefore this encoder can be designed in different

ISSN No :- 2456- 2165

forms by using different components to reduce the chip size, average power consumed and total cost of the system by optimizing transistors' sizes.

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