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Low Power CAM Cell Design With GDI Based NAND Gate

Priya Kumari
M.Tech Scholar
EC-VLSI
Jagannath University , Jaipur(Raj),India
prsingh441@gmail.com

Nidhish tiwari
Assistant professor
Jagannath National Institute of Technology(JNIT),Jaipur(Raj),India
Nidhishtiwari@Gmail.Com

Abstract :- Content-addressable memory referred as CAM is a hardware table that is used to compare the search data with all the data stored in parallel to it. However, due to the parallel comparison feature the power absorption in CAM is usually considerable where a considerable amount of transistors are in active state on each lookup. This main aim of this paper is to present a hybrid-type CAM design to combine the performance advantage of the NAND type CAM with the efficiency of the power of the NOR-type CAM. In our design, two segments are formed of a single CAM word and then de copulation of all the CAM cells is done from the match line. By applying the NAND logic gates, we get the power absorption of CAM. It is obtained from the experimental results that the search energy consumption can be reduced by hybrid-type CAM by around 89% as compared to the traditional NOR-type CAM. As the NAND CAM to enhance the speed of the light weight match line discharge provides a fast pull down path, the search evaluation of the design is much better than that of the conventional NOR-type CAM. For further reduce the power consumption of the CAM design , we apply GDI methodology. We design the NAND gate with the help of GDI methodology .

Keywords: *Content-addressable memory (CAM), hybrid-type CAM, NAND-type CAM, NOR-type CAM , GDI .*

I. INTRODUCTION

Content-addressable memory (CAM) is unique in its type of computer memory used in some very high speed applications for searching purposes. It is also referred as associative memory, associative storage, or associative array, although the last mentioned term is more often used for a programming data structure. It compares search data provided as an input against a table in which data is stored and returns the address of matching data. Several custom computers, like the Good year STARAN, were constructed to implement CAM, and were designated associative computers.

A. Hardware Associate Array

Unlike standard computer memory ie.RAM in which a memory address is supplied by the user and the RAM returns the stored data word at that address. A CAM is designed in such a way that the user provides a data word and the CAM searches whole of its memory to locate that data word which lies anywhere in it. If the word of data is located in its memory, then the CAM will return a list of all the storage addresses where the word was found. Thus, a CAM in the terms of software is known as an associative array still it is hardware embodiment. The recognition unit of data word was recommended by Dudley Allen Buck in 1955.

B. Standards For Content Addressable Memory

A major interface definition for CAMs and other network search engines (NSEs) was declared in an interoperability agreement called the Look-Aside Interface (LA-1 and LA-1B) developed by the Network Processing Forum, which later merged with the Optical Internetworking Forum (OIF). Numerous devices have been produced by Integrated Device Technology, Cypress Semiconductor , IBM, Broadcom and others to the interface agreement of LA. On the December 11, 2007, the OIF printed the serial look a side (SLA) interface agreement.

C. Semiconductor Implementations

The CAM is designed for the purpose to search its entire memory in one go, it do the job fast than RAM in virtually all search applications. However there is a drawback of cost over it. Unlike a RAM chip, which has simple storage cells, thus a CAM fully parallel must have its own associated comparison circuit in each individual memory bit to indentify a common word between the bit stored and the input bit. In addition to this, there is a need to combine yield of a complete data word match signal to the each cell in the data word. Any addition to the circuitry leads to an increase in the physical size of CAM chip which also increases the manufacturing cost which also increases power dissipation since each of the circuit which is on comparison is active on every clock cycle. So, CAM is applied to only specialized applications where searching speed can't be attained using a cheap method. A recent successful implementation was a GPAP IC and System.

D. Alternate Implementations

To attain a contrary balance between memory size, speed and cost, some applications imitate the function of CAM by making the use of tree search which is standard or in hardware using hashing designs, using tricks on hardware like imitating or pipelining to enhance the effective performance. These sorts of designs are used in routers.

A different approach for the implementation is based on Code Words which are super imposed or Words which are field encoded which are required for more database operations which are more efficient with retrieval of information and logical programming, with hardware implementations lies on both of the head monitoring technology of disk and RAM.*E. Ternary Cam*

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Binary CAM is considered to be the simplest type of CAM which requires data search words made up of only of 1s and 0s. TCAM allows "X" or "don't care" as third matching state of for more than one bits that are in the stored data word, thus it adds up the flexibility to search. For example, a ternary CAM a stored word in its memory of "10XX0" which will find out a match in any of the 4 search words "10010", "10000", "10110", or "10100". The enhanced search flexibility embrace an additional cost on binary CAM as the memory cell built internally must now encode 3 possible states rather than of the 2 of binary CAM. This added state is assigned by adding a mask bit of "care" or "don't care" bit to each of the memory cell.

Associative memory in holographic supplies a model that is mathematical for "don't care" associative and integrated recollection using compound valued representation.

Binary CAM is considered as most basic form of CAM that requires data search word comprising of thoroughly 1's & 0's. Ternary CAM (TCAM) [7] permits a third matching state of "X" or don't consider for one or more bits stored over data word and therefore providing flexibility to search. As an illustration, a ternary CAM may be string a word "10XX)" that will match to any of four searched words "10000", "10100", "10010" or "10110". This flexibility puts an extra cost to binary CAM as integrated memory cells should encode three possible levels apart from two in a binary CAM. This supplementary state is incorporated through a mask bit ("care" or "don't care" bit) to each memory cell.

Holographic associated memory produces a mathematical function for "don't care" integrated associative recollection through presentation of complex value.

TCAM (Ternary content addressable memory) is an outgrowth form of RAM but it also grants access to accumulated data by the contents in spite of address & gives the outcome as address non-similar to RAM. As TCAM is able to accumulate don't care state (x) that is not able to match both of the 0s & 1s in the comparison function, several matches can also takes place. A definite CAM works by comparing the search key will all the words retained in parallel position & provides address as output for best matching address. As TCAM provides higher speed parallel searching function, it is widely used in network routers, data compression, translation look-aside buffers in microprocessors, gene pattern searching in bioinformatics, real time pattern matching in virus detection & image processing. This portion represents memory structure called area efficient ZTCAM that makes use of hybrid portioning of TCAM table for attaining functionality of TCAM. This proposed ZTCAL can be applied in networking deigns where data is put in contrast in parallel manner over higher speed. Presently, TCAM are implemented in networking systems but these are costly & not scaled along the clock rate or area of circuitry compared to SRAM. In this theory, mapping of memory is performed to enhance efficiency of ZTCAM layout. This also helps in minimizing area of the design without putting any effect over delay & time. The clock gating concept is also invaded to design for attaining efficient power management.

As this project is concentrated over CAM constituted over RAM, evaluation of theory is performed to best knowledge & very limited amount of work is put over CAMs based over RAM. RAM based CAM are proposed in [9] makes use of hashing methodology and therefore in-taking inborn drawbacks of hashing like bucket over flow & collisions. Number of accumulated elements put a great effect over the performance. As the number of stored components increases, there will be degradation in performance of this technique. Further, this technique imitates Binary CAM but not TCAM. The technique in [5] makes use of hashing technique for imitating the TCAM functionality with RAM. As per the basis of hashing, this technique that deals with bucket overflow & collisions. This technique may be suffering from various limitations. Initially, performance is dependent over actual record distribution & evaluation of such records. If there are too much records are placed in overflow area because of collisions, lookup will not get finished till multiple buckets get searched. As the stored keys comprises don't care bits in bits position which is used for process of hashing, maintaining identity of don't care bits, these keys should be copied to several buckets that also needs more memory. On the other side, if search key is not comprised of don't care bits that are required by hash function then there is a need to access multiple buckets that also degrades the performance. The main aim for implementing TCAM is that it supports deterministic search performance while hah based CAMs are not having deterministic performance as there some potential collisions takes place & are not much efficient to handle wild-card [18]. The performance of techniques as mentioned in [5, 9] is highly base over hash function. The hash functions having ability to reduce collision possibility are referred as good. Though, for randomized data it is not possible to determine which hash function works better [19]. Pipelined CAMs based over SRAM considers clock cycles for attaining search operation & utilization of memory is not performed in efficient manner [10].

F. Cam Circuits

The provided figure displays a conventional SRAM core cell that by using positive feedback stores the data in back to back inverters. There are 2 access transistors are used to connect the bit lines bland /bl to the storage nodes which are in control of the word line, wl. Data can be read or written into the cell through these bit lines. We can make use of cell which are differential as the building for storage of CAM cells. Figure depicts a conventional binary CAM referred as BCAM cell with the match line written as ml and the differential search lines represented as sl and /sl. The figure also displays the truth value T, which is stored in the cell rooted on the worth of d and /d. To have a clear image in this figure and proceeding CAM core cell figures, Read and write access circuitry is excluded from it. For a binary CAM, a single bit is stored differentially. The comparison circuitry connected to the cell meant for storage do contrasting of the data present on the search lines called as sl & /sl and the data of the binary cells with an operation of XNOR (ml = !(d XOR sl)). A mismatch found in the cell formulates a path from the match line to ground through one of the transistor pairs placed in series. A match of d and sl disrupts the match line from ground.

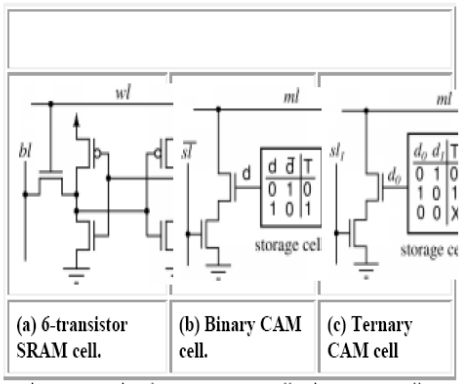

Figure 1:- Conventional SRAM storage cell, Binary CAM cell, Ternary

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II. PROBLEM STATEMENT

NOR gate is consuming more power in the existing design . The memory is design by NOR gate . To enable the memory , use two bit selection line . I1, I0 are the input bit for select the data path of the memory . The data is given by I1,I0 which combined by the decoder . The decoder circuit is design by the combination of the NOR gate . The I1,I0 are the input lines and given the data to the NOT gates . Data proceed by the NOR gate circuit . The output of the decoder are y0,y1,y2,y3.

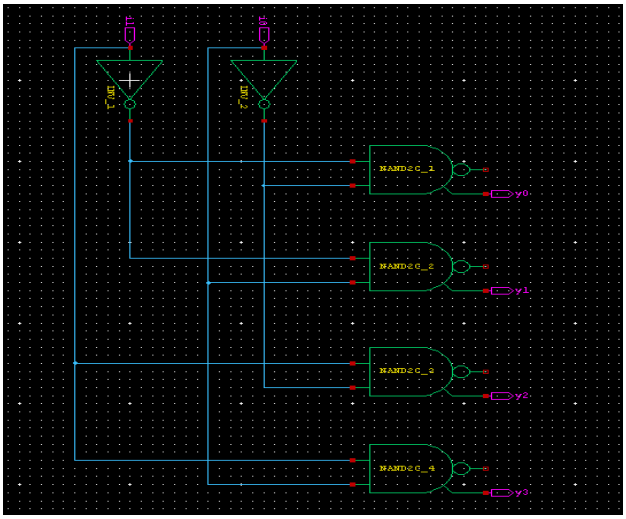

Figure 2:- Decoder circuit for CAM design

For enable to memory four AND gate circuit are used . AND gate are able to execute the memory address .

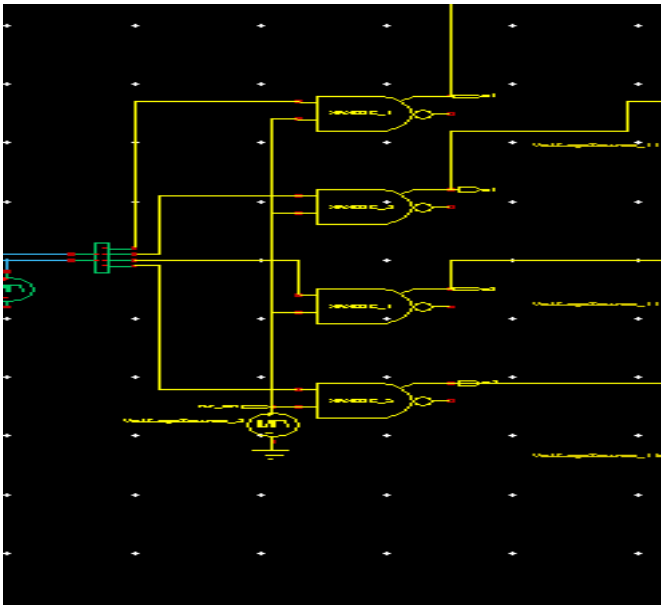

Figure 3:- Enable memory cell design

Three voltage source are using to give the input of the memory . To give the address of the memory , at every memory cell one voltage source is attach .

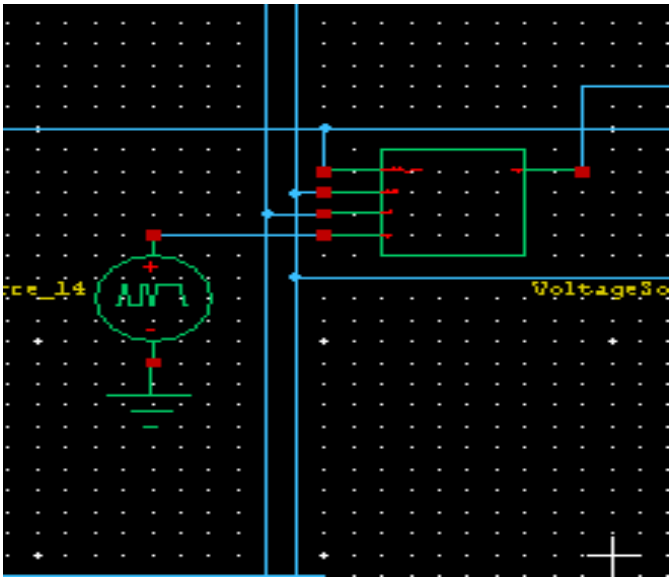

Figure 4:- Memory Cell address

The data of the memory is given by three voltage source . These voltage source are given to the memory address . For design cam based memory ,memory is design by nor gate which consumes more power as compare to NAND gate .

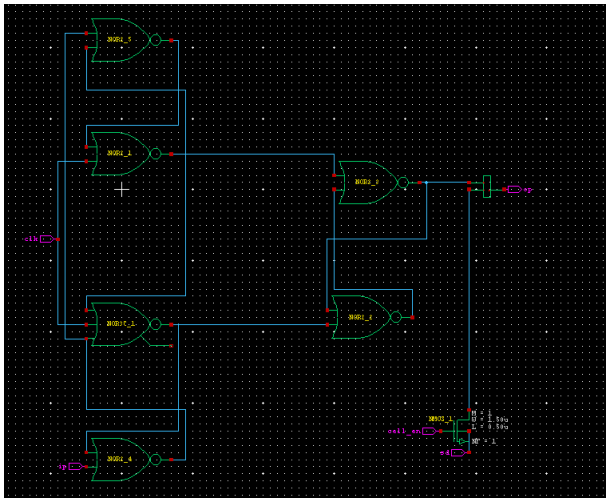

Figure 5 :- NOR gate based design

III. PROPOSED METHODOLOGY

A. Nand-Type Cam

In, the NAND-type CAM the primary aim is to reduce the power abandoned in search operation, in which the CAM cell is devised as XNOR-type rather than the XOR-type and the pull-down transistors of each of the CAM cell in the word similar to its type are arranged in NAND type, as represented in Fig. 6. The match line in its initial stage is pre charged to high and discharged to 0 when the condition that all CAM cells are matched is satisfied. As there is only one match line that is discharged to 0 during the process of searching and the load capacitance of match line is quite small, the power consumption is

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minimal. However, the match line discharge is very slow because the pull-down path is very much long in case to do a match. Thus, the NAND-type CAM trades the performance degradation for a large power saving.

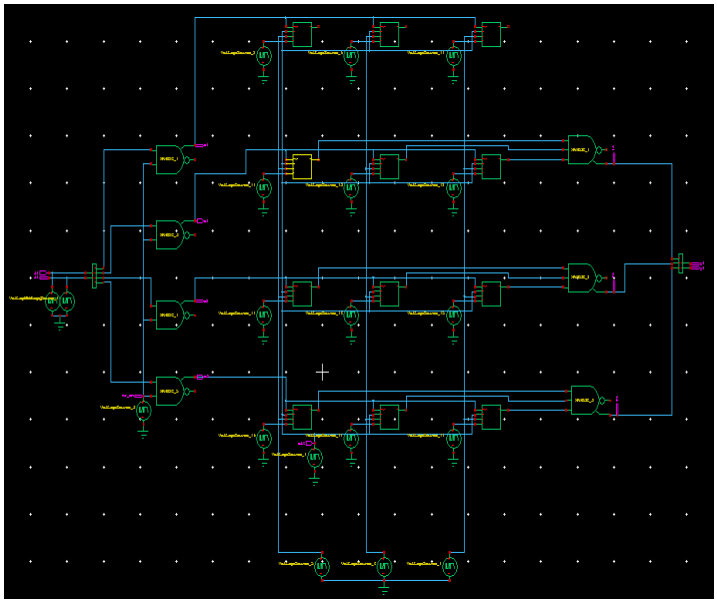

Figure 6:- CAM design by NAND gate

We are giving the input from i1,i0 as the memory input . The value of the bit is giving by voltage source . For select the memory address , use NAND gate design , which select the memory address . The data is saving into the memory according to below image . The memory is given by three voltage source . Design of the memory cell is by NAND gate according to image number 8.

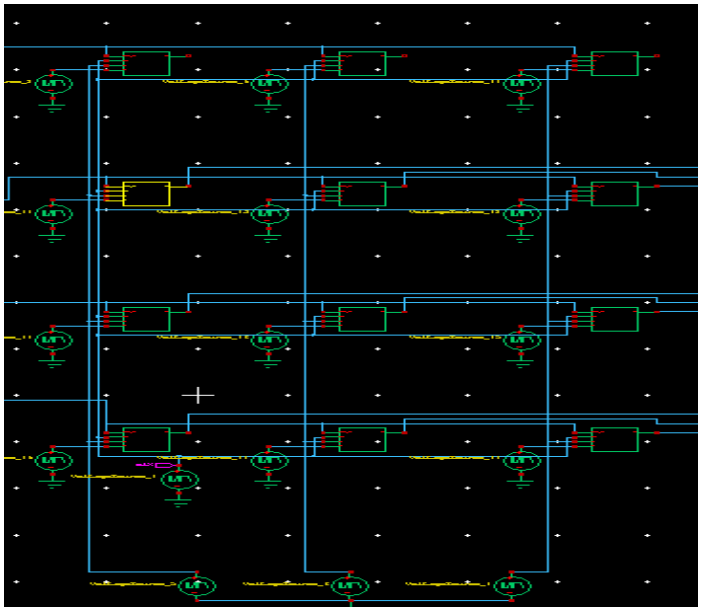

Figure 7:- Cam Design Memory

The CAM design memory cell is designed by NAND gate .Cam based memory cell design use 6 NAND gate . The input of these NAND gate are clock . NAND cell is giving low power consumption as compare to NOR gate .

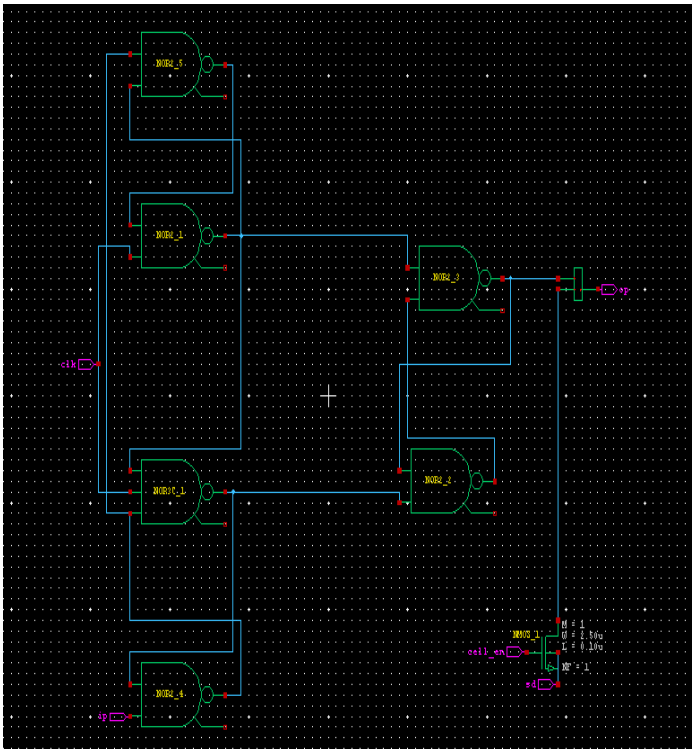

Figure 8:- Memory cell design by NAND gate

B. GDI Methodology

For reduce the power consumption and number of transistor we are applying Modified GDI methodology .Morgenshtein et al. investigated a high-speed and multipurpose logic style for low power electronics design, known as Gate Diffusion Input (GDI),[7] with reduced area and power necessities, and proficient of implementing a broad variety of logic functions. FIG. 9 shows basic M-GDI logic cell, which is used for implementing verity of logic functions and circuits at low power and high speed design where G, P and N are three inputs and output is taken from D terminal. Fig 10 is showing the design of NAND gate by GDI technique .The design NAND gate will be use in Proposed CAM cell.

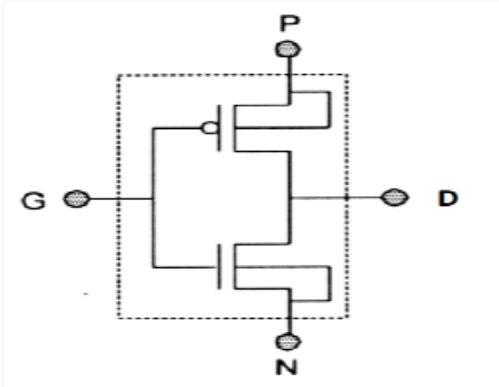

Figure 9:- Basic M-GDI Cell

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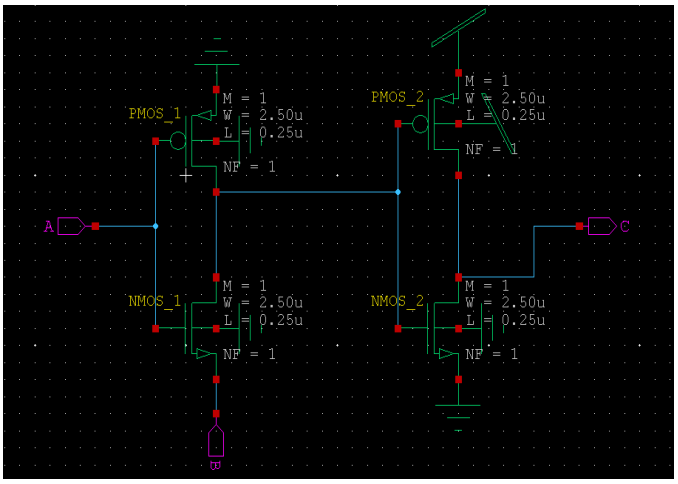

Figure 10:- NAND gate design by GDI Technique

IV. RESULTS

A. NAND Gate Based CAM

For the existing design NOR gate is using for design the memory cell . NOR gate consumes more power as compare to NAND gate . By the NOR gate power consumption is getting 1.220 x 10^-4 .

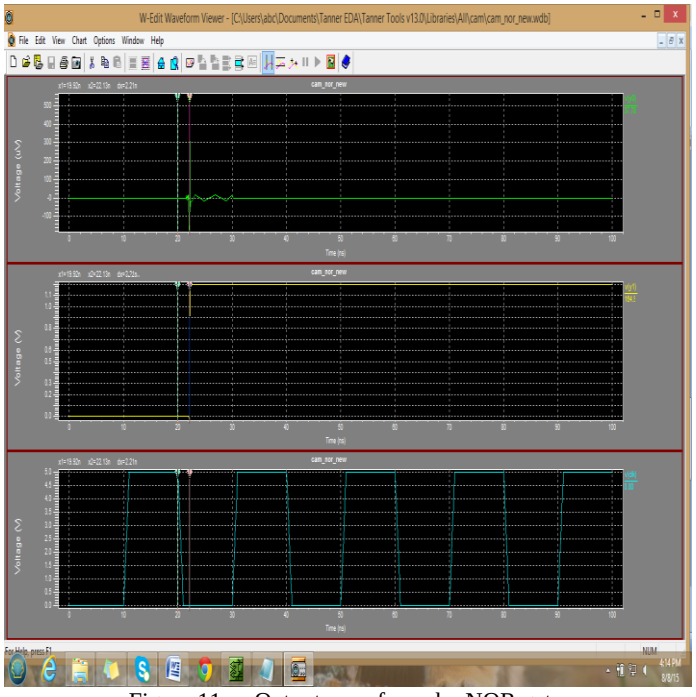

Figure 11 :- Output waveform by NOR gate

B. Proposed Design (Nand Gate With GDI Based Cam Design)

For the proposed design we use NAND gate with GDI for improve the performance of the Cam memory cell . Basically we involve the GDI based NAND gate design in cam memory design . By this results of the power get reduced . GDI based NAND consumes less power as compare to NOR . The power consumption for GDI based NAND gate CAM cell is 5.607793e-005 watts.

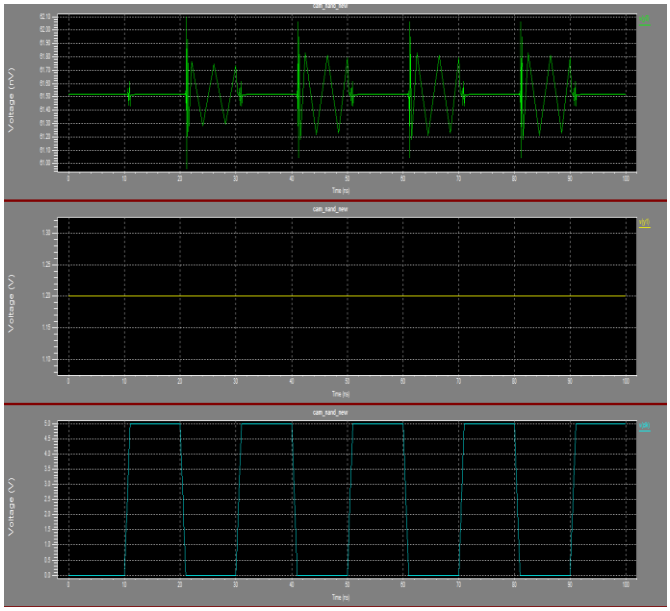

Figure 12:- Output wave form for the GDI based NAND gate design

	Power
NOR Gate based CAM	1.220233e-004 watts
GDI based NAND Gate CAM cell	5.607793e-005 watts

Table 1 :- Comparison Table

V. CONCLUSION & FUTURE SCOPE

A. Conclusion

In this paper , we are proposing the GDI based NAND gate for the design of CAM memory cell . NOR gate consumes more power as compare to NAND gate . For further reduce the power consumption from the NAND gate based CAM cell design , we apply GDI methodology . GDIs will be able to further reduce the power consumption of the circuit .NOR gate based CAM design consume 1.220233e-004 watts . Proposed design is done by GDI based NAND gate . GDI based NAND gate is design for CAM memory cell . The power is reduced up to 5.607793e-005 watts from the proposed design .

B. Future Scope

In the future for further reduce the power consumption of the NAND gate based CAM cell we can use power gating technique and also can be use Clock gating techniques. These two techniques are able to further reduce the power consumption of the CAM cell.

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