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A Review for Fault Tolerant Full Adder/Subtractor Using Reversible Gates

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Abstract:- Reversible Logics are very important and useful for the future computational technologies. Reversible Logic is an important Research Area which is using for CMOS design with Low Power. In this paper, we give the Chronically Review for the Fault Tolerance Full Adder/ Subtractor. We are also showing the logical circuit for the Fault Tolerance Adder/ Subtractor.

Keywords- COG, delay Reversible gate ,Feynman double gate, Fredkin gate, full adder, MIG.

I. INTRODUCTION

Reversible Logic Gates are using mostly in VLSI Domain for Design CMOS Circuit just due to Low Power Capability and low delay property. In the Present time, Quantum Computers are using Reversible Logic Gates. Reversible Logic Gates have lots of applications like low power CMOS. Optical important processing, Quantum Computational, DNA-based computing and Nano Technology. In 1960 R.Landaurer's presented that design system by using Irreversible Hardware design is showing energy consumption and information design is showing high energy consumption and information loss.

A Process, in which impulses reduced to output is called reversible logic; Irreversibility logic gate is the primary factor for dissipation more Power Consumption. The most important computational in energy. Reversible Logic Gate are related to the Power when Landauer[1], prove that loss of information occurs from the irreversibility of function to power consumption in 1961. They inform that Power consumption in the circuit is getting due to one bit Loss information and equal to KITn2 . Here k is a Boltzmann Constant while T is a Temperature. In the 1973, they give the rule that Reversible Logic Gate can reduce power consumption. In the theorem, they prove that power consumption will not perform from the circuit if input extract from the output and reversible logic gate might be used.

II. REVERSIBLE GATES

A. Basic Reversible Gates

Peres Gate, Feynman Gate, Toffoli Gate, Fredkin Gate, BVF Gate are the Reversible Logic Gate which is showing in Figure 1. Due to low Cost and simplicity CMOS-based circuit and tools are combined easily from Reversible Logic Gate.

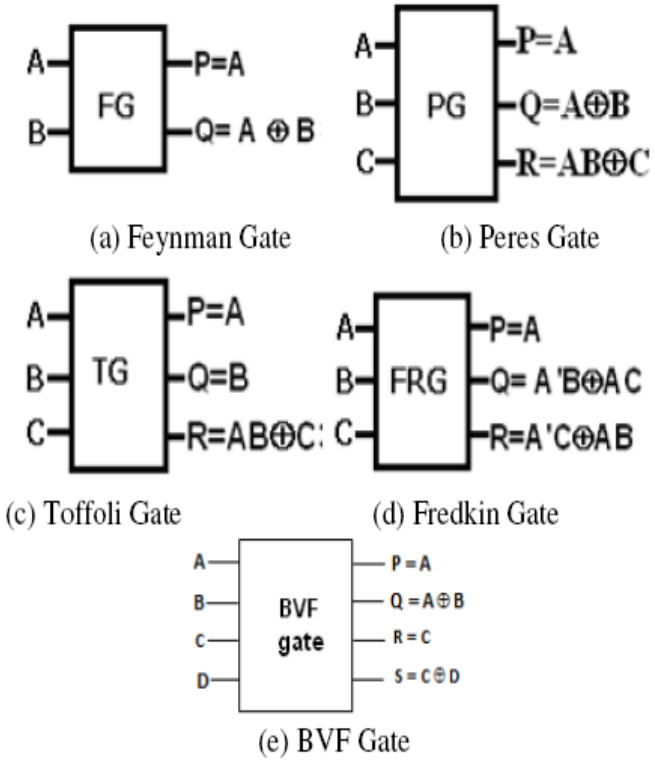

Figure1:- Few preferred Reversible Gates

B. Parity Preserving Reversible Gates

Fault Tolerance has a characteristic which enables to the system and gracefully depends for continues operating property. If the system generates Fault Tolerant itself, in this case, Fault Correction get early, and simple Fault Tolerant is getting from Parity in many systems. Reversible with Parity preserving circuit would by upcoming design which will be used in developing for Fault Tolerant with Reversible system for nanotechnology. Networking of the gate will be Parity Preserving if the Gates are Parity Preserving [5].

Some Reversible Logic Gate with Parity Preserving is described in literature Review. In that 3*3 Feynman Double Gate (F2G) [5], Fredkin Gate (FRG) [10], described in Figure 2.

Parity Preserving Gate F2G and FRG input-output characteristics is showing in Table I and II . The Parity Preserving Reversible Logic Gate provide A xor B xor C = P xor Q xor R and for K*K Reversible Logic ,where Ex-OR of

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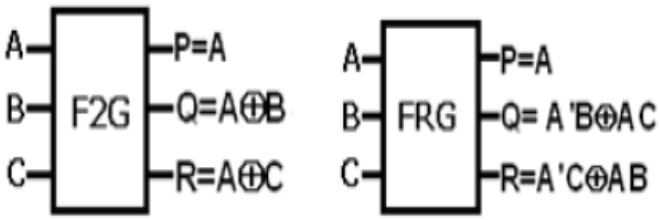
the input is Ex-OR to the output and it will be Parity Preserving .



(a) ***(b)***

Figure 2:- (a)Feynman Double Gate (F2G), (b) Fredkin Gate(FRG)

TABLE I. Table of Parity Preserving Feynman Double Gate (F2G)

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

TABLE II. Table of Parity Preserving Fredkin Gate (FRG)

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Implementation of Reversible Logic has been described in the Literature of the Paper. Reversible Adder circuit is shown by at least two Garbage Output with one constant input. For Fault Tolerant Reversible Logic Gate requirement is not same. Due to Parity input match with output Parity for a Fault Tolerant Adder circuit. In the section, we describe Half Adder/ Subtractor module while another circuit is designed for minimum Garbage output number and Constant input.

C. Design of Half Adder/Subtractor Circuit (FTHA_S)

The basic for the Parity Preserving Reversible Gate Feynman Gate and Fredkin Gate have been explained for the Half adder is

$$Sum = A \text{ Xor } B \quad .....(1)$$
$$Carry = A \text{ and } B \quad .....(2)$$

Half Subtractor Boolean Expression is

$$Difference = A \text{ Xor } B \quad ..... (3)$$
$$Borrow = ((Not\ A) and\ B) \quad .... (4)$$

From the equation (1) and (3), we can see that both are the same. The difference is in between Carry and Borrow. In this Section, we design both Adder / Subtractor. In this Adder / Subtractor, 0 is using for addition and Logic 1 is using for subtraction. From the Figure 3, we can check that there are three input A, B, and Cntrl signal. The control signal is using for control the operation of addition and subtraction.

In Figure 3 , S/D is Sum/Difference while C/B is defined as carry and Borrow. Remaining all the other outputs are Garbage Value. For Design the Half Adder / Subtractor two F2G reversible gate and 2 FRG gates are using. Figure 4 is showing the Fault Tolerance Half Adder / Subtractor Block Diagram. In this Block Diagram A, B, Cntrl are the input and seven output where S/D and C/B are the output.

$$S/D = A \text{ Xor } B \quad .....(5)$$
$$C/B = ((Not\ Cntrl) \text{ and } A \text{ and } B) \text{ or } (Cntrl \text{ and } (Not\ A) \text{ and } B) \quad .....(6)$$

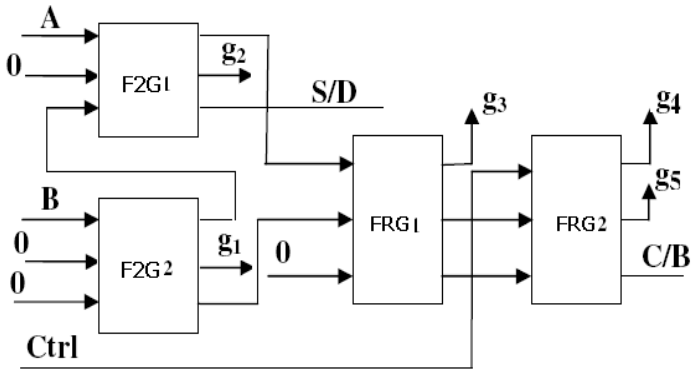


Figure 3. Circuit of reversible fault tolerant Half Adder/Subtractor

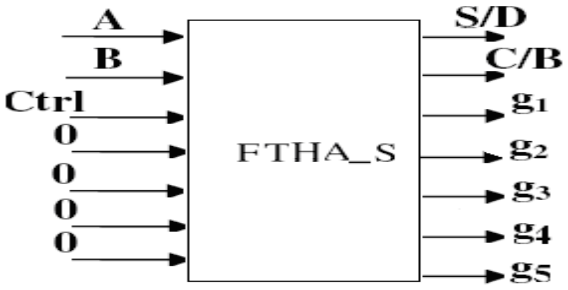


Figure 4. Half Adder/Subtarctor circuit with four constant inputs & five garbage outputs

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D. Design of Full Adder/Subtarctor Circuit (FTFA_S)

Conventional Approach is using for design Full Adder/ Subtractor. In this Conventional Approach, two Half Adder circuit are using. The Block Diagram of the Fault Tolerant Full Adder/ Subtractor is showing in Fig 5. The expression is shown as

$$Sum = A \text{ Xor } B \text{ Xor } C \quad .....(7)$$

$$Carry = ((A \text{ Xor } B) \text{ and } Cin) \text{ Xor } (A \text{ and } B) \quad .....(8)$$

The expression for full subtractor is:

$$Difference = A \text{ Xor } B \text{ Xor } C \quad .....(9)$$

$$Borrow = ((Not\ A) \text{ And } B) \text{ or } (B \text{ and } C) \text{ or } (C \text{ and } (Not\ A)) \quad ....(10)$$

As we can see in Figure 5 , A, B , C, Cntrl signals are the input. In the Full Adder / Subtractor, three inputs A, B, C are using while Cntrl signal is using for control the operation of the Adder/Subtraction. When the Control signal is 0 then addition will perform, and when the Control Signal is 1 then Subtraction will perform S/D, and C/B are the Sum and Difference, Carry and Borrow. In this Design, we are using two Half Adder / Subtraction while one F2G Gate.

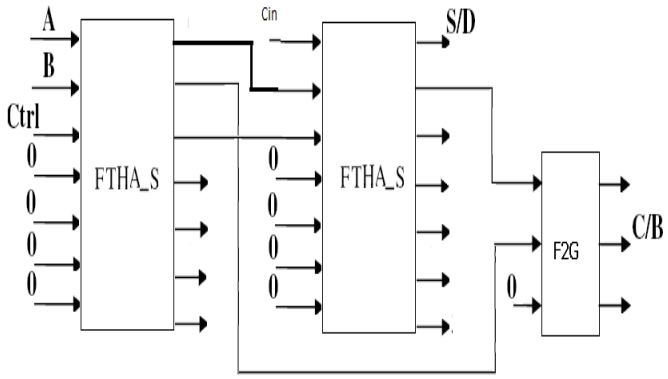

Figure 5. Circuit of reversible fault tolerant Full Adder/Subtractor

III. CHRONOLOGICAL REVIEW

In 2012 Parminder Kaur[et.al] presented a paper for reversible logic gate. Reversible Logic Gate are presented in many Research and it is the latest topic for research. In this paper author is working for full adder which is based on fault tolerant. The design can work singly as a reversible Full Adder/Subtractor unit. It is a parity preserving reversible adder cell, that is, the parity of the inputs matches the parity of the outputs. The proposed parity preserving reversible adder can be used to synthesize any arbitrary Boolean function. It allows any fault that affects no more than a single signal readily detectable at the circuit's primary outputs. The proposed design offers less hardware complexity and is efficient in terms of gate count, garbage outputs and constant inputs than the existing counterparts.

In 2013 Prashanth[et.al] presented a paper for the reversible logic gate. Reversible Logic Gate are the latest technology which is working for low CMOS design. Reversible Logic gate are using in many type of applications like Quantum Computing , Nano Technology and optical commuting. This proposes the design of efficient fault tolerant carry skip adder/Subtractor. Design of carry skip adder/Subtractor requires full adder/Subtractor and parallel adder/Subtractor those designs also included in this paper. In this paper all the designs are efficient in terms of gate count, constant input, garbage output and quantum cost. The proposed design work singly as a unit which consist both adder and Subtractor, according to the control logic input it can act adder or Subtractor. The below section covers Full adder/Subtractor and Parallel adder/Subtractor design required for the construction of Carry skip adder/Subtractor.

In 2014 Dondapati Naresh[et.al] presented a paper for Reversible Logic Gate. Reversible Logic Gate plays an important role in VLSI Domain. Nowadays, It has voluminous applications in quantum computing, optical computing, quantum dot cellular automata and digital signal processing, low power CMOS design, nanotechnology. This paper proposes the fault tolerant carry skip adder/subtractor by using parity preserving reversible logic gates. According to the control logic input the proposed design can works as a carry skip adder or carry skip subtractor. The design will consists of control line ctrl which will selects adder or subtractor according the control logic input i.e. when ctrl is 0 it will acts as parallel adder and when ctrl is 1 it will acts as parallel subtractor.

In 2015 S.Mounika[et.al] presented a paper for the reversible logic is a most popular and emerging field in low power consideration. It will be having many applications in quantum computing, nanotechnology and optical computing etc. This proposes the design of efficient fault tolerant carry skip adder/subtractor. Design of carry skip adder/subtractor requires full adder/subtractor and parallel adder/subtractor those designs also included in this paper. In this paper all the designs are efficient in terms of gate count, constant input, garbage output and quantum cost.

In 2016 Subramanian Saravanan[et.al] presented paper for Reversible logic is a new emerging technology with many promising applications in optical information processing, low power (Complementary Metal Oxide Semiconductor) CMOS design, (DeOxy RiboNucleic Acid) DNA computing, etc. In industrial automation, comparators play an important role in segregating faulty patterns from good ones. In previous works, these comparators have been implemented with more number of reversible gates and computational complexity. All these comparators use propagation technique to compare the data. This will reduce the efficiency of the comparators. To overcome the problem, this paper proposes an efficient comparator using (Thapliyal Ranganathan) TR gate utilizing full subtraction and half subtraction algorithm which will

improve the computation efficiency. The comparator design using half subtraction algorithm shows an improvement in terms of quantum cost. The comparator design using full subtraction algorithm shows effectiveness in reducing number of reversible gates required and garbage output.

IV. CONCLUSION

In this paper, we introduce the Fault Tolerant Full Adder/Subtractor by Reversible Logic gate with low delay for improve the performance of the fast adder and Subtractor .We give the Chronological Review for the different papers for Fault Tolerant Reversible Logic Gate .

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