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Analysis and Design of Full Adder Circuit in Source Couple Logic (SCL)

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***Abstract*— Presently source-coupled logic (SCL) circuits are widely used in mixed mode designs. This is because of several advantages associated with SCL circuits in terms of delay (D), number of transistors (N), current spike (I_S) and power-delay-number of transistor-current spike-product ($PDNI_SP$) are these have lower values compared to other circuit design techniques. However, the power consumption of SCL circuits is higher. In the present dissertation, various full adder circuits reported in literature have been considered.**

Properties of the electronic devices change with the variation in process parameters. Process variation is due to variations in the manufacturing conditions such as device dimension, pressure and doping concentration. The variations of various parameters of the full adder circuits with respect to change in process corners has been analysed in the present work.

The working of SCL circuits and an SCL circuit minimization technique namely multiplexer-minimization technique are studied. Performance of full adder circuits viz. SERF, SERF-Imp, PTL, CMOS, SCL, SCL-Min and SCL-Gated has been analysed in terms of $PDNI_SP$. Power, delay, power delay product, number of transistors, current spike, $PDNI_SP$ and voltage swing are considered as performance parameters. To study the effect of change in process corners on performance parameters of full adder (FA) circuits, different full adder circuits are analysed in 180nm, 130nm, 90nm and 45nm technology nodes. An SCL full adder (SCL-Gated) and an encoder have been proposed for improved power consumption.

From the analysis, it is observed that SCL circuits exhibit low value of I_S and $PDNI_SP$ but at the cost of some other performance parameters such as power and PDP. The performance of proposed FA circuit has been compared with the other SCL FA circuits reported in literature. Power and PDP is significantly reduced in case of SCL-Gated circuit but with slight increase in $PDNI_SP$.

I. INTRODUCTION

SCL is a dual rail logic circuit that use both the variable and its complement (A, A') as an input pair. The output of a dual rail circuit is also a pair (E, E') that drives the next gate(s) in the logic cascade. However, dual rail logic interprets the difference (E - E') as the logic variable instead of just one or the other. When viewed at the level of Boolean algebra, the use of both the variable and it is complement is superfluous; the result is the same as that found using a single-rail circuit. Moreover, dual rail networks are more complicated to wire.

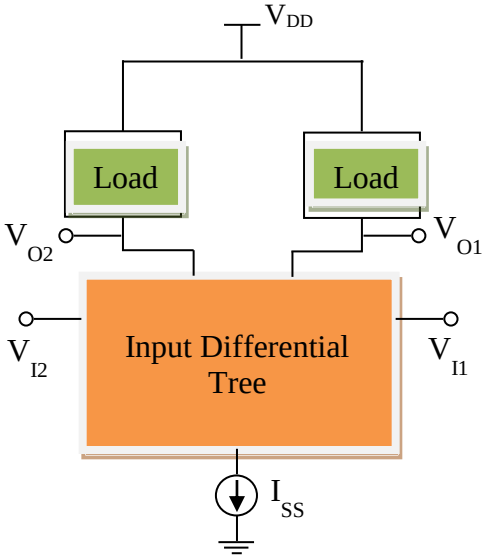

Fig 1. circuit schematic of an SCL gate

The circuit schematic of an SCL gate, shown in Figure 1 is made up of load pair, input differential tree and current source. Input differential tree is made up of NMOS source-coupled pair having transistors working in the saturation or cut off region, that approximate well the behavior of a voltage-controlled current switch. The biasing current (I_{SS}) is steered to one of the two output branches and converted into a differential output voltage by two PMOS transistor working in the linear region (active load pull-up resistance). The logic function of the SCL is implemented by the input differential tree. For an inverter/buffer, the

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logic block is the differential pair constructed by NMOS transistors.

The SCL gate uses PMOS active load, but other types of load, such as physical resistor or a diode-connected NMOS/PMOS could be used. However, resistor load is not normally chosen since large silicon area needed and its parasitic capacitance can be high. For the second type of load, the output levels will loss the threshold voltage furthermore; the MOS diode load is slower than the PMOS active load for practical bias currents.

II. PROBLEM FORMULATION AND RESEARCH OBJECTIVES

Delay (D), number of transistors (N), current spike (I_S) and the product of P, D, N and I_S (i.e. PDNI$_S$P) performance criteria.Design and analyses of low power and high performance source coupled logic circuits. This shall be based on power (P),

To fulfill the above research problem, the following objectives have been dealt with:

- Detailed literature survey has been carried out.
- Full adder circuit has been considered.
- Design, analyses and implementation of full adder circuit using SCL.
- Analysis of full adder using different other logics namely pass transistor logic, CMOS logic, etc. has been done.

Performance analysis of the circuits for different technology nodes using Tanner EDA Tool has been carried outof the current designations.

III. DESIGN ISSUES IN SOURCE COUPLED LOGIC

The operation of the SCL logic is based on the input differential pair circuit. The two inputs control the flow of current through the two branches of the differential pair. For example, in **Figure 2**, if V_{GS} (M_2) is higher than V_{GS} (M_1), the current I_{D2} exceeds the current I_{D1}. Therefore, the output voltage V_{O2} begins to drop until it reach steady state, where the current going through PMOS active load (M_4) matches the I_{D2}. In mean time V_{O1} is charged to V_{DD} through M_3.

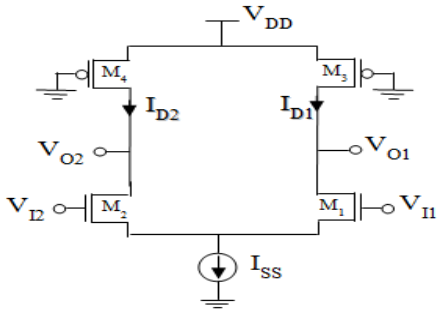

Fig 2. SCL logic

The output voltage swing V_{SWING} is defined as voltage difference between V_{O1} and V_{O2} at steady state. The amount of current passing through the ON branch (M_2) controls the delay of the logic gate transition (1→0), while the PMOS active load (M_3) controls the charging of the output nodes (0→1 transition). Defining ΔV as the voltage drop of M_3 (M_4) due to the drain current equal to I_{SS}, the logic swing (V_{SWING}) of the gate will be equal to 2ΔV. To achieve best performance, all current must pass through the ON branch and the load resistance (PMOS) should be small in order to reduce the RC delay. This guarantees that the voltage is V_{DD} - Iss.R_D, where I_{SS} is the current flowing through current source and R_D is the PMOS equivalent linear resistance.

IV. SCL CHARACTERISTICS

As conversion from current-to-voltage in the SCL inverter is performed by the two PMOS transistors M_3-M_4, both of which have a source-gate voltage equal to V_{DD} and a much smaller source-drain voltage (in order of hundred milli-volts). Therefore, transistors M_3-M_4 work in the triode region and can be modeled as an equivalent linear resistor R_D.

Using the standard BSIM3v3 MOSFET model, under the static condition, PMOS transistor can be suitably approximated by an equivalent linear resistance R_D given by:

$$R_D = R_{int}/\left(1 - (R_{DS}/R_{int})\right) \quad (1)$$

Where R_{DS} = (R_{DSW} ×10^{-6})/W_P models the source/drain parasitic resistance which depends on the empiric model parameter R_{DSW} as well as the PMOS transistor effective channel width W_P. R_{int} is given by:

$$R_{int} = 1/\left[\mu_{eff,P}.C_{ox}.\frac{W_P}{L_P}.\left(V_{dd} - |V_{th}\right.\right. \quad (2)$$

This represents the intrinsic resistance of PMOS transistor in the linear region (it does not account for the parasitic drain/source resistance). In Eq. 2 the $\mu_{eff,P}$ represents the effective hole mobility, parameter L_P is the PMOS effective channel length, C_{ox} is the oxide capacitance per area and $V_{th,P}$ is the threshold voltage.

The output voltage $V_O(V_i)$ of SCL inverter can be evaluated by substituting the equivalent resistance R_D in Eq. 1. Thus, the differential output voltage V_O is equal

$$V_O = V_{O2} - V_{O1} = -R_D.(I_{D1} - I_{D2}) \quad (3)$$

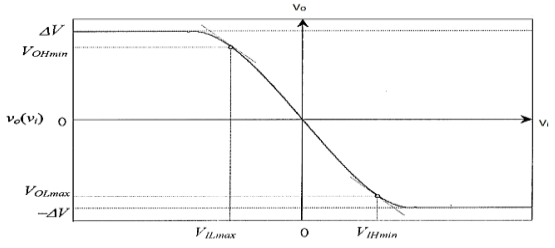

Figure 3 .

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The minimum differential input (V_i) required to fully switch the entire tail current I_{SS} to one side is given by:

$$V_i = \sqrt{2I_{SS}/\mu_n C_{OX}(W/L)} \quad (4)$$

This gives output transfer characteristics:

$$v_o(v_i) = \begin{cases} R_D I_{SS} & \text{if } v_i < -\sqrt{\frac{2I_{SS}}{\mu_n C_{ox} W_n/L_n}} \\ -vR_D I_{SS}\sqrt{\frac{\mu_{eff,n}C_{ox}}{I_{SS}}\frac{W_n}{L_n}}\sqrt{\left(\frac{\mu_{eff,n}C_{ox}}{I_{SS}}\frac{W_n}{L_n}v_i\right)^2} & \text{if } |v_i| \le \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} W_n/L_n}} \\ -R_D I_{SS} & \text{if } v_i > \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} W_n/L_n}} \end{cases}$$

(5)

Where, $V_i = V_{i1} - V_{i2}$ (Differential input). From Eq. 5, $V_{OL} = -R_D . I_{SS}$ and $V_{OH} = R_D . I_{SS}$, then the logic swing is equal to:

$V_{SWING} = V_{OH} - V_{OL} = 2.R_D . I_{SS} = 2\ \Delta V$ (6)

The $V_{SWING}/2$ ($I_{SS}.R_D$) must be kept low enough to ensure the NMOS transistors M_1-M_2 are not in the triode region. In particular, when the gate voltage of an NMOS transistor is high (equal to V_{DD}), the drain voltage is equal to $V_{DD} - I_{SS}.R_D$, the triode region can be avoided if the gate-drain voltage V_{GD} is lower than threshold voltage by:

$$V_{GD} = V_{DD} - [V_{DD} - R_D.I_{SS}] = R_D.I_{SS} \le V_{th(7)}$$

Which imposes an upper bound to $I_{SS}.R_D$ and hence the logic swing is given by Eq. 6.

V. NOISE MARGIN (NM)

Due to the symmetrical property, the logic threshold is equal to zero ($V_{LT} = 0$) and the associated small-signal voltage gain is $g_{m,\ n.RD}$, (where $g_{m,n}$ is the small-signal transconductance of transistor M_1-M_2 with $I_{D1,2} = I_{SS}/2$). Since $v_{i1} = v_{i2} = v_{o1} = v_{o2} = V_{DD} - \Delta V/2$ and $I_{D1,2} = I_{SS}/2$, when the gate is biased around logic threshold, voltage V_{DS} of transistor M_1-M_2 is equal to their V_{GS}.

Hence, the resulting expression of the voltage gain A_V is :

$$A_V = g_{m,n}.R_D = \Delta V.\sqrt{\mu_{eff,N}.C_{ox}.\frac{W}{L}} \quad (8)$$

The NM is equal to NM_L (for Low-Logic) and similar to NM_H (for High-Logic) due symmetrical

property, which is defined as $NM_H = V_{OHmin} - V_{IHmin}$ ($NM_L = V_{ILmax} - V_{OLmax}$) where V_{ILmax} and V_{IHmin} are the input voltage values such that $\partial V_O/\partial V_I = -1$. V_{OLmax} and V_{OHmin} are the corresponding output voltages ($V_{OLmax} = V_O(V_{IHmin})$ and $V_{OHmin} = V_O(V_{ILmax})$).

VI. MULTIPLEXER MINIMIZATION TECHNIQUE

In the multiplexer- minimization (MUX-MIN) technique [3], NMOS differential pairs are treated as 2 X 1 current multiplexer (I-MUX) stages. In **Figure 4**, for example, the input variable A and Ab acts as a select line to the lowest level NMOS differential pair (I-MUX) stage to steer I_{SS} into either node X or node Y. MUX-MIN is based on the Shannon Expansion Theorem wherein a logic function F(A, B, C,…) with n-input variables is factored first with

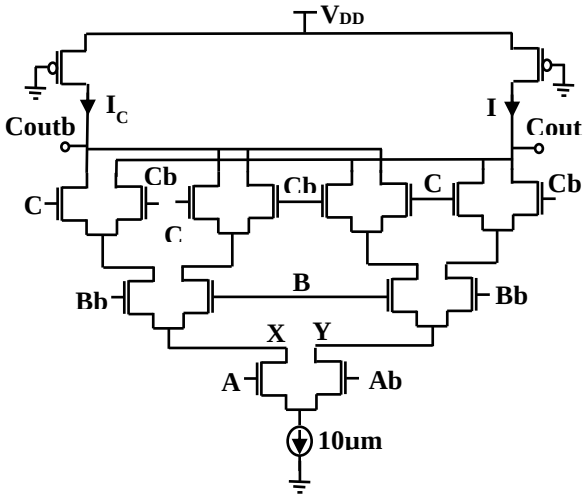

Figure 4.Carry circuit of Full Adder

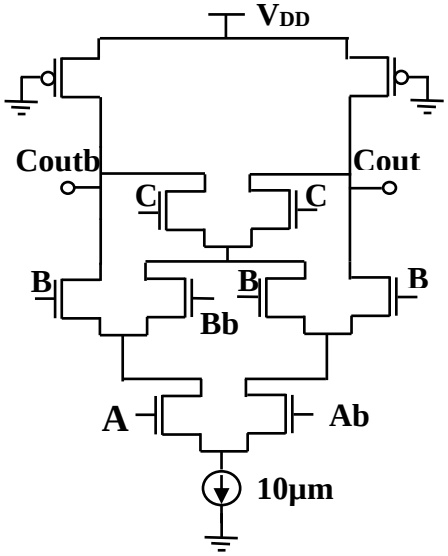

Figure 5.Carry circuit of Full Adder after minimization using MUX-MIN technique.

Respect to the variable A as

F(A, B, C,…)=F(0, B,…).Ab+ F(1, B,…).A

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where F(0, B,…) and F(1, B,…) are F(A, B, C,…) evaluated with A = 0 and A =1 respectively.

In contrast to conventional static CMOS logic, current steering is the basic principle of operation of SCL. Hence, the logical expression for I_C (Figure 5) is expanded rather than that for Coutb and similarly, I is synthesized rather than Cout. I and I_C are the current flowing through load devices connected at Cout and Coutb outputs respectively as shown in Figure 5. The expression for I and I_C can be obtained from Table .1

Table3.1 Ordered Truth Table For Carry Output

A	B	C	Cout	I	Coutb	I_C
0	0	0	0	1	1	0
0	0	1	0	1	1	0
0	1	0	0	1	1	0
0	1	1	1	0	0	1
1	0	0	0	1	1	0
1	0	1	1	0	0	1
1	1	0	1	0	0	1
1	1	1	1	0	0	1

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In contrast to conventional static CMOS logic, current steering is the basic principle of operation of SCL. Hence, the logical expression for I_C (Figure.5) is expanded rather than that for Coutb and similarly, I is synthesized rather than Cout. I and I_C are the current flowing through load devices connected at Cout and Coutb outputs respectively as shown in Figure.5 The expression for I and I_C can be obtained from Table 1.

The MUX-MIN expansion of I_C, with respect to A follows from (9) as

$$I_C = A.B + B.C + A.C$$

$$= I_C(0, B, C).Ab + I_C(1, B, C).A$$

$$= Ab.B.C + A.Bb.C + A.B \quad (10)$$

Similarly, the expression for I(A,B,C) = I_Cb(A,B,C) = Ab.Bb + Ab.Cb + Bb.Cb

$$= I(0, B, C).Ab + I(1, B, C).A$$

$$= Ab.Bb + Ab.B.Cb + A.Bb.Cb \quad (11)$$

An example of MUX-MIN technique applied to SCL carry circuit is shown in Figure 5. Since, Eq. (10) is sum of three terms: Ab.B.C, A.Bb.C and A.B. Therefore, to realize Coutb function, three branches are connected to Coutb node. First branch consist of transistors M_C-M_{B2}-M_{Ab} corresponding to Ab.B.C term. Second branch consist of transistors M_C-M_{Bb1}-M_A corresponding to A.Bb.C term. And third branch consist of transistors M_{B1}-M_A corresponding to A.B term. Similarly, for the realization of Cout function, three branches that consist of transistors M_{Bb2}-M_{Ab}, M_{Cb}-M_{B2}-M_{Ab}, M_{Cb}-M_{Bb1}-M_A are connected to the Cout node. These branches correspond to Ab.Bb, Ab.B.Cb and A.Bb.Cb terms respectively of Eq. (11). Therefore, current $I_C = I_{SS}$ flows into the decision tree from node Coutb, only when Eq.(10) is true, else current I_{SS} flow into the decision tree from node Cout.

VII. PERFORMANCE PARAMETERS

Performance parameter is used to qualify the quality of any design. The various performance parameters in the design of SCL full adder circuits for reduced power are presented in this section.

1. Power

The power consumption determines how much energy consumed per unit time and how much heat is dissipated by the circuit.

2. Delay

Delay is defined as how fast circuit responds to the change in the input. It is measured between the 50% transition point of the input and output waveform.

3. Power Delay Product (PDP)

It is product of the value of power and delay.

4. Number of Transistors (N)

This parameter is measure of the number of transistors used in the circuit. This parameter also indicates indirectly the area occupied by the circuit.

5.Current Spike (I_S)

It is the measure of maximum value of current flowing between power supply (V_{DD}) and ground terminal (GND).

6. Power-Delay-Number of Transistor-Current Spike-Product ($PDNI_SP$)

This parameter is indicates the product of power, delay, number of transistors and current spike. This parameter has been considered as Figure of Merit (FOM) of this work.

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7. Voltage Swing (V_{SWING})

Voltage swing is the difference between maximum and minimum value of a signal

VIII. SUMMARY

This provides detail discussion about SCL circuit operation along with voltage characteristics and noise margin. The multiplexer minimization technique used to minimize SCL Circuits is also discussed. Various performance parameters used in the analysis are explained.

IX. FULL ADDER CIRCUITS

A. Static Energy-Recovery Full (SERF) adder

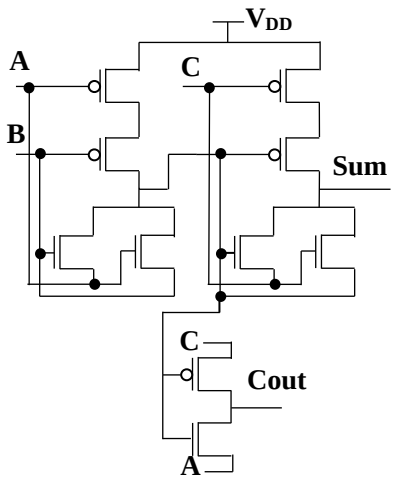

Figure.6. Static Energy-Recovery Full (SERF) adder

B. Improved SERF adder

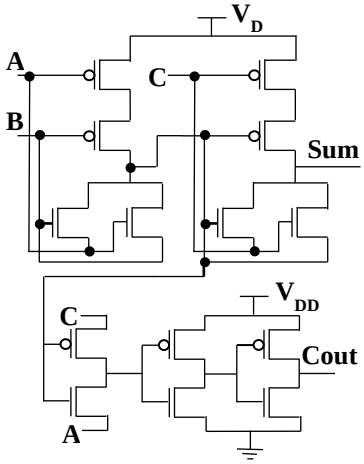

Figure.7. Improved SERF adder

C. Full adder circuit implemented using 14 transistor

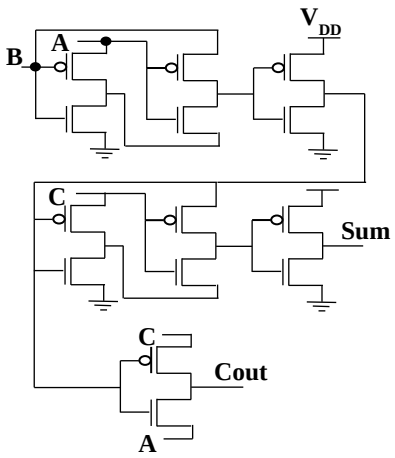

Figure.8. Full adder circuit implemented using 14 transistor

D. Full Adder circuit implemented in CMOS Logic

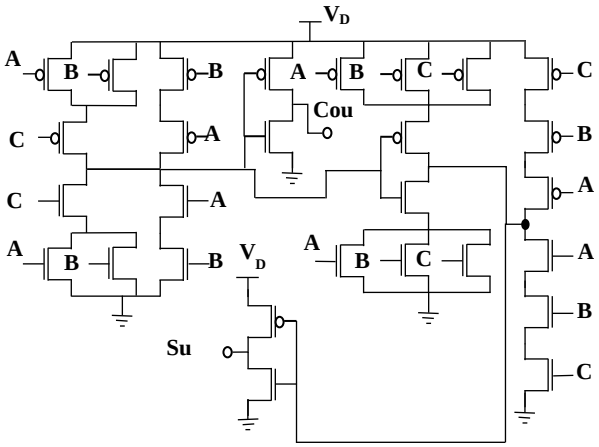

Figure.9. Full Adder circuit implemented in CMOS Logic

E. Sum output of full adder implemented in SCL

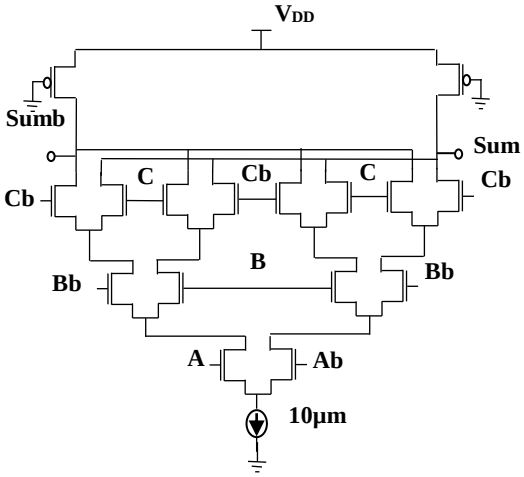

Figure.10. full adder implemented in SCL

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F. Carry output of full adder implemented in SCL

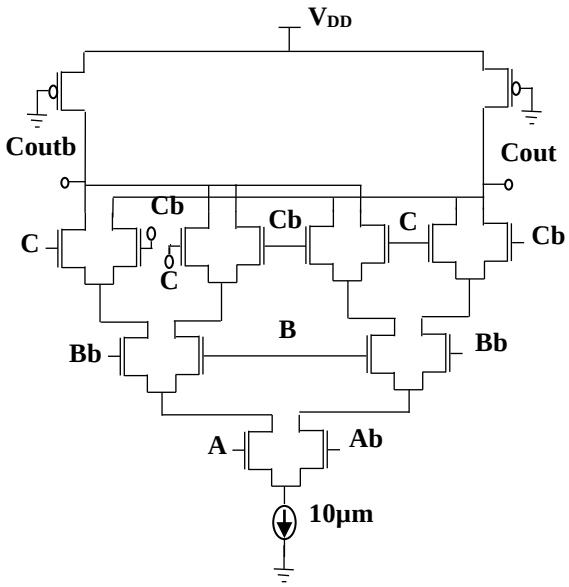

Figure.11. Carry output of full adder implemented in SCL

G. Sum output of full adder implemented in SCL (Minimized using MUX-MIN method)

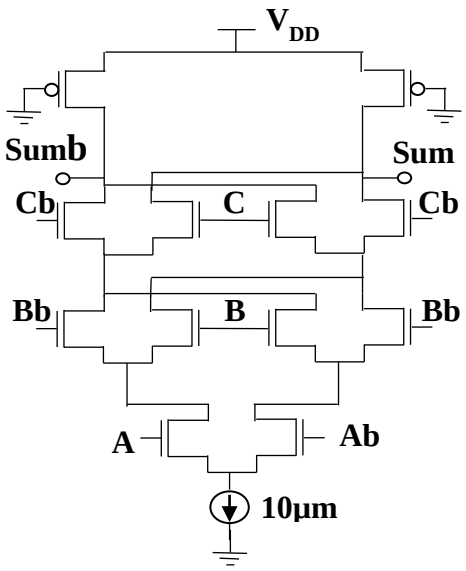

Figure.12

H. Carry output of full adder implemented in SCL (Minimized using MUX-MIN method).

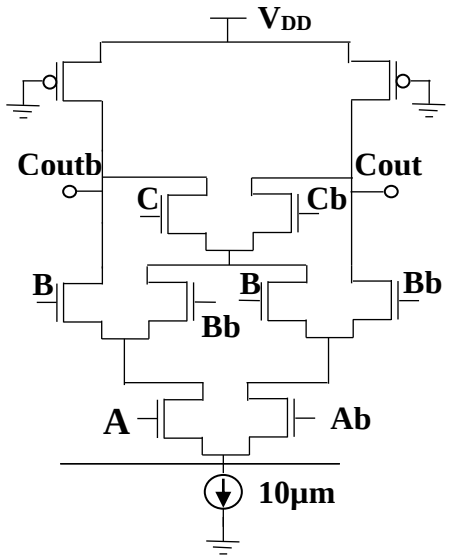

Figure.13. Carry output of full adder implemented in SCL

I. Proposed Modified SCL-Gated full adder circuit

SCL-Gated full adder circuit incorporate 6 more NMOS and its stops the flow of bias current throw the circuit for the time duration when the output of the circuit is not changing. This full adder circuit is shown in Figure .14.Aspect ratio (W/L) for PMOS and NMOS taken to be (1/6) and (3/2) respectively. Out of the 6 extra transistors used in SCL-Gated FA, transistors M1 and M2 are used to stop the flow of current in Sum and Carry circuits respectively.

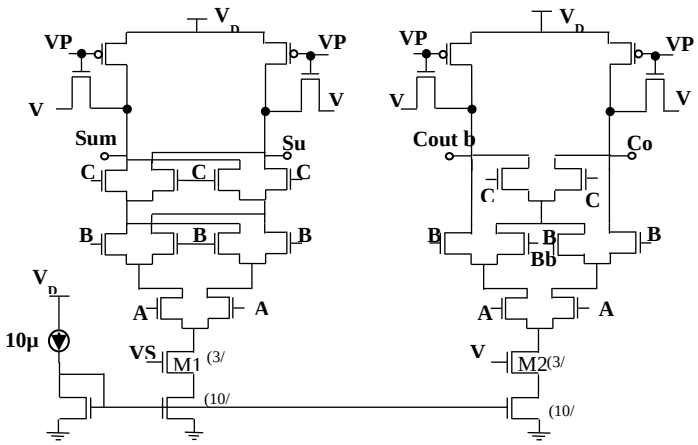

Figure.14. Proposed Modified SCL-Gated full adder circuit

X. RESULTS AND DISCUSSION

In the present dissertation work, different full adder circuits have been designed. Their performance has been analyzed in terms of power (P), delay (D), power delay

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product (PDP), and number of transistors (N), current spike (I_S), power-delay-number of transistors-current spike-product ($PDNI_SP$) and output voltage swing (V_{SWING}). In order to study the effect of process corners on different parameters, full adder circuits have also been analyzed at 180nm, 130nm, 90nm and 45nm technology nodes using Tanner EDA tool.

A. Power Consumption Of Full Adder Circuits At Different Technology Nodes

Technology Node / Type of Full Adder Design	180nm	130nm	90nm	45nm
	Power (µW)			
SERF [13]	***6.38***	***1.87***	***2.11***	***0.78***
SERF-Imp [13]	26.97	4.96	5.09	2.05
PTL [14]	15.95	4.56	4.88	1.87
CMOS [29]	18.45	4.39	3.41	1.32
SCL [3]	36.0	24.0	14.4	8
SCL-Min [3]	36.0	24.0	14.4	8
SCL-Gated	22.84	19.7	11.9	6.24

B. Delay Of Full Adder Circuits At Different Technology Nodes

Technology Node / Type of Full Adder Design	180nm	130nm	90nm	45nm
	Delay (ps)			
SERF [13]	***139.96***	114.96	***86.83***	***147.52***
SERF-Imp [13]	263.41	187.96	139.97	208.08
PTL [14]	252.25	189.02	143.74	166.41
CMOS [29]	431.88	230.69	189.33	263.12
SCL [3]	397.08	153.22	179.46	252.76
SCL-Min [3]	238.19	96.62	167.19	238.56
SCL-Gated	319.79	***106.88***	183.44	275.99

C. Power Delay Product Of Full Adder Circuits At Different Technology Nodes

Technology Node / Type of Full Adder Design	180nm	130nm	90nm	45nm
	PDP (fJ)			
SERF [13]	***0.89***	***0.21***	***0.18***	***0.11***
SERF-Imp [13]	7.1	0.93	0.71	0.42
PTL [14]	4.02	0.86	0.70	0.31
CMOS [29]	7.97	1.01	0.64	0.34
SCL [3]	14.3	3.67	2.58	2.02
SCL-Min [3]	8.58	2.31	2.40	1.90
SCL-Gated	7.3	2.11	2.18	1.72

D. Number Of Transistors Of Full Adder Circuits At Different Technology Nodes

Technology Node / Type of Full Adder Design	180nm	130nm	90nm	45nm
	No. of Transistors (PMOS/NMOS)			
SERF [13]	***(5/5) 10***	***(5/5) 10***	***(5/5) 10***	***(5/5) 10***
SERF-Imp [13]	(7/7) 14	(7/7) 14	(7/7) 14	(7/7) 14
PTL [14]	(7/7) 14	(7/7) 14	(7/7) 14	(7/7) 14
CMOS [29]	(14/14) 28	(14/14) 28	(14/14) 28	(14/14) 28
SCL [3]	(4/28) 32	(4/28) 32	(4/28) 32	(4/28) 32
SCL-Min [3]	(4/18) 22	(4/18) 22	(4/18) 22	(4/18) 22
SCL-Gated	(4/24) 28	(4/24) 28	(4/24) 28	(4/24) 28

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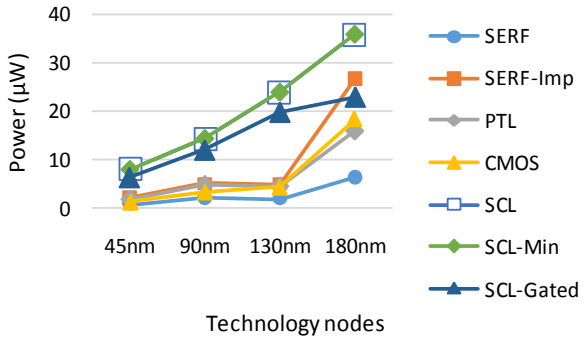
E. Current Spikes Of Full Adder Circuits At Different Technology Nodes

Technology Node / Type of Full Adder Design	180nm	130nm	90nm	45nm
	Current Spike (µA)			
SERF [13]	125.87	63.54	71.00	40.28
SERF-Imp [13]	234.20	116.61	130.97	56.85
PTL [14]	297.39	153.93	178.55	78.28
CMOS [29]	192.93	107.93	112.15	44.47
SCL [3]	***20.0***	***16.0***	***12.0***	***8.0***
SCL-Min [3]	***20.0***	***16.0***	***12.0***	***8.0***
SCL-Gated	***20.0***	***16.0***	***12.0***	***8.0***

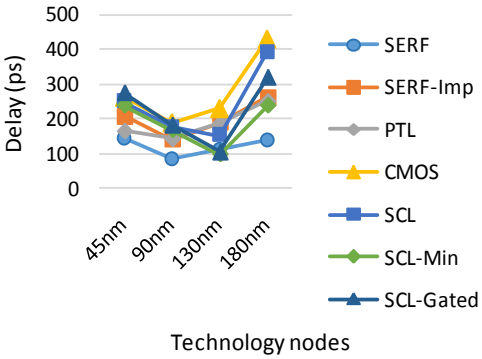
F. Voltage Swings Of Full Adder Circuits At Different Technology

Technology Node / Type of Full Adder Design	180nm (V_{DD}=1.8V)	130nm (V_{DD}=1.5V)	90nm (V_{DD}=1.2V)	45nm (V_{DD}=1V)
	Voltage Swing (V)			
SERF [13]	50.56%	37.77%	50.83%	40.00 %
SERF-Imp [13]	78.89%	86.67%	81.67%	78.00 %
PTL [14]	73.33%	69.33%	65.83%	62.00 %
CMOS [29]	***100%***	***100%***	***100%***	***100%***
SCL [3]	***100%***	***100%***	***100%***	***100%***
SCL-Min [3]	***100%***	***100%***	***100%***	***100%***
SCL-Gated	***100%***	***100%***	***100%***	***100%***

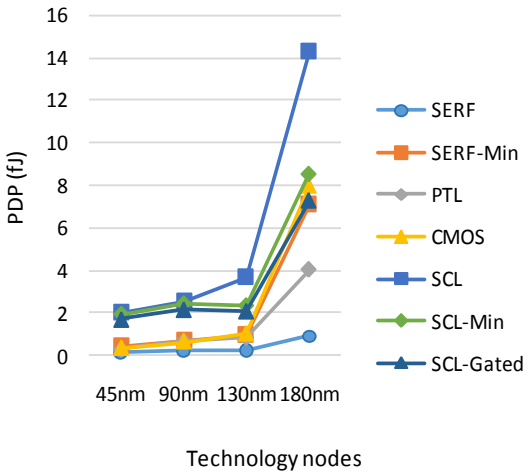
G. Effect of technology scaling on Performance Parameters of different Full Adder Circuits



Power of full adder circuits at different technology nodes



Delay of full adder circuits at different technology nodes



PDP of full adder circuits at different technology nodes.

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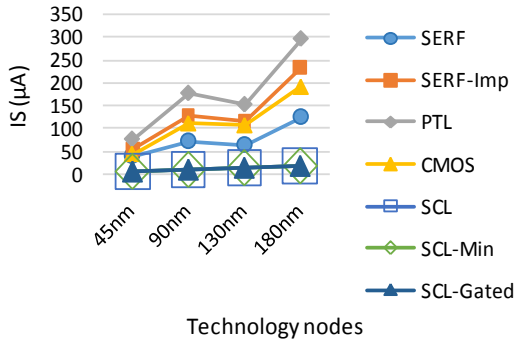
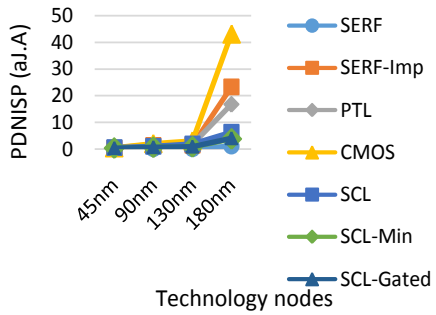


Current spike of full adder circuits at different technology no.



PDNI$_S$P of full adder circuits at different technology nodes

XI. CONCLUSIONS

From the literature review it is observed that power reduction in the source-coupled logic (SCL) circuits is important area of research. The study of various types of full adder circuits, SCL circuits, SCL families, SCL minimization techniques has been carried out. The performance analysis of the full adder circuits is performed. A new SCL full adder circuit has been proposed in this literature which improves the power of the circuit but at the cost of area and delay. The analysis is carried out for 180nm, 130nm, 90nm and 45nm technologies. The PDNI$_S$P reduces with technology but the delay increases.

SCL full adder circuit with bias current gating (SCL-Gated) shows reduction in power dissipation by stopping the flow of current in the circuit when the inputs to the full adder circuit is not changing. But this reduction in power is at the cost of delay and area

Source-coupled logic full adder circuits provide constant value of current spike and small value of PDNI$_S$P which makes these circuits suitable for application in mixed-mode designs. SCL-Gated full adder circuit in addition to previously described features provides some extra reduction in power which will make SCL-Gated circuit even more appropriate for mixed mode applications.

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