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Analysis of Modified Asymmetrical Twenty One level Inverter for Standalone PV Applications using Different Multicarrier PWM Techniques

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***Abstract*- As the power demand is increasing continuously, the use of non-conventional energy sources is increasing rapidly. Among the different non conventional energy sources, solar energy is finding more application. The solar energy is converted in to electricity which is DC in nature by using the PV modules. In order to convert from DC to AC Multilevel inverters are used. As the voltage level increases the THD decreases in MLI. In this paper an asymmetrical multilevel inverter which has four main switches and one H-bridge has been implemented. With this circuit we are generating 21 level of output voltage with reduced THD which can be used for standalone PV application. This topology uses less number of power switches and diodes as compared to other conventional MLI. For controlling the output voltage of this topology multi-carrier different PWM techniques are used. And the results of different PWM techniques are compared for different modulation index and FFT analysis is done by using the MATLAB SIMULINK software.**

Keywords: *Multi-level inverter (MLI), pulse width modulation (PWM), Total harmonic distortion (THD), Phase disposition (PD), Phase opposition disposition (POD), Variable frequency (VF).*

I. INTRODUCTION

The use of multilevel inverter in industry is increasing from last few decades due to its high power and voltage application. The important characteristics of MLI is less THD and less dv/dt stress. In case of Multilevel inverter as the number of switches increases the number of steps also increases and the output voltage obtained will be nearly sinusoidal in nature and the THD obtained will be less. Among renewable energy source solar energy is most commonly used as it is available in nature for free of cost and abundant in nature. The energy which is obtained from the solar panel is DC in nature. In order to convert it from DC to AC multilevel inverters are used.MLI are divided as symmetrical and asymmetrical in case of symmetrical MLI the value of all the voltage sources will be equal and in case of asymmetrical MLI all the DC sources will be having unequal value. The conventional MLI are classified in to three types diode clamped inverter, flying capacitor inverter, cascaded H-bridge multilevel inverter. Another name given to Diode clamped multilevel inverter is neutral point clamped multilevel inverter [4-6]. In this paper a new asymmetrical MLI has been implemented by using four main switches and one H-bridge and four voltage sources which has unequal voltage values. For controlling of the output voltage of the MLI different techniques are used among them few of them are Selective Harmonic elimination ,Fundamental switching frequency , space vector modulation technique ,High switching frequency and Multi-Carrier PWM techniques. In this paper different Multi-Carrier PWM techniques are used for controlling the output voltage of the 21-level asymmetrical MLI. This new topology uses less number of power switches for more number of output voltage level as compared to other conventional MLI therefore the THD obtained will be less.

II. MULTILEVEL INVERTER TOPOLOGIES

A. Conventional Topologies

- Diode-clamped MLI

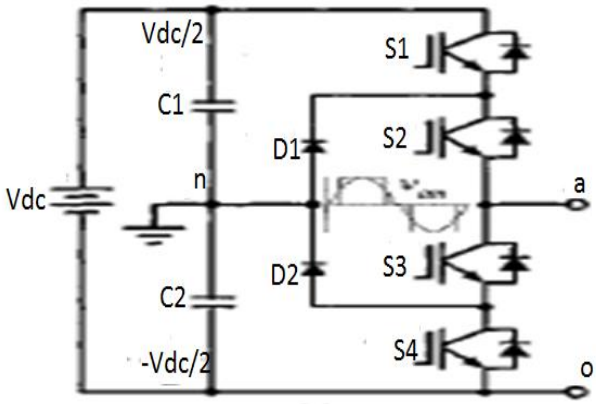

Fig (a)

Another name which is given to Diode-clamped MLI is neutral-point clamped inverter and was first introduced by Nabae.Takahashi,and Akagi in 1981 . And basically it was a three level inverter[1]. In this circuit diode D1 and D2 is used to clamp the switch voltage to half the level of dc-bus voltage and the input voltage is divided in to two parts[14].The output voltage obtained is +Vdc/2 when switch S1 and S2 are turned on and –Vdc/2 by turning on the switch S3 and S4 and for zero level S2 and S3 are turned on. Therefore the number of diodes required is given as

$$N=(M-1)*(M-2)$$

N=number of diodes used

M=number of levels at inverter output

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- Flying-capacitor MLI:-

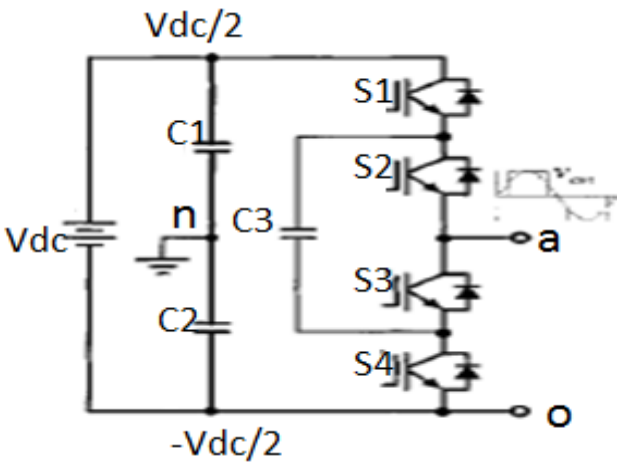

Fig (b)

Flying-capacitor MLI was first introduced by Maynard and Foch in 1992 [1]. The fig (b) shows the three level capacitor clamped inverter. The capacitor C1 and C2 is used to clamp the switch voltage to half the level of dc- bus voltage. The output voltage V_{an} has three voltage levels and they are$+V_{dc}/2$, $-V_{dc}/2$, 0 [14]. For $+V_{dc}/2$ The Switches S1 and S2 will be turned on for $-V_{dc}/2$ switches S3 and S4 will be turned on and for 0 level either pair ($S1\ S3$)or ($S2\ S4$) can be turned on. The numbers of capacitors used in this circuit are

N= ((M-1)*(M-2))/2

Where

N= number of capacitors
M= number of levels at inverter output
In addition to these capacitors $(M-1)$ main dc bus capacitors are also required.

- Cascaded H-bridge MLI

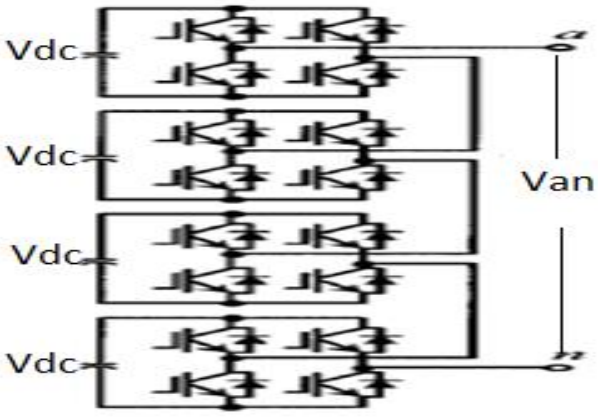

Fig (c)

Four cascaded H-bridge multilevel inverter topology for *N* level inverter is shown in fig(c). The output level and number of H-Bridges required are related by the equation,

M= (2N+1)

Where,

N= number of H-bridges
M= number of levels at inverter output

If there is increment in the output levels, then the waveform becomes more sinusoidal and % THD content decreases. This will increase the quality of the output signal. On the other hand, with the increment in the output levels, the number of H-Bridges required also increases and these results in more number of switches. Hence, the complexity of the switching circuit increases. Further, rise in number of switches leads to higher switching losses, decrement in the efficiency.

III. PROPOSED TOPOLOGY

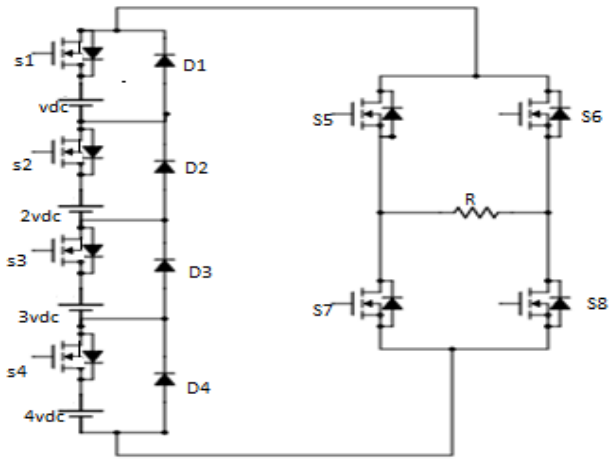

Fig (d)

The proposed asymmetrical multilevel inverter is depicted in fig (d). 21 level asymmetrical MLI uses four main diodes D1,D2,D3,D4 four main switches S1, S2, S3, S4 and one H-bridge. It has four separate dc source for 21-level MLI. By increasing the main switches and voltage source the number of voltage levels can be increased. In this asymmetrical MLI voltage sources will have unequal value. The proposed 21-level MLI can operates in different modes of operation and the switching sequence of the asymmetrical multilevel inverter is as shown in table-I.

In H-bridge four switches are used for its operation these are S5, S6, S7, S8 in which one pair of switches i.e switch S5 and S8 works for positive half-cycle and other pair of switches S6,and S7 works for negative half-cycle. In this topology four separate dc sources are used they are "Vdc","2Vdc","3Vdc","4Vdc" having voltages of 31.5V, 63V, 94.5V, 126V each respectively. There are twenty one switching modes of operation for this topology in order to generate the output voltage of 21 level and the operating modes for positive half cycle are explained in modes of operation concept

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SWITCHING TABLE- I

Voltage level	S1	S2	S3	S4	S5	S6	S7	S8	Output Voltage (V)
10	1	1	1	1	1	0	0	1	10Vdc
9	0	1	1	1	1	0	0	1	9Vdc
8	1	0	1	1	1	0	0	1	8Vdc
7	0	0	1	1	1	0	0	1	7Vdc
6	0	1	0	1	1	0	0	1	6Vdc
5	1	0	0	1	1	0	0	1	5Vdc
4	0	0	0	1	1	0	0	1	4Vdc
3	0	0	1	0	1	0	0	1	3Vdc
2	0	1	0	0	1	0	0	1	2Vdc
1	1	0	0	0	1	0	0	1	Vdc
0	0	0	0	0	1	1	0	0	0
-1	1	0	0	0	0	1	1	0	-Vdc
-2	0	1	0	0	0	1	1	0	-2Vdc
-3	0	0	1	0	0	1	1	0	-3Vdc
-4	0	0	0	1	0	1	1	0	-4Vdc
-5	1	0	0	1	0	1	1	0	-5Vdc
-6	0	1	0	1	0	1	1	0	-6Vdc
-7	0	0	1	1	0	1	1	0	-7Vdc
-8	1	0	1	1	0	1	1	0	-8Vdc
-9	0	1	1	1	0	1	1	0	-9Vdc
-10	1	1	1	1	0	1	1	0	-10Vdc

IV. MODES OF OPERATION

Mode (1&2): In mode 1 operation switches S1, S5 and S8 are conducting and diode D2, D3, D4 are forward-biased with diode D1is reverse biased in order to get the output voltage of "Vdc". The operating mode is shown in fig (e). In mode 2 operation switches S2,S5 and S8 are conducting and diode D1,D4,D3 are forward –biased with diode D2 is reverse biased in order to get the output voltage of "2Vdc" which is as shown in fig (f).

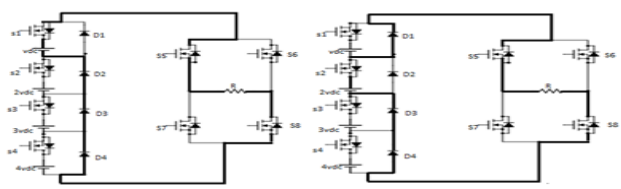

Fig (e) Fig (f)

Mode (3&4): In mode 3 operation switches S3, S5 and S8 are conducting and diode D1, D2, D4 are forward-biased with diode D3 is reverse-biased in order to get the output voltage of "3Vdc" which is as shown in fig (g). In mode 4 operation switches S4, S5, S8 are conducting and diode D1, D2, D3 are forward – biased with diode D4 reverse biased in order to get the output voltage of "4Vdc". This is shown in fig (h).

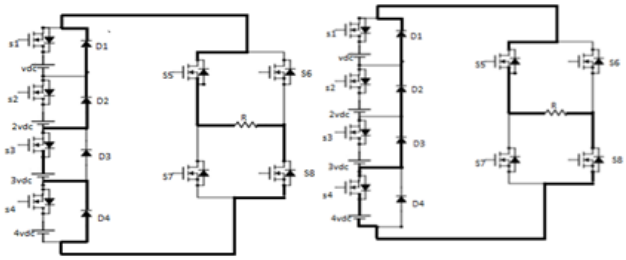

Fig (g) Fig (h)

Mode (5 &6): In mode 5 operation switches S1, S4, S5 and S8 are conducting and diode D2, D3 are forward biased with D1, D4 are reverse biased in order to get the output voltage of "5Vdc" which is as shown in fig(i). In mode 6 operation switches S2, S4, S5 and S8 are conducting and diode D1 and D3 are forward biased with diode D4 and D2 are reverse biased in order to get the output voltage of "6Vdc". This is as shown in fig (j).

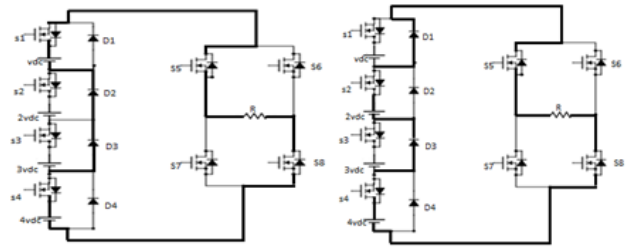

Fig (i) Fig (j)

Mode(7&8): In mode 7 operation switches S3 S4, S5 and S8 are conducting and diode D1, D2 are forward biased with diode D3 and D4 are reverse biased in order to get the output voltage of "7Vdc" which is as shown in fig (k). working as reverse biased. In operating mode 8 switches S1, S3, S4, S5 and S8 are conducting and diode D2 as forward biased with diode D1, D3, D4 are reverse biased in order to get the output voltage of "8Vdc" which is as shown in fig (l).

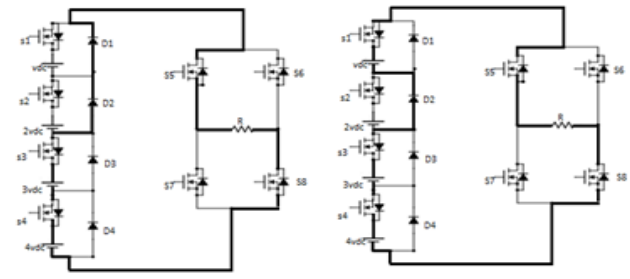

Fig (k) Fig (l)

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Mode(9&10): In mode 9 operation switches S2, S3, S4, S5 and S8 are conducting and diode D1 as forward biased with diode D2, D3, D4 are reverse biased in order to get the output voltage of "9Vdc" which is as shown in fig (m). In mode 10 operation switches S1, S2, S3, S4, S5 and S8 are conducting with all the diodes are reverse biased in order to get the output voltage of "10Vdc" which is as shown in fig (n).

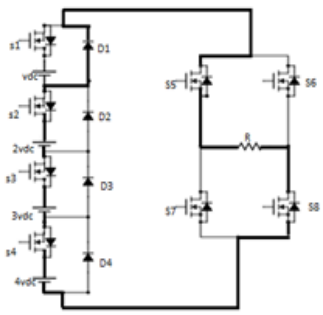

Fig (m)

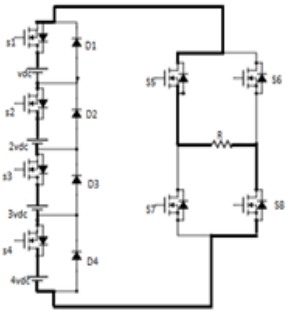

Fig (n)

Mode 11: When switch S5, S6or S7, S8 are conducting the obtained output voltage is "zero" for zero level. The operating mode is as shown in fig (o).

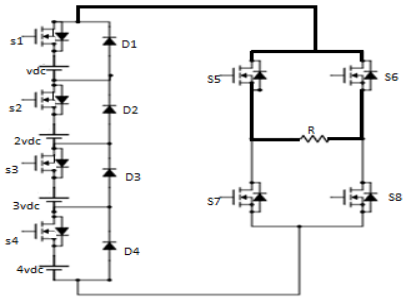

Fig (o)

Similarly For the conduction of the negative half cycle switch S6 and S7 are turned on in the H-bridge instead of S5 and S8.

V. CONTROL AND MODULATION TECHNIQUE OF MULTILEVEL INVERTER USING DIFFERENT PWM TECHNIQUE

Multicarrier sinusoidal pulse width modulation technique is based on the comparison of sinusoidal reference wave with vertically shifted carrier signals. For N-level output we have to use N-1 carrier signals. And these carrier signals have the same amplitude Ac and same frequency fc and the frequency can be chosen in the range of 1Kz – 5Kz. And the sinusoidal reference wave frequency to be chosen as 50Hz and it is denoted as fr and amplitude of the reference wave is given as Ar [7-13]. As the value of modulation index increases THD decreases up to modulation index value of 1. If the value of modulation index value decreases THD increases. In multilevel inverters the amplitude modulation index Ma and frequency modulation index Mf are defined as follows,

$$Mf=fc/fr$$

$$Ma=Ar/(N-1)*Ac$$

The principle operation of multicarrier PWM technique is implemented using several carrier wave with one sinusoidal wave as modulating waveform. In MATLAB SIMULINK carrier waves are generated by using the repeating sequence block with a frequency of 2kHz. Output of the repeating sequence and sine wave block are given to mux in order to get carrier wave arrangement for PD,POD,and VF techniques which are as shown in below Fig(1) ,Fig(2), and Fig(3) respectively. The frequency chosen for a sinusoidal waveform is 50Hz and it is placed at the center of the carrier wave arrangement.

Different types of PWM techniques are used for controlling output voltage. In this paper we are using three different techniques which are explained below,

A. Phase disposition pulse width modulation

In this technique the carrier wave above the zero reference and below the zero reference are in phase therefore this technique is called as phase disposition pulse width modulation technique. The reference wave is continuously compared with each of the carrier wave, if the amplitude of the reference is greater than the carrier then the pulse will generated. By using these pulses the gate pulses which are required for asymmetrical multilevel inverter are generated. The carrier arrangement for this technique is shown in fig (p)

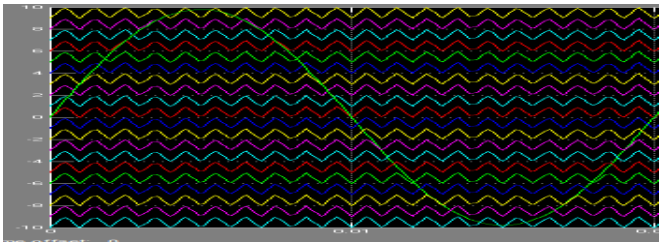

Fig (p). Carrier wave arrangement for PD PWM technique

B. Phase opposition disposition pulse width modulation

In this technique the carrier wave above the zero reference and below the zero reference are in phase opposition by 180 therefore this technique is called as phase apposition disposition pulse width modulation technique. The reference wave is continuously compared with each of the carrier wave, if the amplitude of the reference is greater than the carrier then the pulse will be generated. By using these pulses the gate pulses which are required for asymmetrical multilevel inverter are generated This is as shown in fig (q).

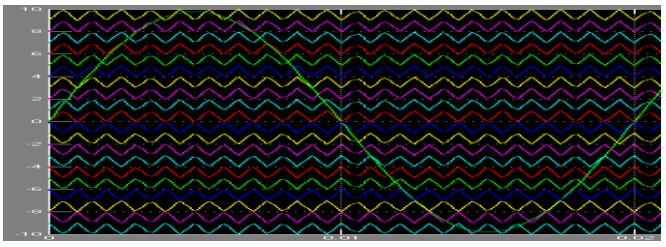

Fig (q):- Carrier wave arrangement for POD PWM technique

C. Variable Frequency pulse width modulation Technique

In this technique all the carrier wave which are above the zero reference and below the zero reference have the variable frequency with each other. The reference wave is continuously compared with each of the carrier wave, if the amplitude of the reference is greater than the carrier then the pulse will generated. By using these pulses the gate pulses which are required for asymmetrical multilevel inverter are generated. The carrier arrangement for this technique is shown in Fig(r)

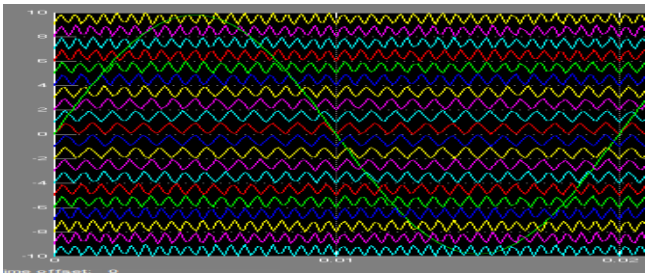

Fig (r) . Carrier wave arrangement for VF PWM technique

VI. SIMULINK MODEL

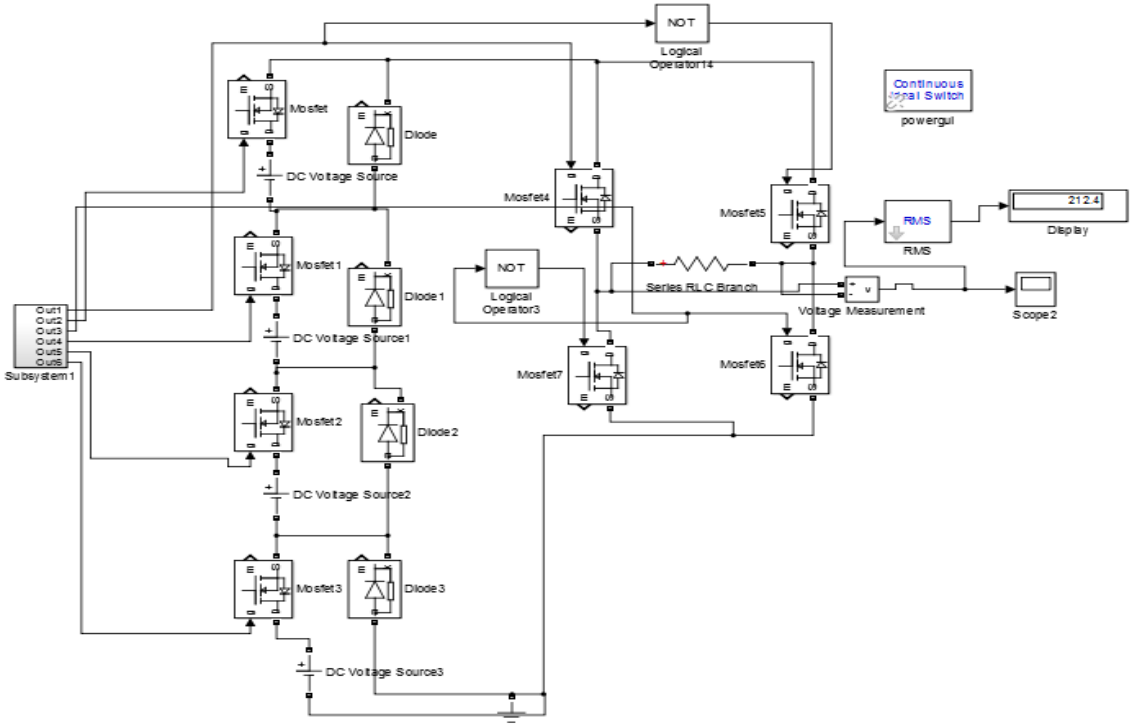

Fig (s)

VI. SIMULATION RESULT

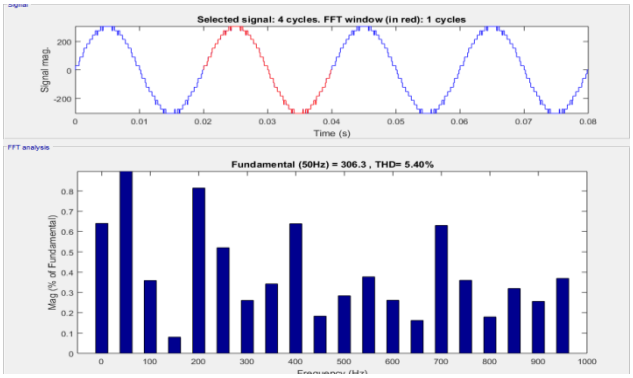

Fig (t) FFT analysis by PDPWM (Ma= 1,Mf= 20)

The fig(t) shows the output voltage waveform and harmonic analysis which is obtained for a amplitude modulation index of 1 and frequency modulation index of 20 for phase disposition PWM technique.

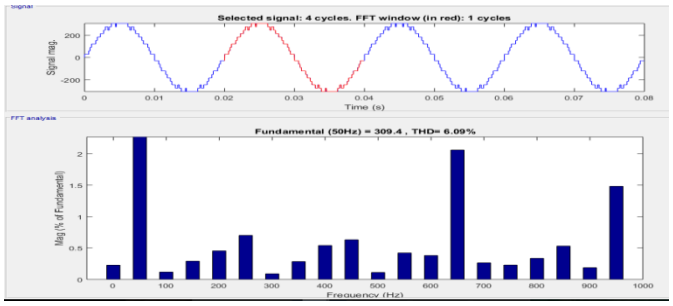

Fig (u) FFT analysis by PODPWM (Ma=1 , Mf=20)

The fig(u) shows the output voltage waveform and harmonic analysis which is obtained for a amplitude modulation index of 1 and frequency modulation index of 20 for phase opposition disposition PWM technique.

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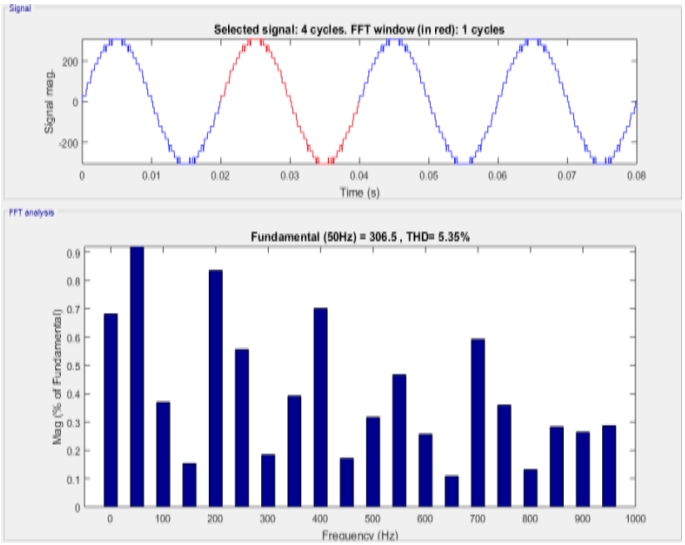

Fig (v) FFT analysis by VFPWM (Ma=1, Mf=20)

The fig(v) shows the output voltage waveform and harmonic analysis which is obtained for a amplitude modulation index of 1 and frequency modulation index of 20 for variable frequency PWM technique.

TABLE-I. Comparison between different multilevel inverter topologies

Inverter topologies	**CHB MLI**	**NPC MLI**	**Flying Capacitor**	**Proposed topology**
Number of switches	40	40	40	8
Number of diodes	0	0	0	4
Clamping diode	0	380	0	0
DC bus Capacitor	0	20	20	0
Flying capacitor	0	0	190	0
DC source	10	1	1	4

From table -1 it is seen that the number of switching devices used in this proposed topology are less compared to conventional H-bridge MLI. Due to this complexity of the proposed topology is reduced. In this proposed topology the number of clamping capacitors and flying capacitors are not used like as that of neutral clamped and flying capacitor multilevel inverter. The number of DC sources used in this topology are also less. Because of these reasons complexity of the system reduces and switching losses can be reduced and hence the system efficiency can be improved**.**

TABLE-2. THD analysis between different PWM technique for 21- level MLI

PWM Technique	Modulation index			
	1	0.9	0.8	0.7
PD PWM % THD	5.40	5.86	6.80	8.01
POD PWM % THD	6.09	6.15	6.97	8.06
VF PWM % THD	5.35	6.11	6.67	7.73

From table-II it is seen that THD Analysis for Twenty-one level MLI is carried out for PD ,POD and for VF PWM technique. From the above table it is clear that as the modulation index value starts to decrease from 1to0.7 THD increases.In all the above explained techniques it is possible to get the less THD for a modulation index value of 1.

VII. CONCLUSION

In this paper a 21-level asymmetrical multi level inverter topology is proposed with different Multi carrier PWM technique. In order to realize the 21 level MLI twenty multicarrier waves are used for PD,POD and VF PWM technique. And the results of the different PWM techniques are compared. From this different multicarrier PWM technique variable frequency PWM technique is giving the less THD compared to other methods. And from this simulation result it is seen that the THD of the system reduces with increase in modulation index value i.e from 0.7 to 1.As per the IEEE standard THD of 5.35% is obtained for variable frequency PWM technique for amplitude modulation index value of 1. By using this proposed topology efficiency of the system is improved as compared to other conventional multilevel inverter as the number of switching devices used in this proposed topology are very less and hence the efficiency of this topology is improved.

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