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MLI using POD Technique and Comparison of THD for Different Levels

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***Abstract* :- Recent day's Multi Level inverters are extensively used due to their increased power handling capability, reduced harmonic distortion or content, less prone to electromagnetic interference and low switching losses. The different multilevel inverter topologies have drawn significant interest in power industries because it can provide high power for the higher power application. The paper deals with implementation of single phase 5 Level inverter using POD PWM technique. The proposed technique for MLI able to generate 5 level output with reduced components as compared conventional topology. POD technique is a Level Shifted scheme where single carrier wave and two sinusoidal waves are used for pulse generation, which is applied to cascaded H-bridge multilevel inverter. The entire work is designed and implemented using software tool MATLAB/Simulink and complete THD analysis is done.**

***Keywords* —** *Electromagnetic Interference, PD, APOD and POD technique, PWM, Multilevel Inverter.*

I. INTRODUCTION

The voltage source or Current source inverters produce an output voltage or current with levels of 0 or $\pm V_{dc,}$ these are called as two level inverters. To obtain minimum distortion, less ripple content and high quality output voltage or current waveform inverters require high switching frequency along with various types of pulse width modulation techniques. The two level inverters cannot be used for high voltage and high power applications because of their switching losses and limitations in operating frequency. In order to overcome the issues associated with two level inverters [1], concept of multi level inverter was introduced. As the levels of the output voltage or current waveform increases the ripple content and the distortions in the signal will reduce significantly.

Now day's multilevel inverters has drawn very much importance in the field of power electronics, due to their higher power handling capability, efficiency and reduced switching losses [5-8]. Different topologies exist for Multi Level Inverters other than the conventional topologies which makes ease in operation of the circuit with reduced number of components. The inverters must fulfill the following requirements.

- Generation of pure sinusoidal output wave.
- Output current should contain low THD.
- Less prone to Electromagnetic Interference.

The multi Level Inverters are mainly classified into three types

- Diode Clamped MLI
- Flying Capacitor type MLI.
- Cascaded H Bridge type MLI.

A. Diode Clamped Multilevel Inverter

A diode clamped multilevel inverter consists of *(m*-1) capacitors on the input side and produce *m* levels of output voltage. The voltage across each capacitor is given by V_{dc}/ (*m*-1). An *m* level inverter requires 2**(m*-1) switching devices and *(m*-1)*(*m*-2) clamping diodes. The main features of diode clamped inverter are they have high voltage rating for blocking diodes, unequal switching devices rating, overcome capacitor voltage unbalance. The major advantages of Diode clamped inverters are; high efficiency because, all the devices are turned at fundamental frequency. Harmonic content is low enough to avoid need for filters and simple control method. Disadvantage are as the levels of voltage increases clamping diodes required will be more and control of reactive power flow becomes difficult for individual converter.

B. Flying Capacitor Multilevel Inverter

Another topology of multilevel inverter is Flying Capacitor Multilevel Inverter. It is also well known as Imprecated Cell Inverter. They are called Flying Capacitor Multilevel Inverter, because the capacitors float with respect to earth's potential. It is similar to diode clamped multilevel inverter. This type of multilevel inverter requires capacitor to be pre-charged. Main features of flying capacitor multilevel inverter are they have large number of capacitors and balancing of capacitor voltages. The main advantages of flying capacitor multilevel inverter are both real and reactive power can be controlled and provide switch combination redundancy for balancing different voltage levels. Disadvantages are excessive storage capacitors are required as the level increases and switching frequency, switching losses are high for real power transmission.

C. Cascaded Multilevel Inverter

The inverter consists of series of H-bridge inverter units of single phase, full bridge. This type of inverter uses separate DC sources to generate desired voltage, which may be obtained from solar cell, fuel cell, or batteries. Cascaded multilevel inverters does not require any voltage balancing

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capacitors and voltage clamping diodes unlike in diode clamped and flying capacitor multilevel inverter. Features of cascaded multilevel inverter are for rectification and inversion of power requires separate DC sources and back to back connection of DC sources is not possible. The advantages of cascaded multilevel inverter is that it requires less number of components as compared to diode and flying capacitor multilevel inverters, optimized circuit layout and smart switching methods are available to minimize device stresses and losses. Major disadvantage is that it requires separate DC sources for real power transmission limiting its applications.

II. PROPOSED MULTI-LEVEL INVERTER

A. Topology of Multi-Level Inverter

As shown in Fig. 2, the proposed MLI is composed of two dc-link capacitors (C_1, C_2) and four switching devices (T_A^+, T_A^-, T_B^+, T_B^-) comprising a H-bridge, and four active switches (T_P^+, T_P^-, T_N^+, T_N^-) located between dc-link and H-bridge. The voltage across the switching devices in the dc-link (T_P^+, T_P^-, T_N^+, T_N^-) is $V_{DC}/2$ and operated at a switching frequency. Whereas, voltage across the switching devices in the H-bridge (T_A^+, T_A^-, T_B^+, T_B^-) is V_{DC} and the switches (T_A^+, T_A^-, T_B^+, T_B^-) are switched at a frequency of the fundamental component of the output voltage (e.g. 50 or 60 Hz).

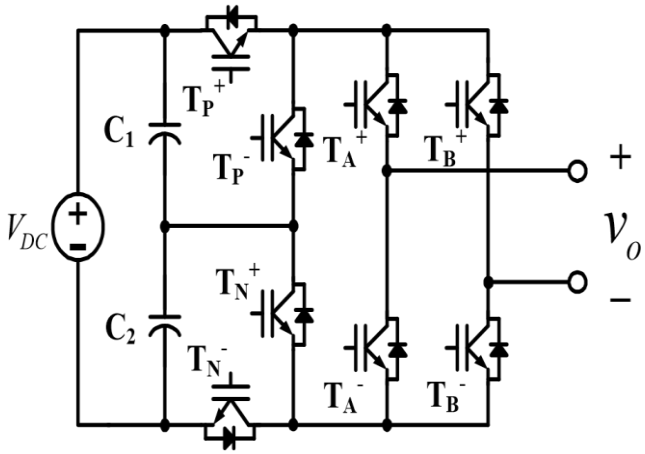

Fig. 1 Proposed single-phase 5-level inverter topology.

TABLE I
Output voltage according to switching states

Output Voltage	Switching Conditions							
	T_p^+	T_p^-	T_n^+	T_n^-	T_a^+	T_b^-	T_a^-	T_b^+
V_{dc}	ON	OFF	OFF	ON	ON	ON	OFF	OFF
$V_{dc}/2$	OFF	ON	OFF	ON	ON	ON	OFF	OFF
$V_{dc}/2$	ON	OFF	ON	OFF	ON	ON	OFF	OFF
0	OFF	ON	ON	OFF	ON	ON	OFF	OFF
0	OFF	ON	ON	OFF	OFF	OFF	ON	ON
$-V_{dc}/2$	OFF	ON	OFF	ON	OFF	OFF	ON	ON
$-V_{dc}/2$	ON	OFF	ON	OFF	OFF	OFF	ON	ON
$-V_{dc}$	ON	OFF	OFF	ON	OFF	OFF	ON	ON

Thus, the dc-link switches (T_P^+, T_P^-, T_N^+, T_N^-) and the H-bridge switches (T_A^+, T_A^-, T_B^+, T_B^-) can be strategically selected based on the rated power of the inverter system in order to reduce system cost and increase efficiency. Table I shows the output voltage according to the switching states.

A. Proposed PWM strategy

The output voltage of the proposed MLI shown in Fig. 2 has five levels (V_{DC}, $V_{DC}/2$, 0, $-V_{DC}/2$, $-V_{DC}$) according to the switching states of the inverter. There are four operation modes depending on the instantaneous value of the reference voltage, *V*ref and the maximum value of the carrier signal, V_C. Table I shows the possible inverter output voltage level.

In case of the N-level NPC type multi-level inverter, triangular carrier signals with the same frequency and amplitude are used so that they fully occupy contiguous bands over the range $+V_{DC}$ to $-V_{DC}$. A single sinusoidal reference is compared with each carrier signal to determine the output voltage for the inverter. Three dispositions of the carrier signal are considered to generate the PWM signal [9-11].

1) Phase disposition (PD); where all carriers are in phase.

2) Alternative phase opposition disposition (APOD); where each carrier is phase shifted by 180 degree from its adjacent carrier.

3) Phase opposition disposition (POD); where the carriers above zero voltage are 180 degree out of phase with those below zero voltage.

The PD, POD, APOD techniques are also known as level shifted techniques. In this paper we have used phase opposition disposition method for generating pulses to the switches. Conventional method uses single carrier signals for generating pulses to each switch but POD technique uses single carrier wave for generating pulses to switches. So this makes circuit operation simple and reduces the complexity.

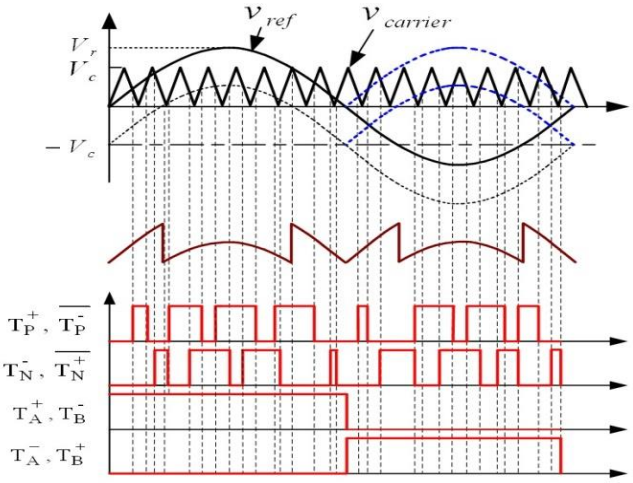

Fig. 2. PWM strategy based on POD with single carrier signal

ISSN No: - 2456 - 2165

A new PWM strategy based on POD modulation which requires only a single carrier signal (*V*carrier) is proposed and the detailed PWM strategy is depicted in Fig. 2. If the reference signal is positive, then the switch pair (T_A^+, T_B^-) are turned on, and if it is negative, then the switch pair (T_A^-, T_B^+) are turned on. Thus the switches composing the H bridge inverter turned on and turned off once during the period of the reference signal. The voltage across the switch at blocking state is V_{DC}. The switches (T_P^-, T_N^+) are operated complementally to the switches (T_P^+, T_N^-).

III. SIMULATION AND EXPERIMENTAL RESULTS

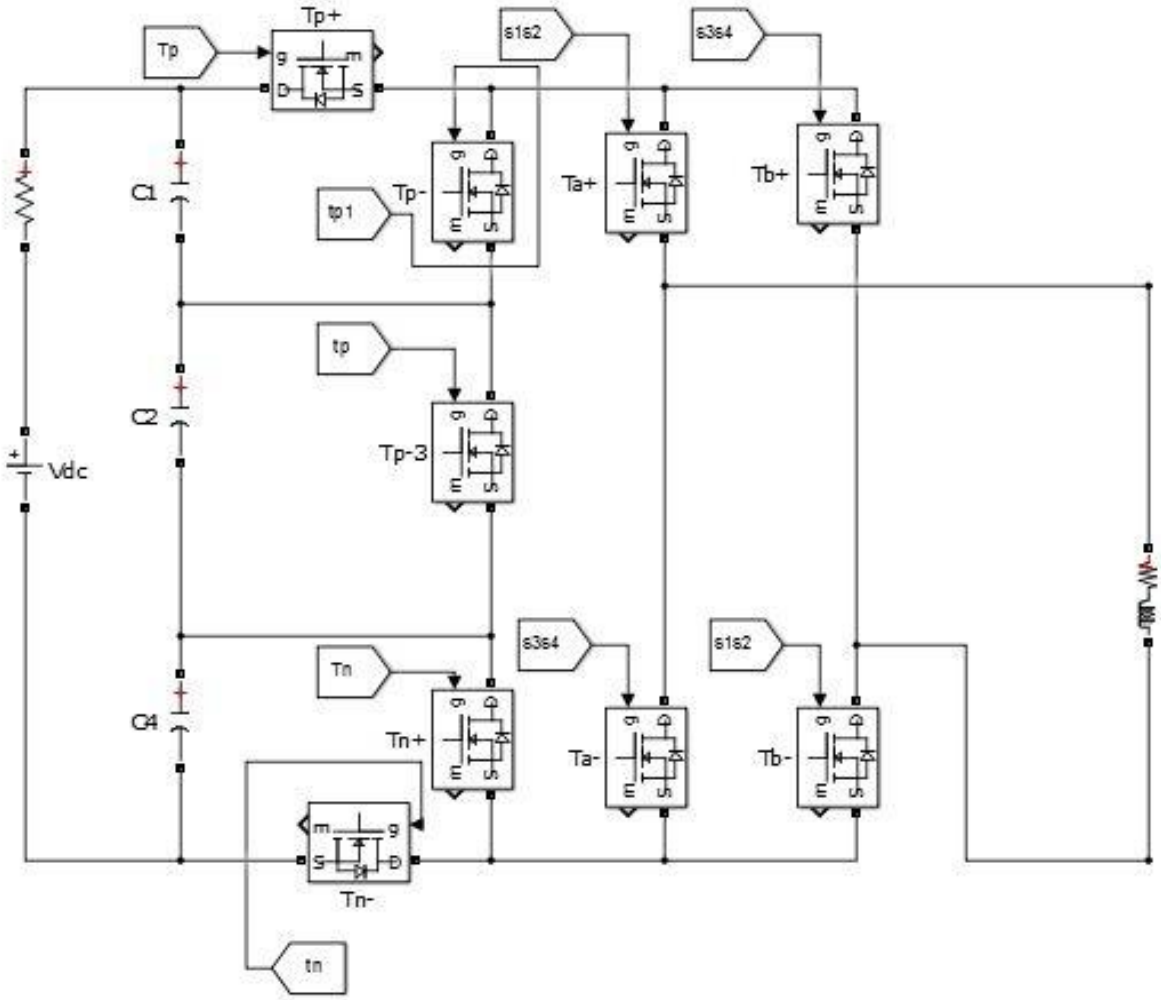

Fig 3. Simulink model of 7 level inverter.

Simulation of proposed MLI is carried MATLAB/Simulink Dc supply of 220V is given to 3 dc link capacitors are used and 9 MOSFET are used as switches. The technique used for pulse generation is POD technique. Generally in order to turn on 9 switches 9 carrier signal are required but by using proposed topology single carrier wave is used to generate signals for 9 switches. The proposed 7-level inverter is tested to verify the operating principle of the proposed MLI. The LC filter is inserted between the output of the inverter and the load. The multi level inverter is connected to LC filter in order to eliminate harmonics and pure sine wave is obtained. Electrical specifications of the proposed inverter are summarized in Table II. Fig. 4 and 5 show simulation waveforms of the proposed inverter in 7-level.

As the level of the inverter increases the total harmonic content in the signal reduces. In this paper Total harmonic distortion of 5 level and 7 level inverter (without LC filter) are shown by FFT analysis in the fig 6 and fig 7 respectively, with fundamental frequency 50 Hz.

TABLE II
Specifications of the proposed single-phase 7-level inverter

dc-link voltage	220V
Output voltage	$150V_{rms}$
dc-link capacitor	8000 mF
Filter inductor (L_f)	300 uH
Filter capacitor (C_f)	150 uF
Output frequency (f_o)	50 Hz

ISSN No: - 2456 - 2165

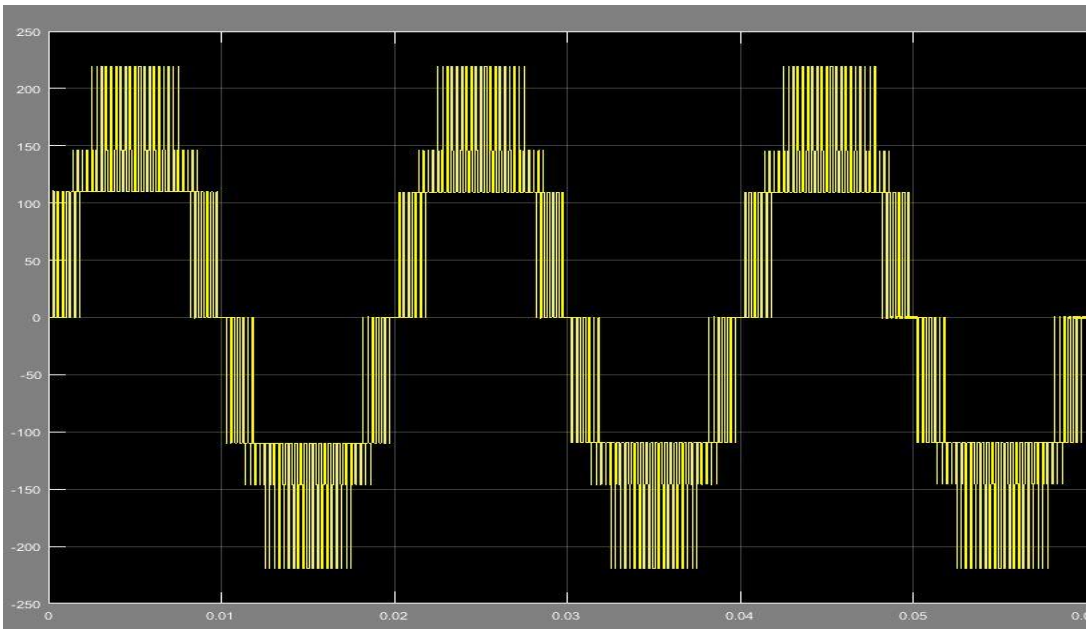

Fig 4.Output voltage of 7 level inverter

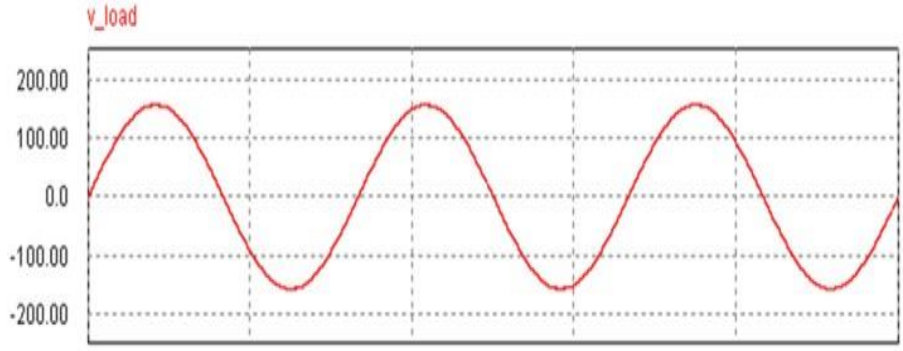

Fig 5. Output voltage with LC filter of 7 level inverter

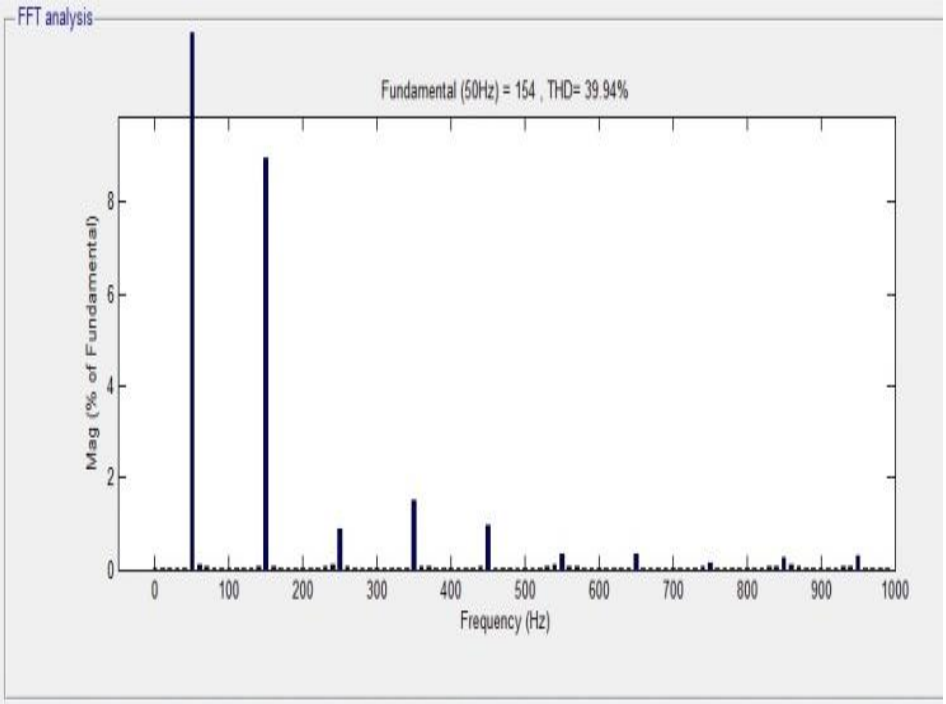

Fig 6.Total Harmonic Distortion of 5 level inverter

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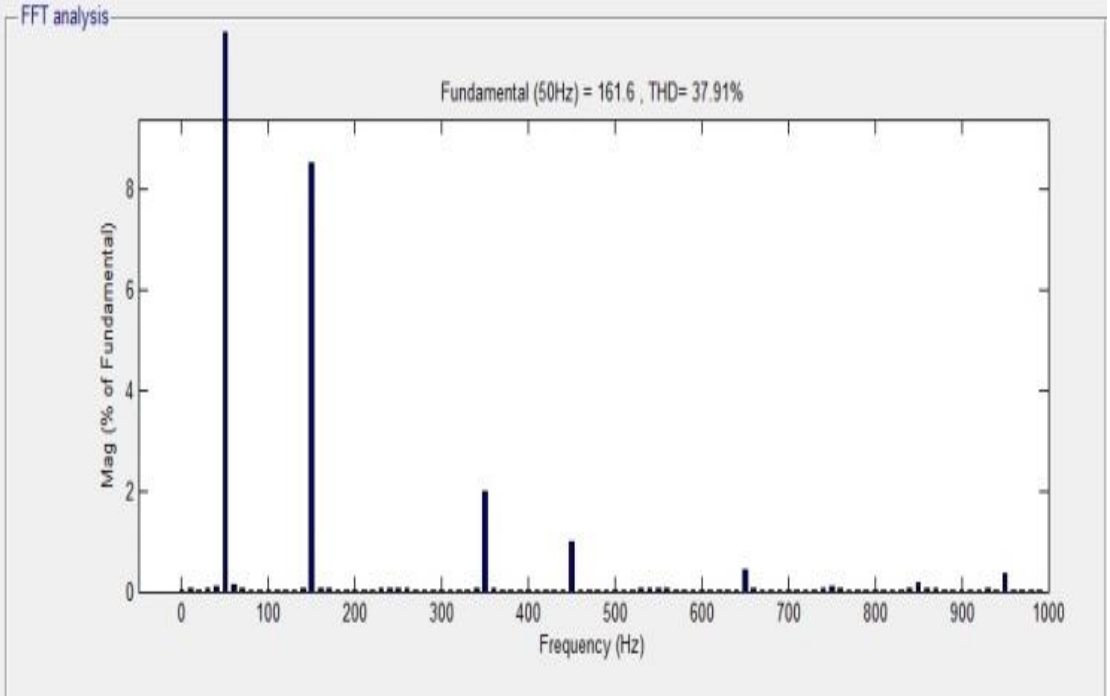

Fig 7.Total Harmonic Distortion of 7 level inverter

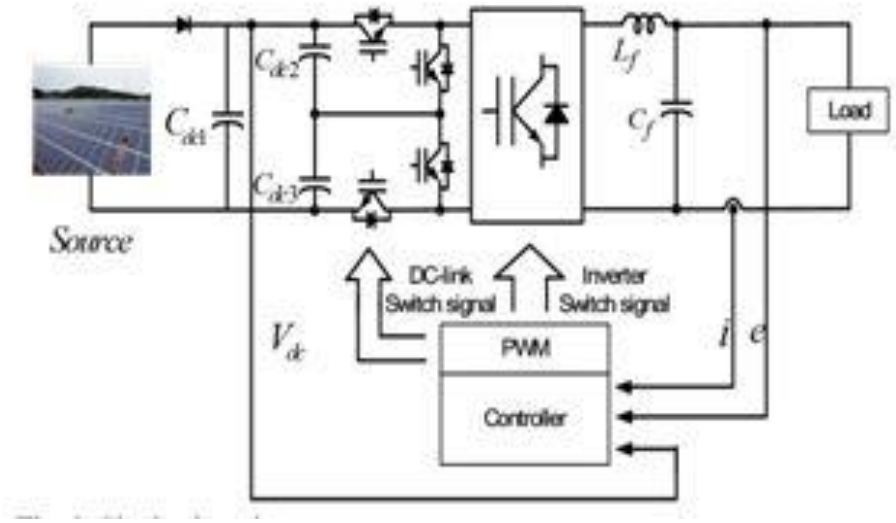

Fig 8. Single phase inverter system

IV. CONCLUSION

This paper proposed a new multi-level inverter topology based on a H-bridge inverter with four switches connected to the dc-link. The proposed MLI has the following advantages over the conventional inverters.

- Number of devices of the proposed multi-level inverter is fewer than that of the conventional multi-level inverters. Therefore, the proposed system is more reliable and cost competitive than the conventional two-level and multilevel inverters.
- The four switches (T_A^+, T_A^-, T_B^+, T_B^-) in the H-bridge are switched at a low frequency (e.g. 60 Hz). Therefore, switching loss of the four switches (T_A^+, T_A^-, T_B^+, T_B^-) is almost negligible.
- Only one carrier signal is required to generate the PWM signals for 4 switching devices (T_P^+, T_P^-, T_N^+, T_N^-).
- The proposed topology can be easily extended to 9-level or higher level with minimized active device component count as shown in fig 9.

ISSN No: - 2456 - 2165

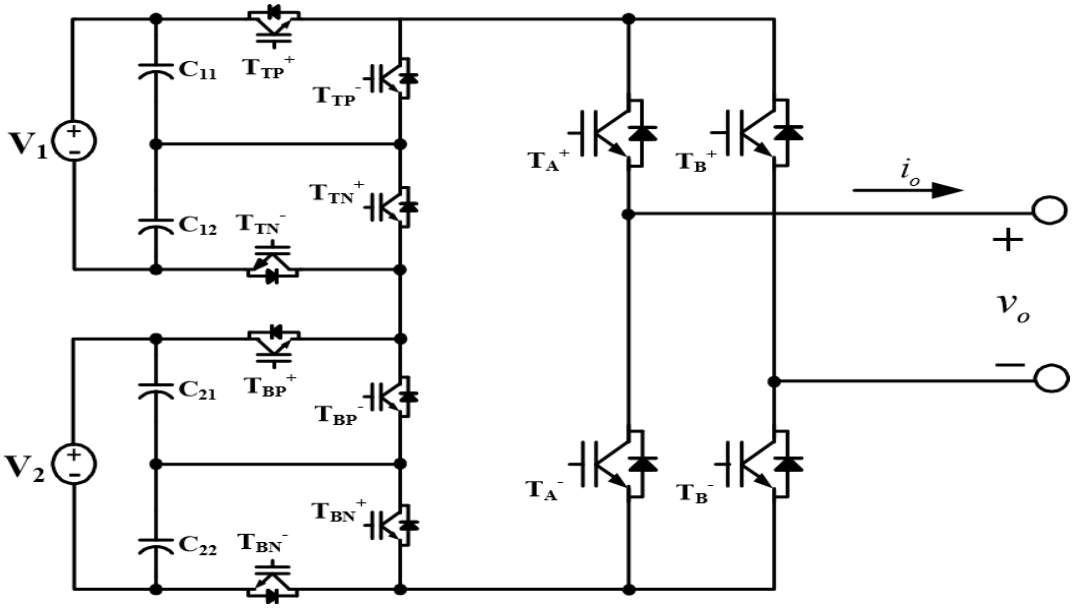

Fig 9. Extension to 9-level inverter

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