ISSN No: - 2456 – 2165

Improve performance of PIPO (Parallel in Parallel Out) Shift Register by use Transistor Gating Technique

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Abstract: - Shift registers are some sort of sequential logic circuitries that are majorly deployed to store data in digital format. In the previous paper , the implementation of a Four bit Parallel in parallel Out (PIPO) shift Register design are showing by use D Flip Flop. D Flip Flop is designing by use NAND Gate. In this Paper, Improving the performance of the D Flip Flop by use Transistor Gating Technique. As Results Session is showing the power Consumption of the NAND Gate. Power Consumption of NAND gate by use normal CMOS Design is $7.9458*10^{-11}$ watts while by use Transistor Gating Technique Power Consumption of NAND Gate gets $1.034*10^{-08}$watts. As use proposed NAND Gate Circuit in the PIPO Circuit the power consumption of the circuit gets $1.34*10^{-03}$watts.

Keywords— Power Gating; Clock Gating; Activity-Driven Optimized Clock-gating; Run Time Power Gating; Serial Input Serial Output Shift Register.

I. INTRODUCTION

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All flip-flop is driven by a common clock, and all are set or reset simultaneously. In these few lectures, the basic types of shift registers are studied, such as Serial In - Serial Out, Serial In - Parallel Out, Parallel In – Serial Out, Parallel In - Parallel Out, and bidirectional shift registers. A special form of counter - the shift register counter, is also introduced.

A. Register

- A set of n flip-flops.
- Each flip-flop stores one bit.
- Two basic functions: data storage and data movement.

II. PARALLEL IN - PARALLEL OUT SHIFT REGISTERS

For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a four-bit parallel in - parallel out shift register constructed by D flip-flops.

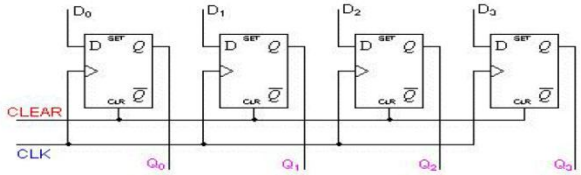

Fig. 1: Parallel in Parallel Out Design

The D's are the parallel inputs and the Q's are the parallel outputs. Once the register is clocked, all the data at the D inputs appear at the corresponding Q outputs simultaneously.

A. D Flip Flop

We remember that a simple SR flip-flop requires two inputs, one to “SET” the output and one to “RESET” the output. By connecting an inverter (NOT gate) to the SR flip-flop we can “SET” and “RESET” the flip-flop using just one input as now the two input signals are complements of each other. This complement avoids the ambiguity inherent in the SR latch when both inputs are LOW, since that state is no longer possible.

Thus this single input is called the “DATA” input. If this data input is held HIGH the flip flop would be “SET” and when it is LOW the flip flop would change and become “RESET”. However, this would be rather pointless since the output of the flip flop would always change on every pulse applied to this data input.

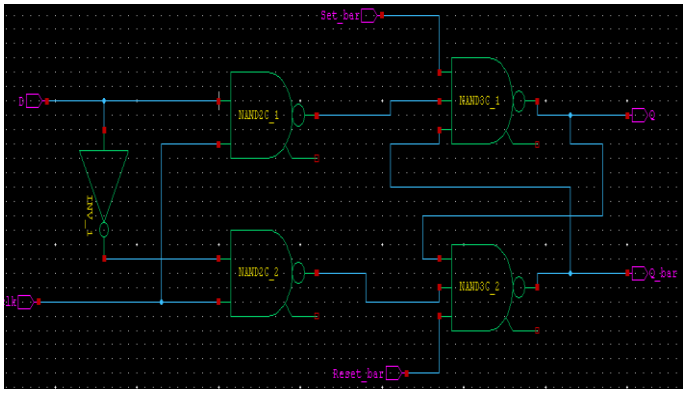

Fig. 2: D Flip Flop Design by NAND Gate at Tanner

ISSN No: - 2456 – 2165

Figure 2 is showing the circuit for the D Flip Flop by use NAND Gate. As we can see from the Figure 3.2 , using two inputs D and Clock while 2 output Q and Q_Bar. In this Design using 4 NAND Gate Design while one inverter is using. Set and Reset input bar will be Logic High . that means the value of these input will logic 1. Q and Q_bar are the outputs of the D Flip Flop.

B. Parallel In Parallel Out by D Flip Flop

Figure 3 is showing the circuit for the Parallel In Parallel Out (PIPO) bys use D Flip Flop. As figure 3 is showing the input of the PIPO are Din and Clock while output are Dout1, Dout2, Dout3 and Dout4. Set and Reset bar of every D Flip Flop will be High.

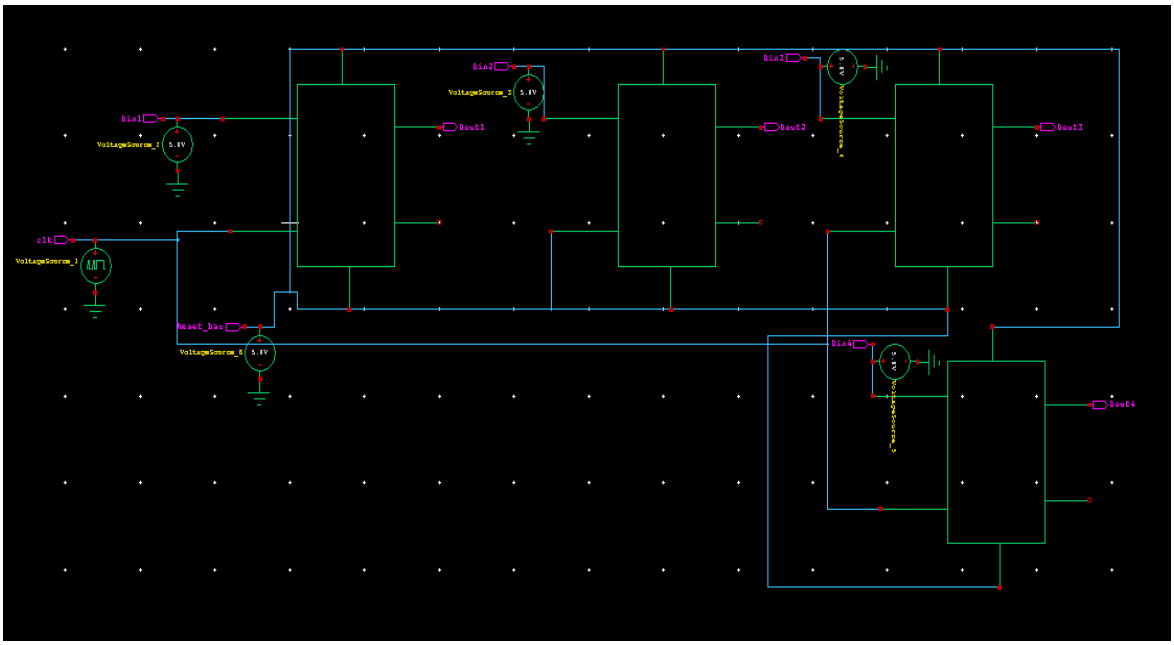

Fig. 3. PIPO Design by use D Flip Flop

III. PROPOSED METHODOLOGY

A. Transistor Gating Technique

This technique also involves 2 sleep transistors, one of them being added between pull-up network and circuit output and another between pull-down network and ground, with both of them aiding in leakage current minimization as in power and drain gating techniques [2]. The Transistor Gating Technique is shown in Figure 4.

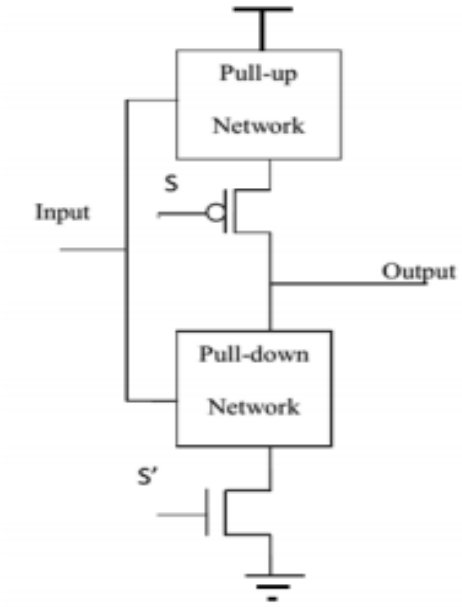

Fig. 4. Transistor Gating Technique

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B. NAND Gate Design by Transistor Gating Technique

Figure 5 is showing the circuit for the NAND gate by use Transistor Gating Technique. As Figure is showing, two extra transistors have been added from Pull up network and Pull Down Network. This transistor will stop the Leakage power of the circuit. A PMOS transistor is connected by Pull Up Network and a NMOS transistor is connected by Pull Down Network. The input of this transistor will be logic Low. That means input of these transistor will be logic 0.

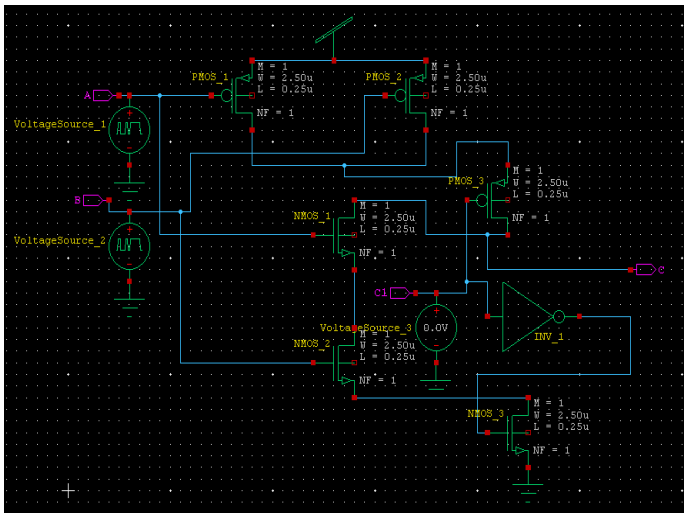

Fig. 5 . NAND Gate design by Transistor Gating Technique

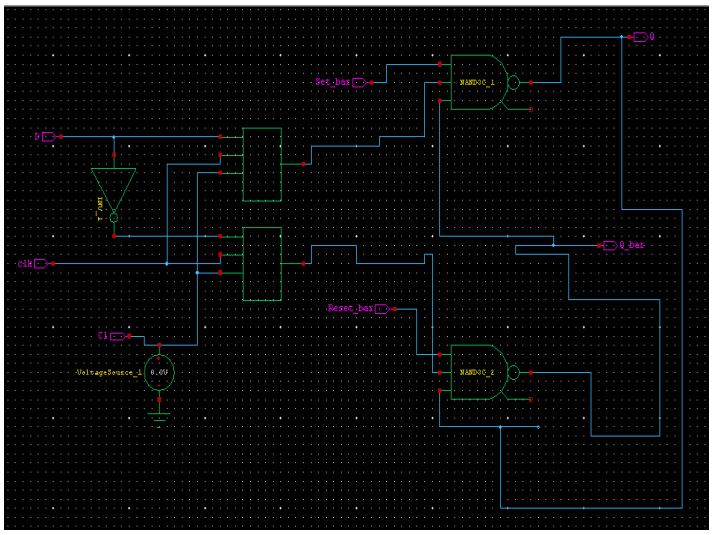

Fig. 6. D Flip Flop by use Transistor Gating

Figure 6 is showing D Flip Flop by use Transistor gating Technique. In this design , replace the 2 NAND Gate Circuit of the D flip flop by proposed NAND gate Circuit. Third input of the NAND gate will be Logic 0. In the Proposed D Flip Flop circuit only 2 NAND gate will replace. Next 2 NAND gate can't replace because these 2 NAND gates are changing the output waveform of the circuit.

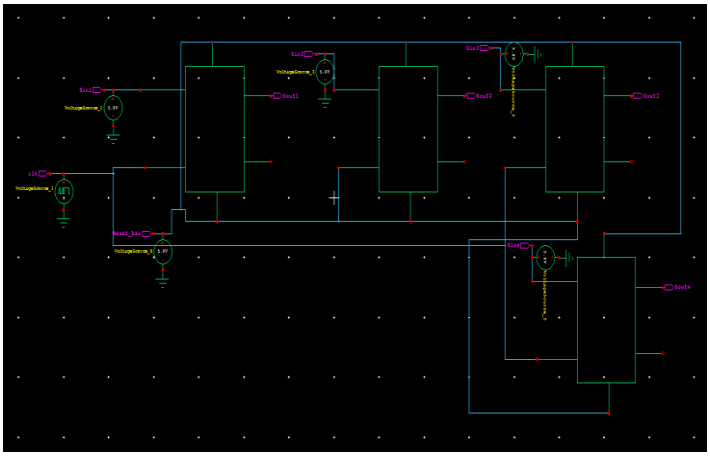

Fig. 7. Proposed PIPO circuit by Transistor Gating Technique

Figure 7 is showing the PIPO(Parallel in Parallel Out) circuit by use of Transistor Gating Technique. In this Circuit, Transistor Gating Based D Flip Flop is using. That D Flip Flop is design by Transistor gating based NAND Gate.

IV. RESULTS

A. NAND Gate Design

- *CMOS Design of NAND Gate*

Figure 8 is showing the circuit of NAND gate by use CMOS design. The Power consumption for the design NAND gate is $4.01*10^{-4}$ watts.

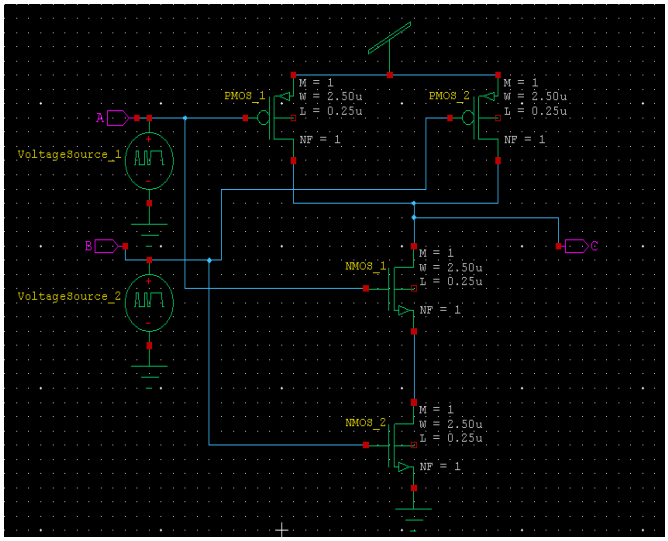

Fig. 8. NAND Gate Circuit

- *Proposed NAND gate Design by Transistor Gating*

Figure 9 is showing the proposed NAND Gate design by use Transistor Gating Technique. The Power Consumption of proposed NAND Gate design is $2.34*10^{-4}$watts.

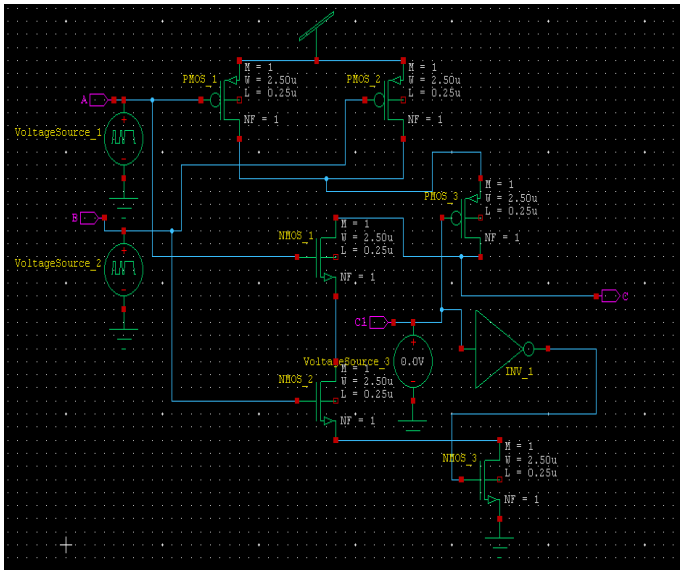

Fig. 9. Proposed NAND Gate Circuit by use Transistor Gating

	NAND gate Design	Proposed NAND Gate Design
Power Consumption	$4.01*10^{-4}$ watts	$2.34*10^{-4}$ watts

Table 1: Comparison Table for NAND Gate

B. D Flip Flop

- *D Flip Flop Design by CMOS Design*

Figure 10 is showing the D Flip Flop Circuit by use Normal NAND Gate. Power Consumption for D Flip Flop is $1.49*10^{-03}$watts. In this circuit 4 NAND Gates are using.

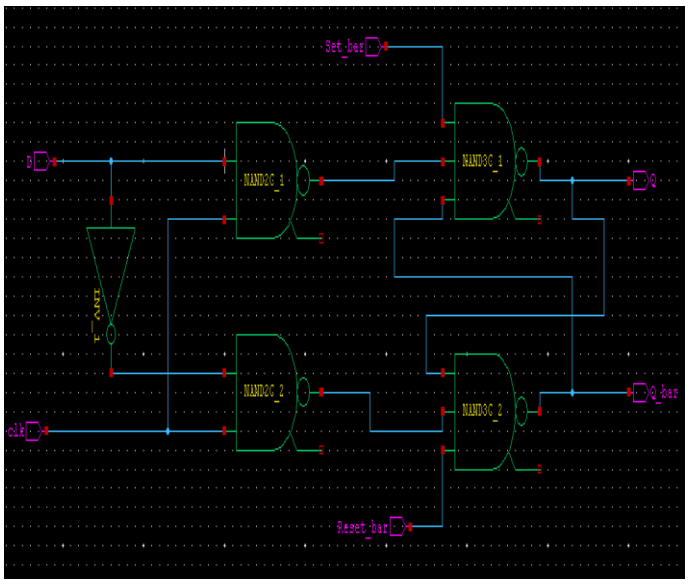

Fig. 10. D Flip Flop Design by NAND gate

- *Proposed D Flip Flop by use Transistor Gating*

Figure 11 is showing the proposed D Flip Flop Circuit by use Proposed NAND Gate. The Power Consumption for the Proposed D Flip Flop is $1.143*10^{-03}$ watts.

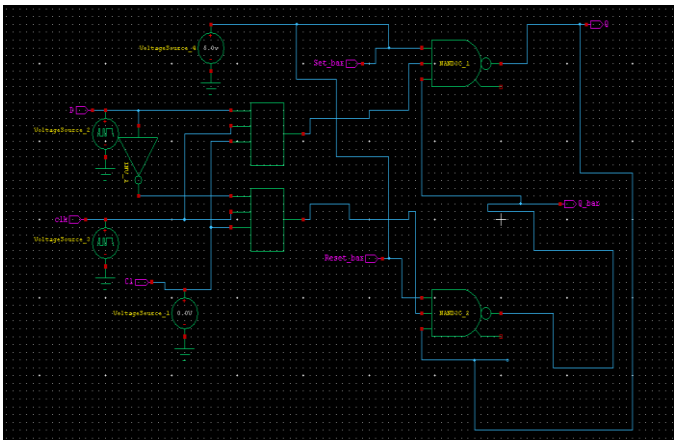

Fig. 11. Proposed D Flip Flop by use Transistor Gating

	D Flip Flop Design	Proposed D Flip Flop Design
Power Consumption	$1.49*10^{-3}$ Watts	$1.143*10^{-3}$ Watts

Table 2: Comparison Table for the D Flip Flop

C. Parallel in Parallel Out (PIPO) Design

- *PIPO Circuit by use CMOS Design*

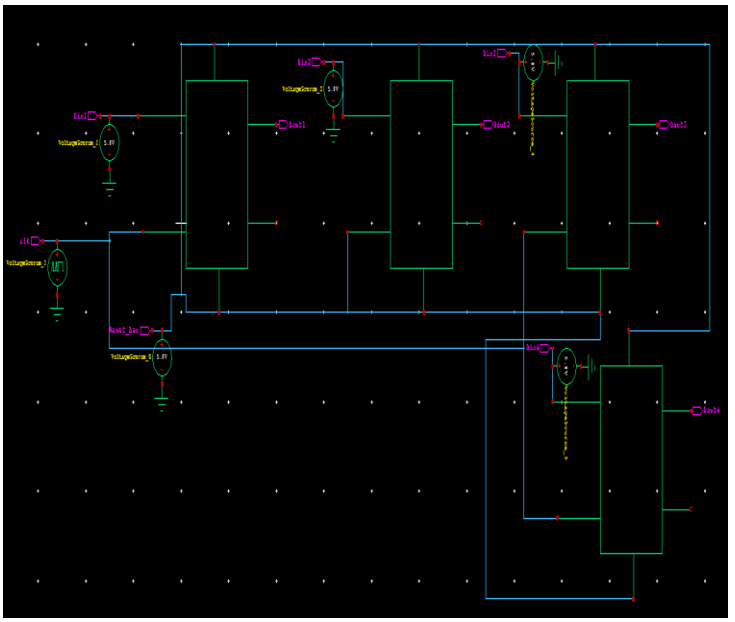

Fig. 12. PIPO Circuit by use normal D Flip Flop

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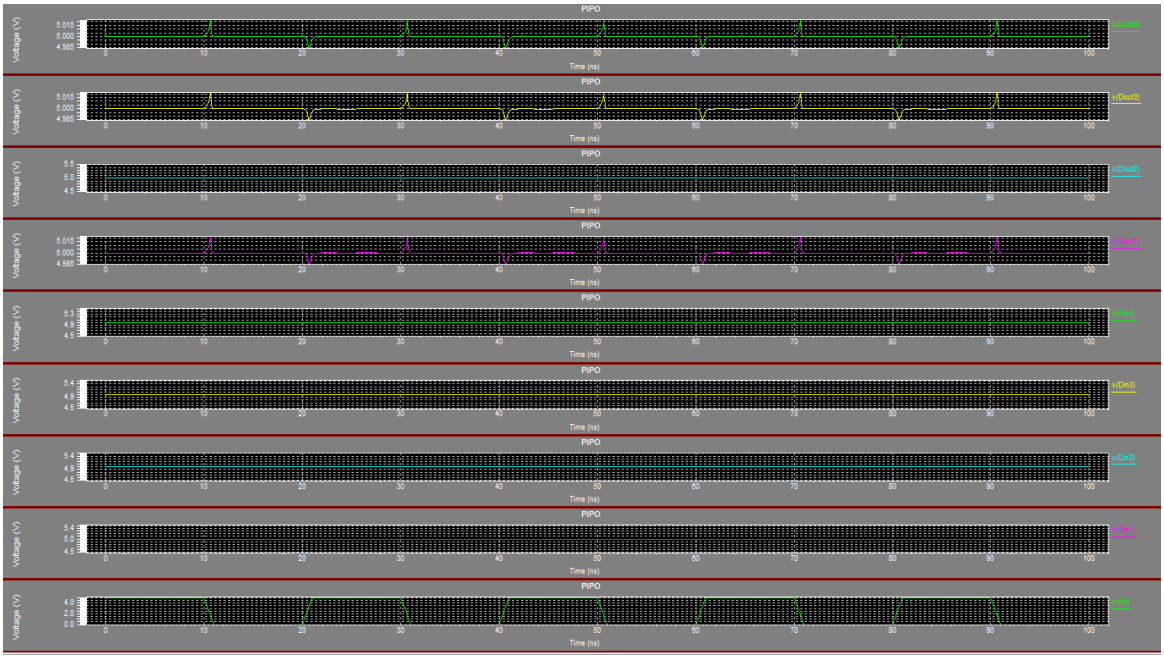

Fig. 13. Output Waveform

Figure 12 is showing the PIPO circuit by use Normal D Flip Flop. The Power Consumption of the PIPO is $2.7474*10^{-03}$watts. Fig 13 is showing the output Waveform for the Normal PIPO circuit.

- *Proposed PIPO circuit by use Proposed D Flip Flop*

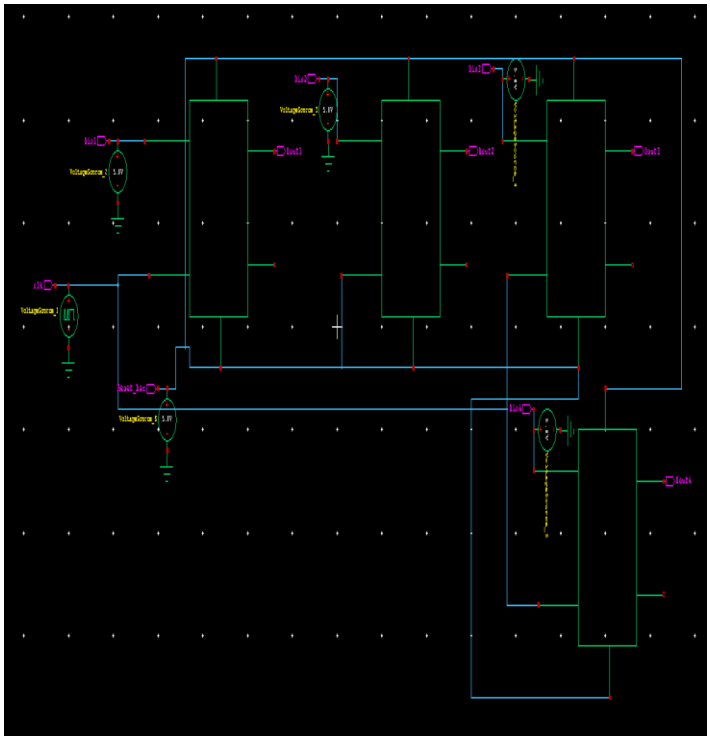

Fig. 14. Proposed PIPO circuit by use Proposed D Flip Flop

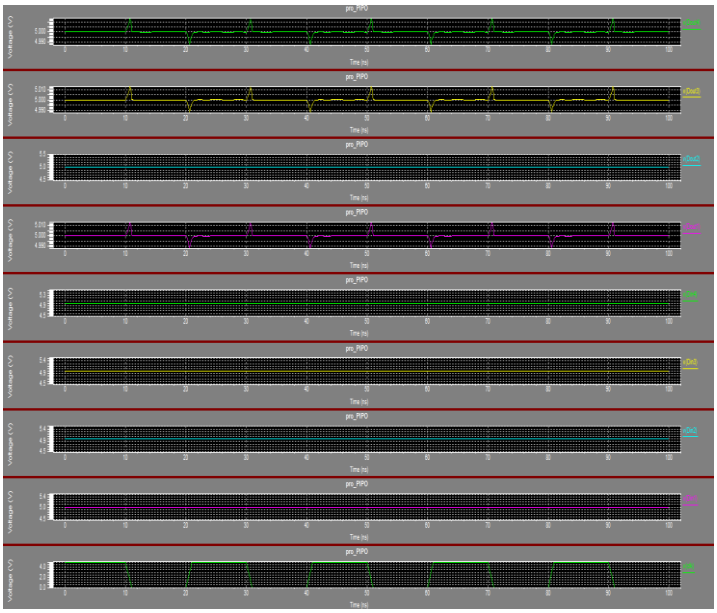

Fig. 15. Output Waveform of PIPO Circuit

Figure 15 is showing the PIPO circuit by use proposed D Flip Flop. The Power Consumption for the Proposed PIPO is $1.34*10^{-03}$ watts.

	Normal PIPO Circuit	**Proposed PIPO Circuit**
Power Consumption	$2.7474*10^{-03}$ watts	$1.34*10^{-03}$watts

Table 3: Comparison Table

V. CONCLUSION AND FUTURE SCOPE

A. Conclusion

In this Research, reducing the Power Consumption of the Proposed PIPO (Parallel in Parallel Out) circuit. For Reduce the Power Consumption , using Transistor Gating Technique. It will reduce the Power consumption of the NAND gate , D Flip Flop and PIPO Circuit. For Design the circuit , working at 130 nm Channel length file. As Results are showing for the NAND gate , D Flip Flop and Proposed PIPO Power Consumption is reducing from the Existing Circuit. Normal PIPO circuit power consumption is $2.7474 * 10^{-03}$ watts while proposed PIPO circuit Power Consumption is $1.34 * 10^{-03}$ watts. That means Power Consumption is reducing for the Transistor gating technique.

B. Future Scope

In the Future , we can further Reduce the Power Consumption of the circuit. In the Future ,we can work at Area also. We can reduce the Area of the circuit.

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