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Linear-Phase FIR Filter Using Low Power Multipliers

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Abstract—The main idea is to reduce the power consumption of FIR filter using low power techniques. The Multipliers are heart of the FIR filter which consumes more power, two architectures namely partitioned Multiplier and selective Activation Multiplier are used to achieve low power. Folding technique is used to reduce the number of Multipliers in FIR filter which refers to reduction in power consumption. Power, Delay and Area are calculated using Cadence software. The power reduction is recorded around 34.9% for FIR filter using Partition Multiplier.

Keywords— Low-Power Multipliers, FIR Filter, Folding Technique.

I. INTRODUCTION

Power reduction [1] is an important design goal in many electronic systems over many decades. More power consumption results in heating up the devices so that performance, reliability and durability are effected. Hence, low power techniques are needed.

Multipliers are widely used in many applications. There are many Multipliers namely Array Multipliers, Booth Multipliers [2], Wallace tree Multipliers and so on. Array Multipliers are better than the remaining Multipliers because it involves partial product generation and their addition. Multipliers generally occupy more area, delay and power. Therefore power reduction in multipliers is necessary to achieve low power systems. The two architectures namely Partitioned Multiplier (PM) and Selective Activation (SA) [3] are used to reduce the power consumption.

Multipliers are foremost parts of major Digital Signal Processing applications, FIR is one of those applications which contains Multipliers to the core part because the output Y(n) is the product of input X(n) and transfer function H(n) [4].

$$Y(n) = H(n) * X(n)$$

FIR filter when implemented in linear-phase will have more number of Multipliers, to reduce the power consumption of the filter folding technique [4] can be used. This technique helps in reducing the Multiplier count to half which simultaneously results in power reduction [5] of filter.

II. PROPOSED ARCHITECTURES

In this segment the two architectures PM and SA are explained in detail. The main criteria is to minimize the power consumption in Multipliers with introduction of architectures that take advantage of input data characteristics. The basic theory of Architectures is to partition a Multiplier such that all parts are not activated for every change in inputs.

A. Selective Activation Approach

In this approach the architecture mainly consists of three blocks namely Selector, Larger section and smaller section. Selector acts as a switch to both smaller and larger parts. It first divides the data into two equal halves, one is LSB part and another is MSB part. Depending on the pre-defined range and position of 1's in the MSB part the selector sends the data to respective part for execution. If one section is active the other remains inactive. Suppose the input 'a' and 'b' of length n is given it gets divided to A_{LSB}, A_{MSB}, B_{LSB}, B_{MSB}.

$$A_{LSB} = a\,[k\text{-}1, 0] \quad .....(1)$$

$$A_{MSB} = a\,[n\text{-}1, k] \quad .....(2)$$

$$B_{LSB} = b\,[k\text{-}1, 0] \quad ....(3)$$

$$B_{MSB} = b\,[n\text{-}1, k] \quad .....(4)$$

Where k is the number of bits that LSB part must contain, and k <= n-2. A select signal is cited when both A_{MSB} and B_{MSB} are either all-zero or all one. The number of Multipliers in larger section and smaller section vary according to the size of the input data (n). Any Multiplier like Array Multiplier, Booth Multiplier and so on can be used in selective Activation approach. Here Carry Save Array Multiplier [3] is used for better performance. After the multiplication operation concatenations, additions and subtractions are calculated to obtain the output. Power, area and delay are obtained using Cadence software.

Selective Activation	8 bit	16 bit
Power (mW)	0.41	2.57
Critical path delay (n S)	5.49	11.45
Area (in cells)	6044	25254

Table. 1: Power, Area And Delay of Selective Activation For N=8, 16 Bit.

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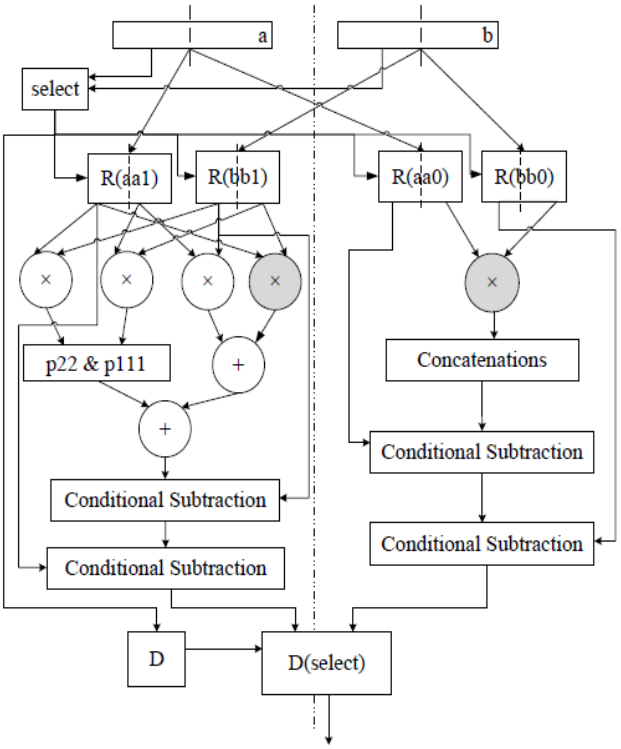

Fig. 1: Selective Activation Architecture

B. *Partition Multiplication Approach*

Selective Activation technique [6] requires all 1's or all 0's in the most significant part of input activate smaller section. This specification may not be real for some applications because if one section is active the other section consumes static power.so the partition multiplication approach [3] is introduced.

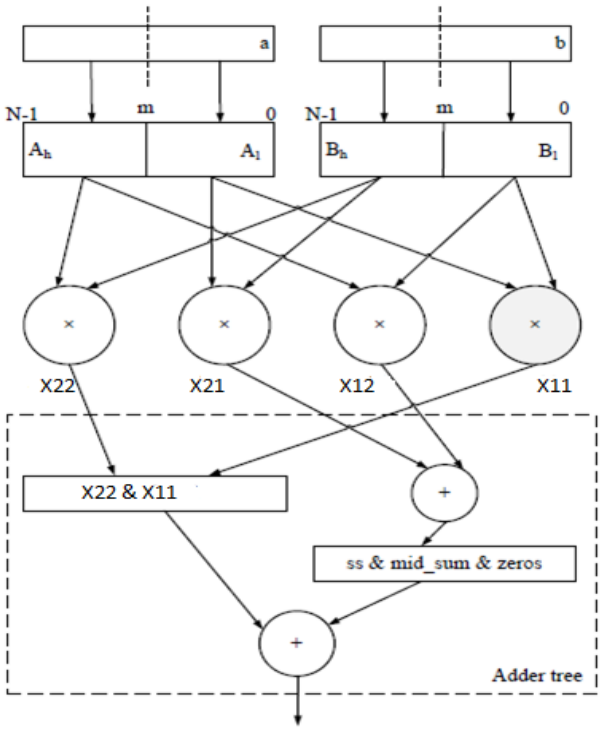

Fig. 2: Partitioning Multiplier Architecture.

In this the additional circuitry is minimized. The Fig. 2 illustrate the working of partition multiplier. In this multiplier, the multiplication is split into 4 independent multiplication which calculate four partial products x11, x12, x21, x22. Among these four only x11 is unsigned. All the four partial products are concatenated after series of operations to provide multiplied output. Here Carry Save Array (CSA) is used to compute the partial products, the size of CSA varies with the size of the input.

Since the circuitry is less compared to Selective Activation [6] approach the power consumption [8] also reduces in this partitioned approach. Hence the partition Multiplier is more efficient than Selective Activation Multiplier in terms of power consumption, area required and delay.

Partitioned Multiplier	8 Bit	16 Bit
Power (mW)	0.351	2.06
Critical path delay (nS)	5.37	11.29
Area (in cells)	4797	20417

Table. 2: Power, Delay And Area For 8 Bit And 16 Bit Partitioned Multiplier.

III. COMPARISON

A. *Power Dissipation*

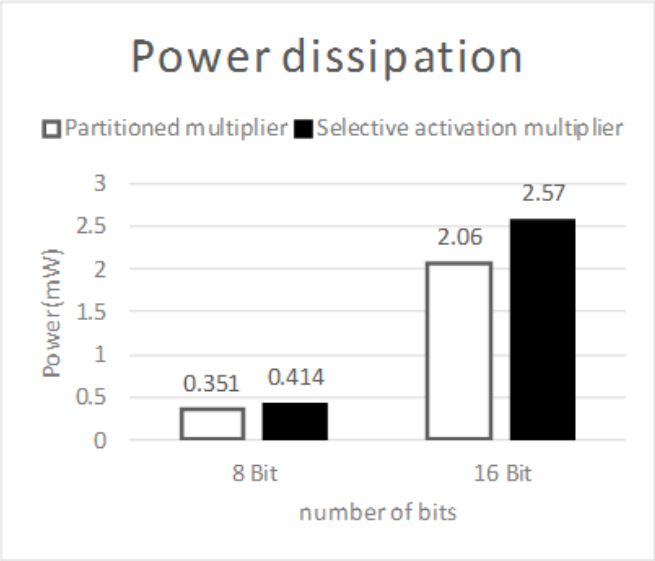

Fig. 3: Comparison of Power Consumed By Partition And Selective Activation Multiplier For N=8, 16 Bit.

The theoretical calculation using Cadence simulation tool shows that 8 Bit Carry-Save Array (CSA) multiplier consumes 0.40mW whereas Partition multiplier consumes 0.35mW. The reduction in power consumption is 12.25% because CSA

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consists of more number of adders and gates which increase the power consumption. 8 Bit Selective Activation multiplier consumes 0.414mW which is more than Partition multiplier, this is due to static power consumption of one of the two paths of Selective Activation multiplier when another path is in use. Similarly the Power consumption of 16 bit Partition and Selective Activation multiplier is 2.06mW and 2.57mW respectively.

B. Critical Path Delay

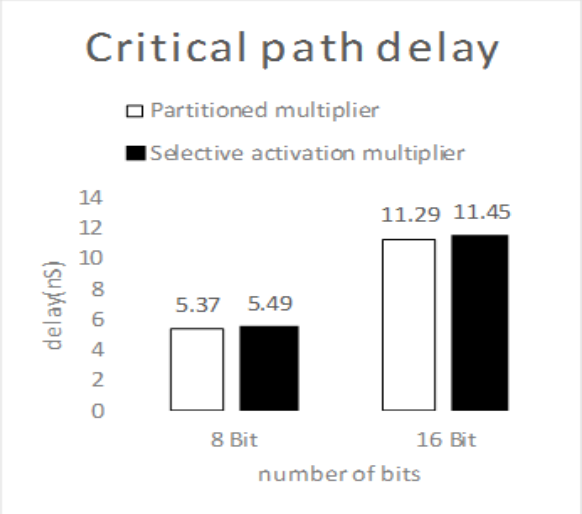

Fig. 4: Critical path delay comparison of Partition and Selective Activation multiplier for n=8, 16 Bit.

Critical path delay is the shortest path delay in a circuit. Delay for 8 Bit Partition and Selective Activation multiplier is 5.37nS and 5.49nS respectively, the increase in delay of selective Activation multiplier is due to the Selector block. Similarly the delay for 16 bit Partition and Selective Activation multiplier is 11.29nS and 11.45nS respectively.

C. Area

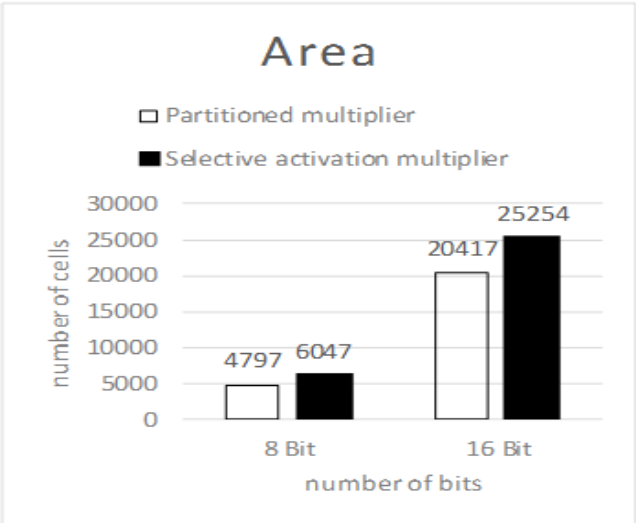

Fig. 5: Area Comparison of Partition And Selective Activation Multiplier For N= 8, 16 Bit.

Area requirement for 8 Bit and 16 Bit Partitioned multiplier is 4797 and 20417 cells respectively, whereas for Selective Activation multiplier it is 6047 and 25254 cells respectively. The reason for increase in area requirement of Selective Activation multiplier is, it provide two different paths for multiplication.

IV. APPLICATION

Finite Impulse Response (FIR) is one of the extensively used operation in Digital Signal Processing. Implementation of an FIR filter comprises of three blocks namely multiplication, addition and signal delay. Generally D flip flop is used in delay block and ripple carry adders are used in adders block. In linear phase FIR filter [7] for n delays there will be n+1 Multipliers, Multipliers consume more power in FIR filter. So partition Multipliers [3] are used in Multiplier block to reduce power consumption and it is reduced up to 21.7%.

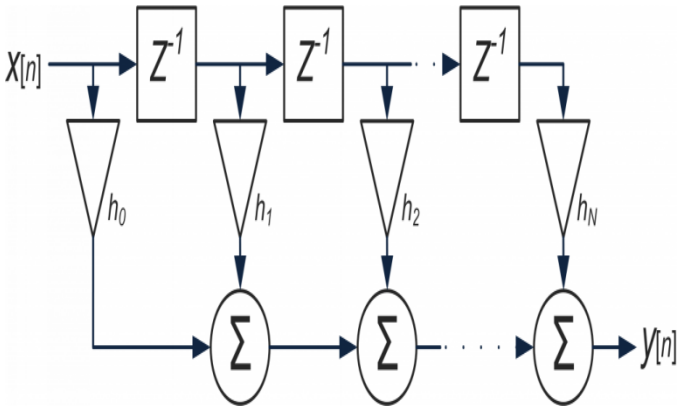

Fig. 6 Block Diagram of Linear-Phase FIR Filter

One way of increasing the power reduction in FIR filter is to decrease the number of Multipliers, this can be done by a technique called folding technique [4]. If the phase of filter is linear, the symmetrical architecture is used to decrease the Multiplier operation. Comparing Fig. 6 and Fig. 7 the reduction in Multiplier count is observed to be half of the Multipliers in Fig. 6.

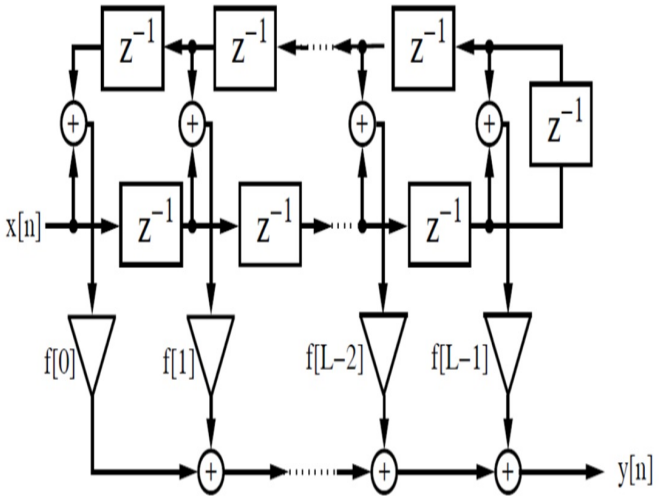

Fig. 7 Linear-Phase Folded FIR Filter

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FIR filter when implemented in linear-phase [5] consumes 1.06mW, same FIR filter when implemented using folding technique consumes 0.898mW. The power reduction is 15.28% and the area is greatly reduced up to 32.5%. This reduction in area helps in reducing the chip area.

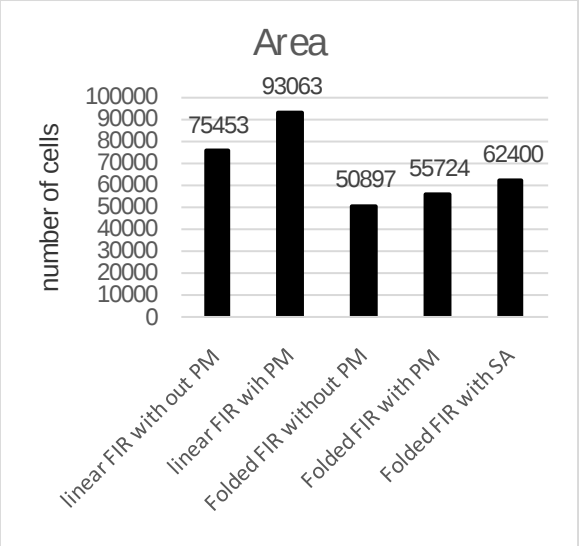

Fig. 8: Area Comparison of FIR Filter Using Different Multipliers.

Area requirement of linear and folded FIR using Partition multiplier is 93063 and 55724 respectively, the reduction in area is 40.1%. This is because Folded FIR consists of less multipliers compared to linear FIR.

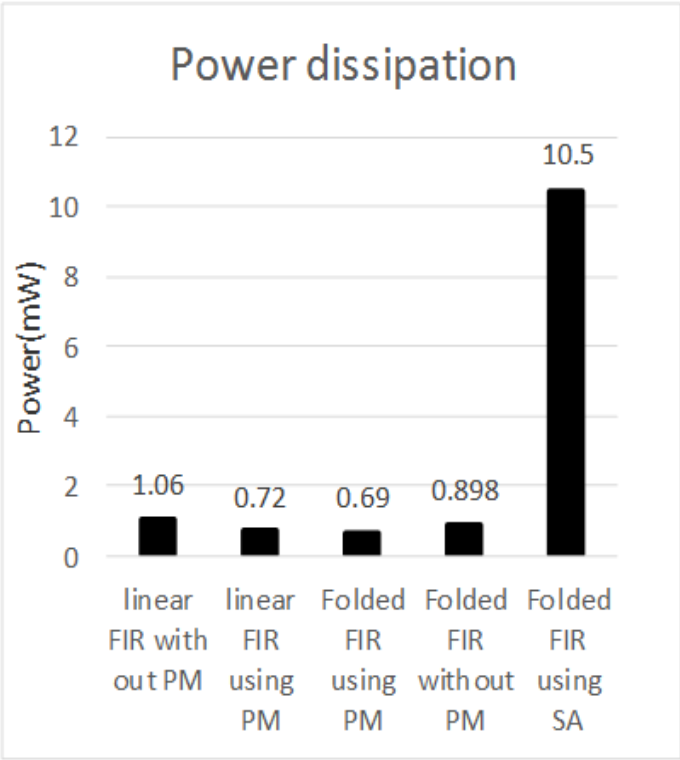

Fig. 9: Power Comparison f FIR Filter Using Different Multipliers.

The power consumption of linear and Folded FIR is 1.06mW and 0.898mW respectively, whereas power consumption using Partition multiplier is 0.72mW and 0.69mW respectively because the number of delays and multipliers gets reduced.

V. CONCLUSIONS

The Multipliers proposed in this paper can be used for various Digital Signal Processing applications. The main advantage of this Multipliers is reduction in power consumption. Partitioned Multiplier consumes 12.5% less power compared to Carry Save Array Multiplier (CSA) with approximately 1% area overhead. Since FIR filter mostly comprises of Multipliers, folding technique can be used to reduce both area requirement and power consumption. Power reduction is achieved up to 34.9% and area requirement is reduced up to 26.1% when folded FIR using Partition multiplier is compared with linear FIR. The Multipliers and FIR filter are designed in Xilinx 14.6, implemented using Spartan 3 FPGA kit and the above mentioned Power, Area and Delay are analyzed using Cadence software.

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