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A Study on Leakage Power in Flip Flops

Abdul Aleem Mohammad
Aleem1625@Gmail.Com

Abstract:-Aggressive scaling of CMOS devices in each technology generation to achieve higher integration density and effective performances has left over so many challenges for designers. The more and more accommodation of components on chip had led to rise in power dissipation as the major challenge. As MOS transistors enter Deep Submicron (DSM) sizes, undesirable consequences regarding power consumption arise. With the smaller geometries in DSM, the number of gates that need to be integrated on a single chip, power density and total power are increasing rapidly. Through this paper, an analytical study on different approaches used to reduce leakage power in sequential circuits especially flip flops has been presented.

Continuous efforts have been made by researchers in the recent past to find new techniques in the field of digital sequential circuits to reduce leakage power to obtain a balancing performance among power, delay and area. Much more exploration is needed as the design aspect is concerned.

I. INTRODUCTION

For the battery operated portable devices, high speed and low power consuming memory elements are needed. Being the basic memory elements, flip flops also act as critical timing elements in digital systems. Even in idle mode flip flops consume much power creating a significant impact on speed as well as delay. Flip flops are used in computational circuits to operate in a sequential manner on recurring clock intervals to receive and store data for a limited period and are completely dependent on clock edges, so referred as edge triggered flipflops.

Flip flops operate mainly in three regions,

Stable Region: In this region setup and hold times are met and this is considered as the desirable region of operation.

Meta Stable Region:The clock-to-Q delay in non-predictable and non-deterministic and this may cause failures.

Failure Region: Where changes in data are unable to be transferred to the output of the flipflop.

CMOS technology allows a very different approach to flipflop design and construction. Scaling in CMOS technology improved the speed nevertheless the leakage currents are left over as an adverse effect. Leakage power comes into existence when the battery-operated devices are in standby mode operation. Anyhow leakage power directly depends on leakage current various other factors.

II. POWER DISSIPATION IN CMOS CIRCUITS

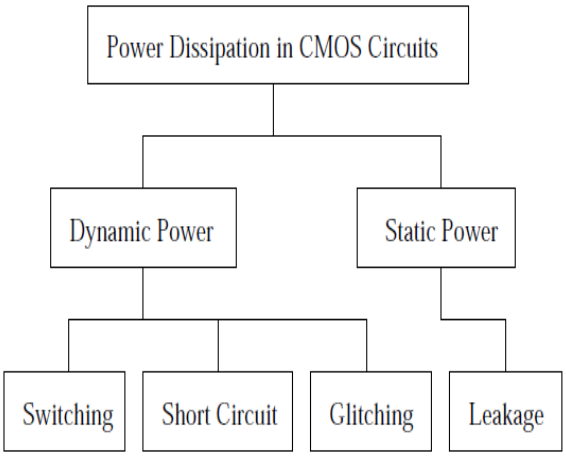


Fig.1: Power Sissipation in CMOS Circuits

Power dissipation in CMOS circuits can be categorised into two types.

- Dynamic power dissipation
- Static power dissipation.

The above mentioned types of power dissipations are actually time-averaged power consumption in conventional CMOS digital circuits. The dynamic power dissipation in the digital logic circuits and the associated logic gates is generated by process of switching from one state to another state. During this switching from one state to another state, charging and discharging of capacitances take place resulting in power consumption. Whereas Static power dissipation is concerened it is mainly because of standby/inactive logic gates in the circuits.Glitching occurs due to a mismatch or imbalance in the path lengths.

A. Dynamic Power Dissipation:

The major component of Dynamic power dissipation arises from Transient switching behaviour of the nodes. Continuous high and low transitions between any two logic levels results in charging and discharging parasitic capacitances. In the Deep Submicron(DSM) process this

dynamic power dissipation can be reduced by proper adjustments of threshold and supply voltages.

B. Static Power Dissipation:

In a transistor when there are no transactions occuring, there is a leakage current from supply to ground which mainly depends on the oxide thickness and gate length.
If the same technique used in dynamic power redcuction is employed here for static power reduction, in this case the leakage current increases exponentially which thereby increases the static power dissipation.

C. The Leakage Current:

In the CMOS circuits if the treshold voltage, channel length and gate oxide thickness are reduced, then high leakage current becomes major contributor to the overall power dissipation.

III. LEAKAGE POWER ANALYSIS

Different types of Leakage Components are:

- Sub Threshold Leakage (weak inversion current)
- Gate Oxide Leakage (Tunneling Current)
- Channel Punch Through
- Gate Induced Drain Leakage
- Drain Induced Barrier Lowering Effect
- Narrow Channel Effects
- Hot-Carrier Injection

A. Sub Threshold Leakage (weak inversion current) {I_2}:

Sub Threshold conduction from source to drain of a MOSFET results in sub threshold leakage current becsause of the weak inversion region i.e gate-to-source voltages are below the threshold voltage.
Expressed as

$$I_{ds}=\mu_0 C_{0x}.W/L.V^2.e^{(Vgs-Vth)/\eta V}$$

B. Gate Oxide Leakage(Tuneling Current){I_3}

It arises due to the finite(non zero) probability of an electron directly tunnelimg through the insulating SiO_2 layer. The gate leakage increases exponentially as the oxide thickness is reduced. To further decrease the effective oxide thickness alternative high dielectric constant materials can be used.

C. Channel Punch Through {I_6}

For a MOSFET in saturation (pinched off) V_{DS} is always lessthan V_{GS}-V_{TH} so that at no point along the channel is the inversion charge zero. When V_{DS}= V_{GS}-V_{TH}, the inversion charge under the gate is zero.The $V_{D,SAT}$ = V_{GS}-V_{TH} indicates the Pinched-off drain channel interface. Further increase in V_{DS}, makes the device punched through as the drain-substrate depletion region extends from the drain to source. The depletion region around drain and source merge eachother causing a rapid increase in the current that indicates increase in conductance and limits the maximum operating voltage of the device.

D. Gate Inducecd Drain Leakage Current {I_5}

In thin Oxide MOSFET's, as the drain voltages are much less than the Junction breakdown voltage a significant gate induced drain leakage current is detected. This drain current is caused because of the gate induced high electric field in the gate to drain overlap region.

However Band-to-Band tunneling process is useful to reduce this effect in which the gate-to-drain overlap region generate electron-hole pairs by tunneling of valence band electrons into the conduction band(holes in n-MOSFETs and electrons in p-MOSFETs).

E. Drain Induced Barrier Lowering Effect:

In the MOSFET's, when the depletion region of the drain interacts with the source near the channel surface to lower the source potential barrier. This condition is reffered to as DIBL. With out the gate interaction the carriers are injected into the channel surface by the source.

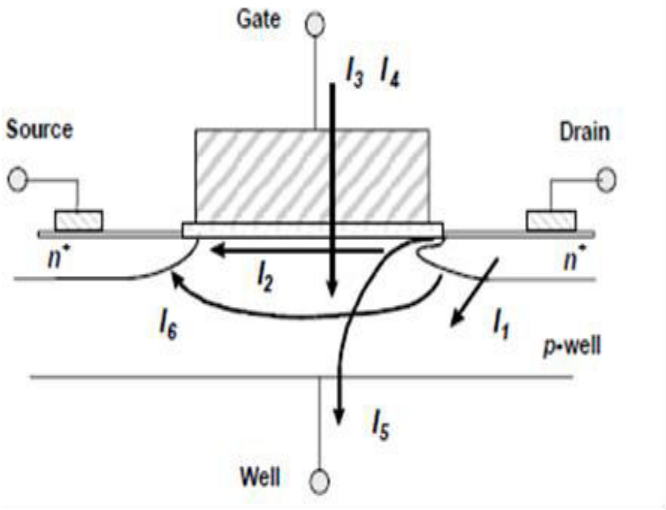
F. Narrow Channel Effects

MOS transistors which have narrow channel widths require higher values of Threshold voltages to operate.

G. Hot Carrier Injection{I_4}:

If a MOS transistor is operated under pinch-off condition also known as "satuarted case", hot carriers travelling with saturation velocity can cause parasatic effects at the drain side of the channel known as Hot Carrier Effects. This carriers can create Impact Ionisation. The generated bulk minority carriers can either collected by the drain or injected into the gate oxide.

Hot carriers can also generate traps at the silicon oxide interface known as the "fast surface states" leading to subthreshold swing deterioration and stress induced leakage current. Lighthly Dopped Drain(LDD) or Graded Channel(GC) structures help to reduce the drain electric field while maintaining a high supply voltage.



I_1 is the Reverse bias pn junction leakage current

Fig.2 Summary of Leakage Currents in Transistors

IV. SCALING IMPACT ON LEAKAGE CURRENTS

In 1975, Gordan Moore predicted that the number of transistors per square inch on an IC will approximately double every 18 months. For every new process generation the dimensions of transistors are scaled down to allow an higher level of integration. The two types of scaling strategies in practice are: full(CF) scaling, proposed by Dennard& others and constant voltage(CV)& others scaling proposed by Chatterjee. Reduction of the power dissipation is one of the most attractive features of CF scaling but it also causes sub-threshold leakage currents to grow exponentially. The CV scaling increases the drain current densities and the power density by a factor of S3.

V. SOME LEAKAGE REDUCTION TECHNIQUES

- Super cutoff Stacking
- MTCMOS Technique
- Leakage Control Transistor Approach (LECTOR)
- VLSI CMOS Leakage Reduction Approach(VCLEARIT)

A. Super Cutoff Stacking

In this approach a sleep pMOS transistor is placed in super cutoff region in parallel to the one of the stack transistors. It fullfills the requirement of high threshold of the dual threshold logic.The pMOS transistor when operated in OFF mode, draws a leakage current that can be further reduced if V_{dd} is maintained less than V_{gs}. Increase in V_{gs} of sleep transistor reduces leakages exponentially.

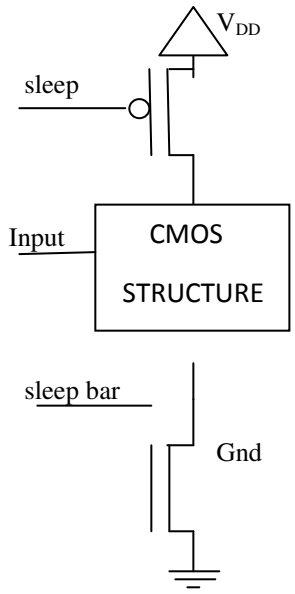


Fig.3: SCCMOS PMOS Structure

a).Stack Effect

Two series-connected off" transistors or transistor “stacks" will have lower leakage currents than those of a single off" device due to the self-reverse biasing effects. This so-called “stack effect", shown in Figure, causes the leakage current to vary with the circuit primary input vector.

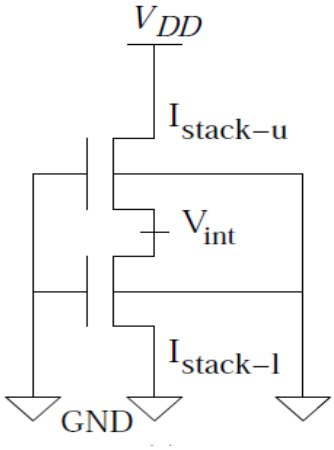


Fig. 4: Stag Effect

Therefore, special flip-flops can be inserted in the circuit to produce the input vector that provides the least amount of leakage at the primary input flip-flops. This technique can reduce leakage power at the standby mode. However, determining the input vector that minimizes the leakage current is a difficult problem due to the inherent logic correlations in the circuit. The stack effect can be extended to inserting an extra series of “off "devices into the single stack paths. This provides a moderate leakage reduction while a standard single threshold voltage technology is used.

B. MTCMOS Technique

MTCMOS is an enabling technology that provides a high speed performance and low-power operation by utilizing both high and low threshold voltage (V_T) transistors by using low V_T transistors in a signal path, the supply voltage (V_{DD}) can be lowered to reduce the switching power dissipation without affecting the performance. Although the switching power can be reduced according to the V_{DD} reduction, the V_T that has been decreased for the performance compensation leads to an exponential increase in the sub-threshold leakage current. The basic circuit scheme of the MTCMOS technique

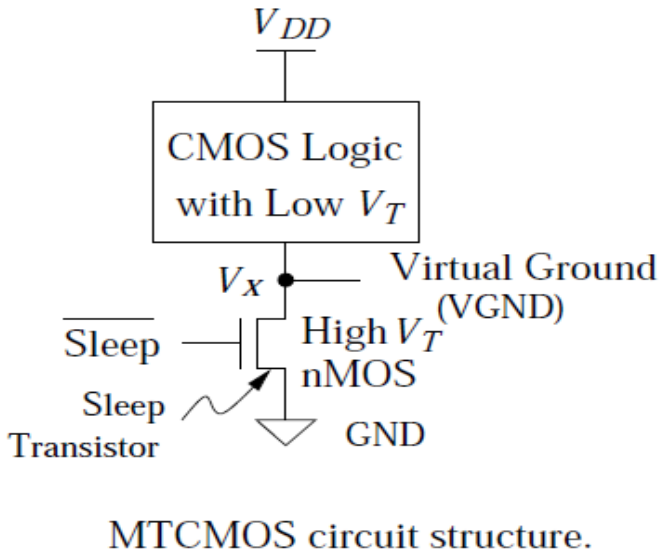


Fig.5: MTCMOS Circuit Structure.

In fact, the increased leakage power can dominate the switching power if the voltage is scaled down aggressively. In many sequential circuit applications, circuits are usually in an idle state when no computation is being performed. During this standby state, it is of no use to have a large sub-threshold leakage current. This power dissipation in the standby mode can be reduced dramatically by using high VT transistors (sleep transistors) with very low leakage currents to gate the power supply. If a portion of logic is inactive for some period of time, its leakage current maybe greatly reduced by temporarily switching it out of the power grid.

C. Leakage Control Transistor Approach

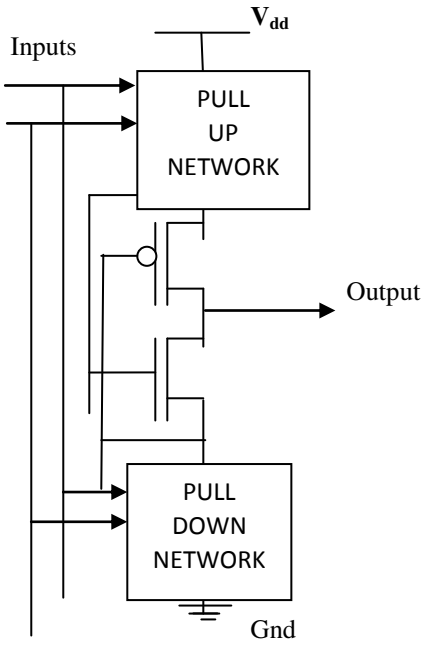


Fig. 6: LECTOR

The main ain behind this aapproach is the reduction of leakage power using the effective stacking of transistors between the paths from supply voltage to ground. In this technique two extra transistors (one PMOS and one NMOS) are introduced between pull down and pull up network. These two transistors are self controlled transistors and are called Leakage Control Transistors (LCT). The gate of each LCT is controlled by the source of other. And because of this kind of arrangement one of the LCT always remains in its near cut off region.

D. VLSI CMOS Leakage Reduction

This technique VLSI CMOS Leakage Reduction Technique(VCLEARIT) introduced the combination of one high Vt sleep transistor (P1) and two standard Vt sleep transistors (P0 and N0). In the circuit, sleep signal is '0' during active mode and '1' during standby mode. During active mode, P1 is on P0 and N0 are off. Thus the circuit operates as a conventional design. During standby mode, P1 is off and P0 and N0 are on, node N1 is connected to supply voltage and node N2 is connected to ground. Thus, the pull up network is connected across the same supply voltage and pull down network is connected across the same ground voltage thus reducing the leakage power. P1 is the leaky transistor in the design which needs to be sized appropriately match the performance with that of conventional CMOS design.

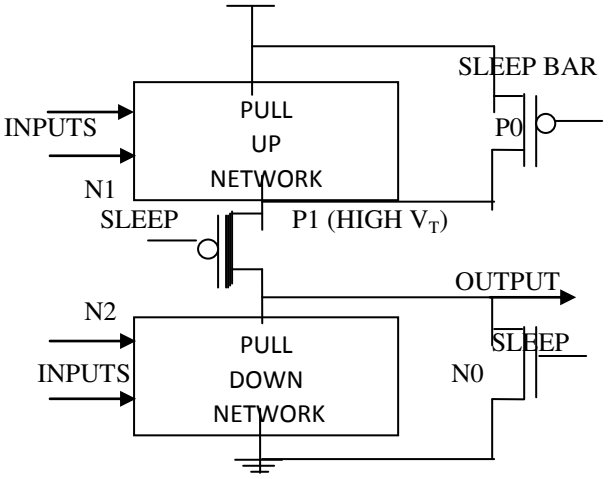


Fig. 7: VCLEARIT

a). VI.PROPOSED Work:

In the proposed work for Leakage power reduction, Performance Analysis of MTCMOS type D Flip Flop will be done. And also LECTOR and VCLEARIT that are help ful for power reduction are discussed. In low power applications area and power consumption by the device are the main technological aspects to prefer a design over the other contending designs. In this paper various literatures have studied.

To reduce leakage power in MTCMOS circuits, sleep and sleep bar transistors are operated with high threshold voltages. When sleep input is OFF and sleep bar input is ON, there is no current flow in the low threshold voltage main circuit. When sleep is ON and sleep bar is OFF then the circuit works in normal Mode

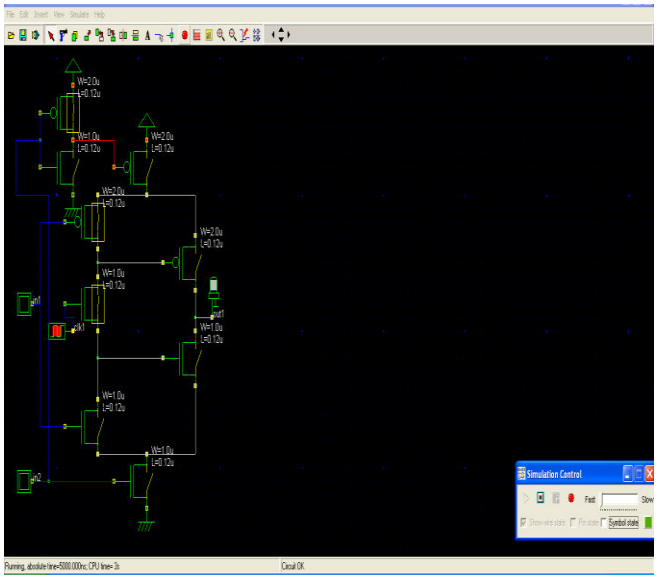


Fig. 8: Logic Circuit of a MTCMOS FLIP-FLOP using SLEEP and SLEEP BAR.

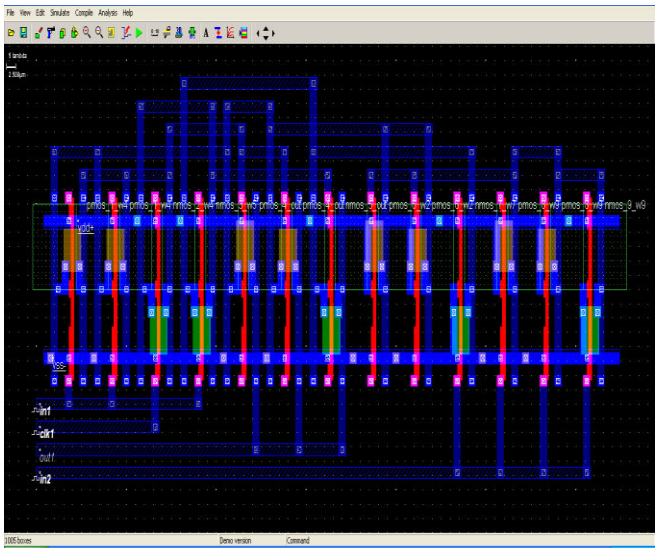


Fig. 9: Layout of MTCMOS based D Flip-Flop

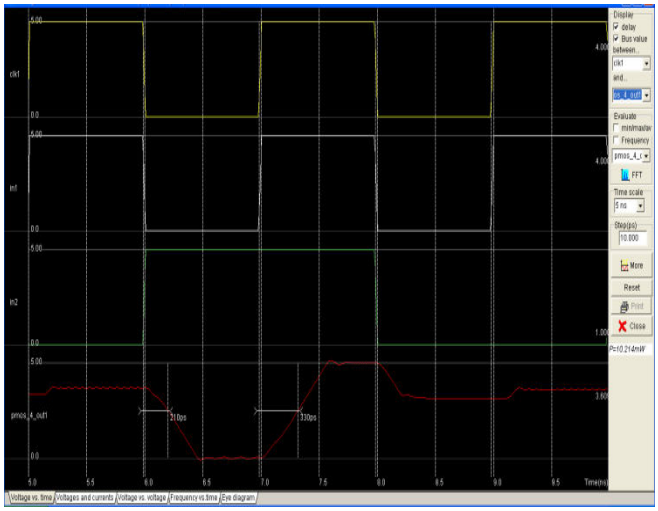


Fig. 10: Simulation Output of MTCMOS based D Flip-Flop

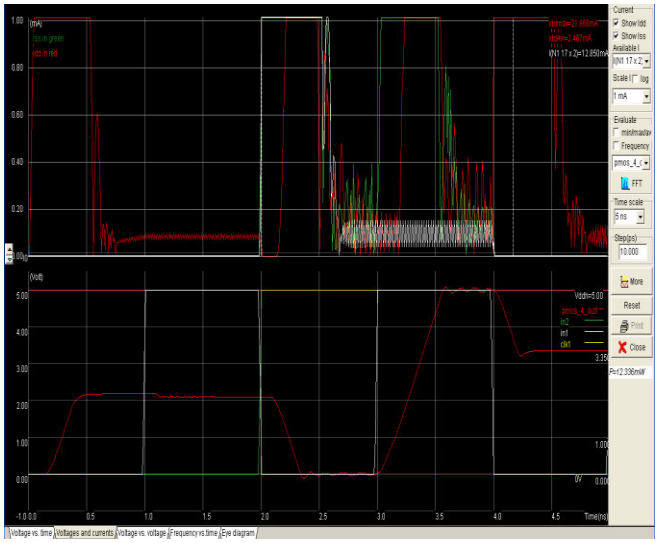


Fig.11: Simulation Results of MTCMOS based D FLIP-FLOP showing Voltage versus Current.

VI. CONCLUSION

Simulation is carried out using Microwind. From simulation results it is concluded that by applying MTCMOS leakage power minimization technique, the leakage power is minimized when technology scales down. At the same time newly emerged technologies that are discussed by Sridhara K and G S Biradar *et al.* [2] concluded that the percentage of leakage power reduction is more in VCLEARIT approach with slightly increase in the delay. LECTOR approach gives minimum leakage with minimum delay but consumes more power. Overall VCLEARIT and LECTOR approach can be consider for the design of CMOS D flip flop with lesser leakage power.

D flip flop using No.of transistors	Avg.Power consumption (μW)	Avg.Leakage power (nW)
LECTOR approach (20)	36	1.194
VCLEARIT approach (36)	16.91	0.869

Table 1.

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