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Study of Performance of Dynamic Carry Skip Adder using 22nm Strained Silicon CMOS Technology

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Abstract:-Adders are surveyed based on their delay, power and area. Most of the research in the last few years have concentrated on reducing the delay of adders and also power consumption. Carry skip adders are widely used in tree structure configuration for high speed performance. This paper analysis on speed, delay, area and temperature effect of 256 bit carry skip adder using 22nm strained silicon CMOS technology and it uses a supply voltage 0.8V. The simulation results are obtained by a HSPICE software tool. This dynamic carry skip adders consumes only 50% area compared to static CMOS technology based carry skip adders and also speed of the circuit will be increased.

Keywords:- Carry Skip Adder, High Speed Performance, Power Consumption, and CMOS Technology Etc…

I. INTRODUCTION

Adders are combinational circuits whose outputs fully depends upon the input signals. High speed adders are widely used in Digital Signal Processing ,ALU, to find the address and take indices in power chips .In this paper adders are design using Dynamic CMOS technology .In Dynamic CMOS technology less number of transistors are used compared to the Static CMOS technology (N+2 transistors are required) to design a circuits. So it occupies less area and it also increases the speed of the circuit. To design a CMOS circuit with the help of Pull up (PMOS) and Pull down(NMOS) connected in series manner .Single bit full adder circuits are connected in series it forms a Ripple Carry Adder circuits(RCA).In Ripple Carry Adder circuit output (C0) of first adder is given as the input of the next succeeding adder circuit. So it will take more time .Because of this delay will occur. Carry skip adders are used instead of Ripple Carry Adder to avoid the delay in the circuits. Delay of Carry Skip Adder is very low compared to the all other type of adder circuits. By reducing number of transistor ,it occupies less area and it consumes less power and speed of the circuit will be increased automatically. In Carry Skip Adder circuit delay fully depends upon gate delay and number of bits used . Area, power, speed and delay are important factors of to design a circuits in VLSI. Simulation results are obtained by the HSPICE software tool under the room temperature. Based upon the simulation result to show the Dynamic CMOS technology is best compared to the Static CMOS technology.

II. DYNAMIC CMOS TECHNOLOGY

Carry Skip Adder are mostly used to reduce the delay of adder circuits compared to the other adder circuits. This carry skip adder is efficient one according to its area usage and power consumption. Carry skip adders otherwise called as carry bypass adder. The most widely used technology is CMOS logic due to the advantages like low power consumption with no static power consumption. A dynamic CMOS technology are implemented by using combinations of Pull up and Pull down transistors. Pull up transistors of static CMOS circuit is replaced by single Pull up transistors in dynamic CMOS technology. The operation of all dynamic logic gates depends upon temporary of charge in parasitic node capacitance, instead of relying on steady state behavior. It require periodic clock signal in order to control charge refreshing. The capability of temporary storing a state, at a capacitive node allows us to implement very simple sequential circuits with memory functions. Common clock signals synchronize the operation of various circuit blocks. Power consumption increases with Parasitic capacitance. Therefore dynamic circuit implementation in smaller area, consumes less power than the static logic. It requires only N+2 transistor. Keeper device holds dynamic node high and source current to overcome leakages like junction leakages and sub threshold noise .Dynamic CMOS having faster switching speed because of lower load capacitance and c(in). The static power loss is very less in dynamic logic circuits.

A. Dynamic Conventional Carry Skip Adder

The schematic diagram of the conventional carry skip adder is shown in fig 1. The conventional carry skip adder consists of four full adder (ripple carry adders), four two input EX-OR gates, single four input AND gate and single 2:1 multiplexer. Here four bit conventional carry skip adder (CSKA) is designed using Dynamic CMOS technology. To

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design a single bit full adder 32 transistors are needed. For designing four bit carry skip adder (CSKA) four blocks of full adders are required. Totally 192 transistors are needed to design Dynamic Conventional Carry skip adder(DCCSA). Power consumption and area usage of the carry skip adder is very efficient. Multiple full adder circuits can be cascaded in parallel to form a N bit number of Ripple Carry Adder.RCA is logic circuit in which the output of the first full adder circuits is given as input of the next succeeding full adder circuits. So it is called as RCA. Totally 128 transistors are needed to design for four block of ripple carry adder.

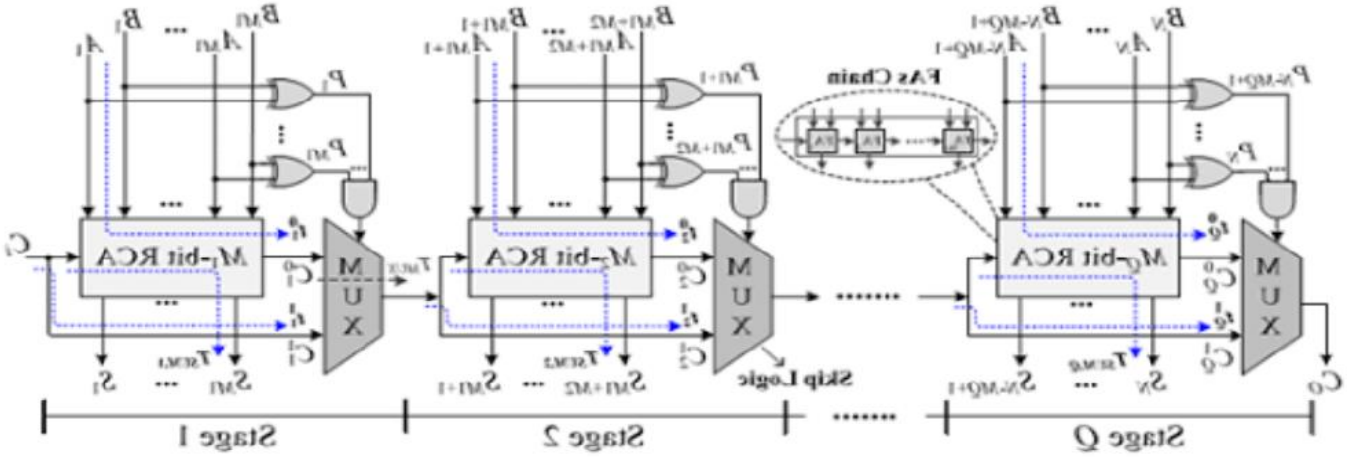

Fig -1: Schematic Diagram of Dynamic Conventional Carry Skip Adder

The function of EXOR gate is both inputs are low or if both inputs are high means the output will be zero. Otherwise the output will be one (high). EXOR gate outputs areY0,Y1,Y2,Y3. This output will be given to input of AND gate it produce the output as Po . Output of ripple carry adder(C3),input (Cin), and select line of AND gate output (Po) is given to the 2:1 multiplexer. The output of 2:1 multiplexer is calculated.

$$c_{out} = p_0.c_{in} + \overline{p_0}.c_3$$

B. Dynamic Proposed Carry Skip Adder

The schematic diagram of dynamic proposed carry skip adder circuit shown in fig- 2. The proposed dynamic carry skip adder consists of eight bit full adder circuit (RCA), four two input EXOR gate, five two input AND gate, and one two input OR gate. Here eight bit proposed dynamic carry skip adder is designed using Dynamic CMOS technology. To design a single bit full adder is 32 transistors are required. For designing eight bit carry skip adder (CSKA) eight blocks of full adder is required. Dynamic CMOS technology requires only 2+N number of transistor. So area will be reduced and also the speed of the circuit will be increased compared to the static CMOS technology. Compare to the conventional dynamic CMOS technology is better because of incrimination block is used . So only proposed Dynamic CMOS technology is preferred.

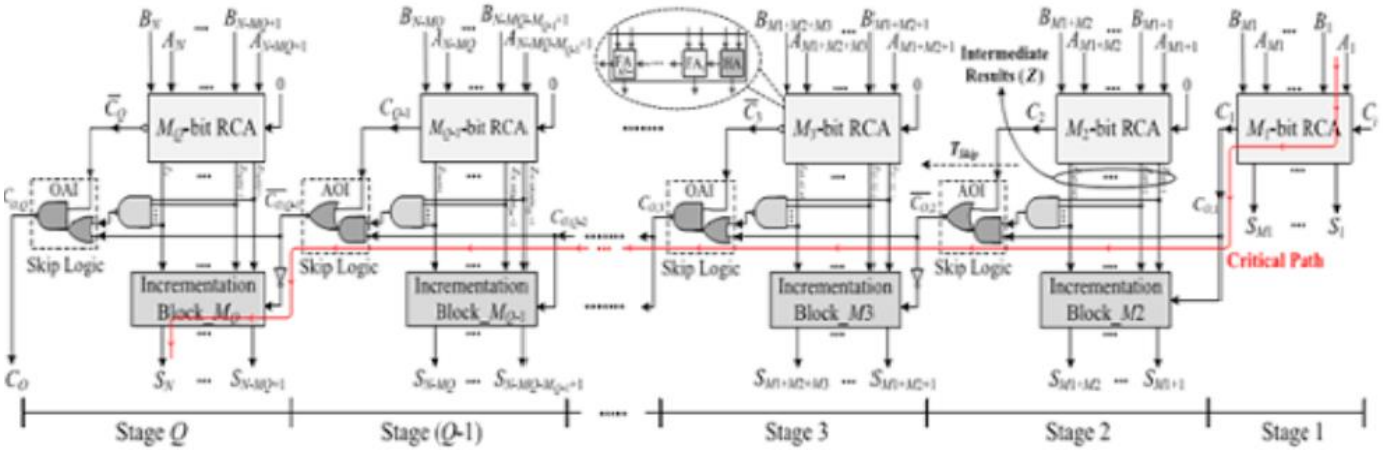

Fig-2: Schematic Diagram of Dynamic Proposed Carry Skip Adder

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III. SIMULATION AND RESULT

The simulation results obtained and also the performance of dynamic conventional and proposed carry skip adders were studied using HSPICE software tool. The circuit is built using high performance 22nm strained silicon CMOS technology. Simulation were performed at temperature of 300K. The power supply voltage used for simulation of dynamic adder voltage 0.8V. The input and output waveform of 4 bit conventional carry skip adder is shown in fig-3,4. The input and output waveform of 8 bit dynamic proposed carry skip adder is shown in fig 5,6. From fig-7,8 ,it is found that when temperature is 107(^{0}C) , the delay is 95.4pS, and the power is obtained is 30.5 micro watt. From fig -9,10 ,it is found that when the temperature is 107(^{0}C) , the delay is 4.7pS and the power is obtained is 83.4microwatt. When the temperature is increases the delay also be increases.

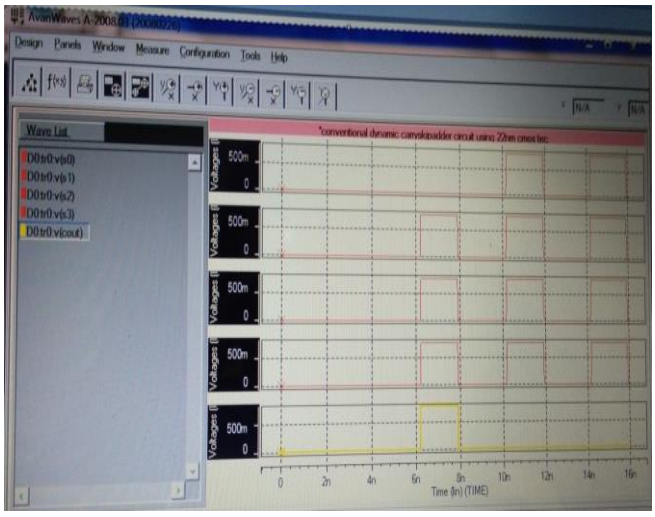

Fig-3: Input Waveform of 4bit Dynamic Conventional Carry Skip Adder

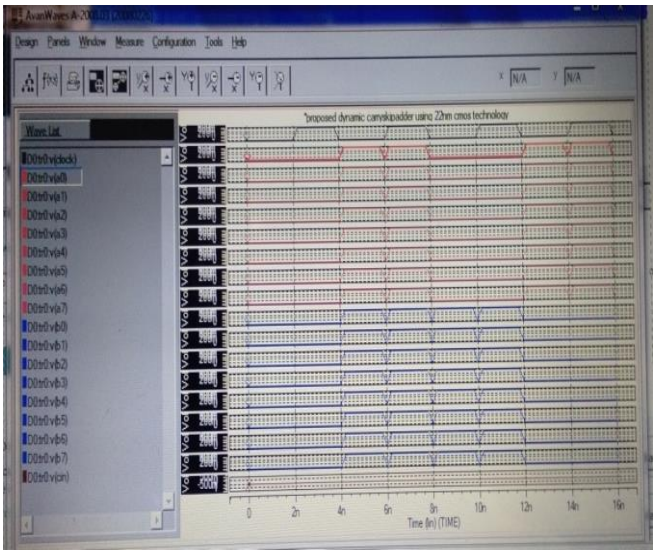

Fig-4:Output Waveform of 4 Bit Dynamic Conventional Carry Skip Adder

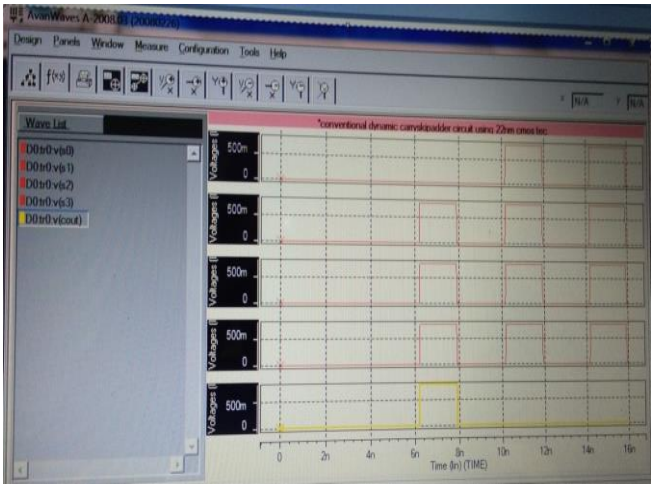

Fig-5: Input Waveform of 8bit Dynamic Proposed Carry Skip Adder

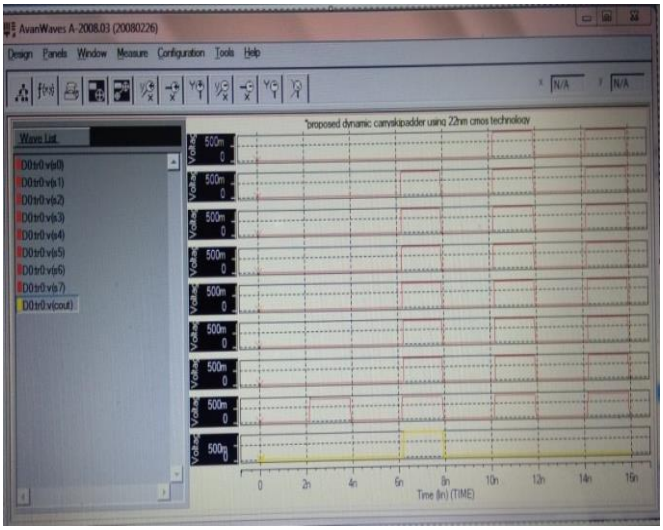

Fig-6: Output Waveform of 8bit Dynamic Proposed Carry Skip Adder

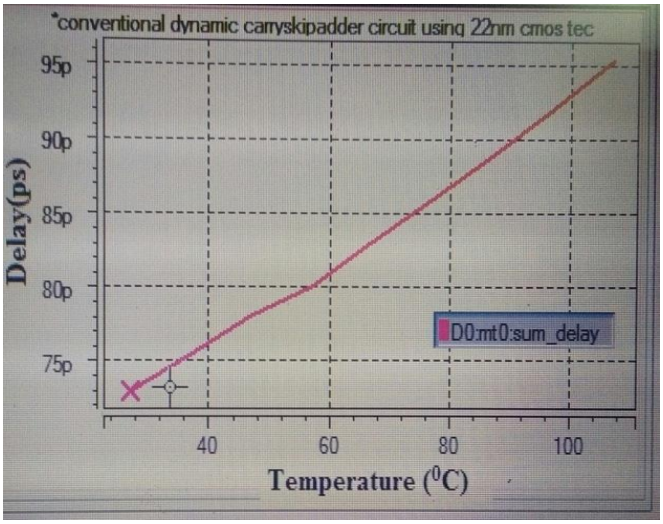

Fig-7: Delay Vs Temperature of Dynamic Conventional Carry Skip Adder

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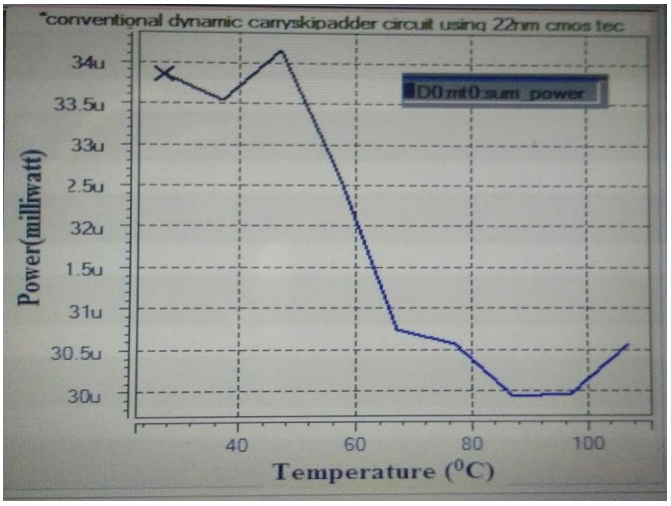

Fig-8: Power Vs Temperature of Dynamic Conventional Carry Skip Adder

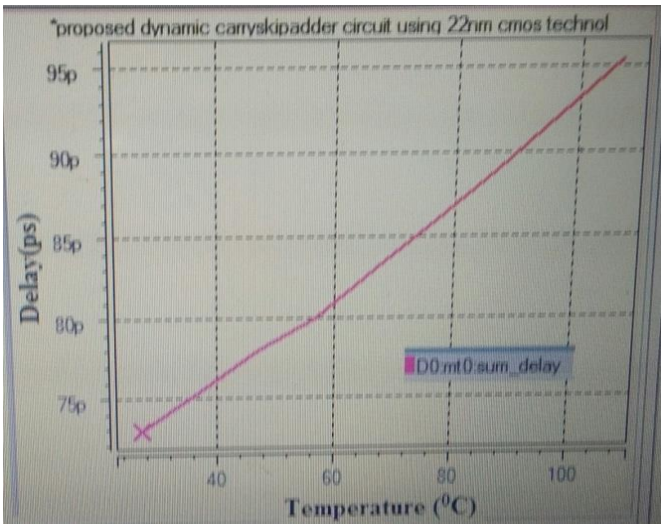

Fig-9: Delay Vs Temperature of Dynamic Proposed Carry Skip Adder

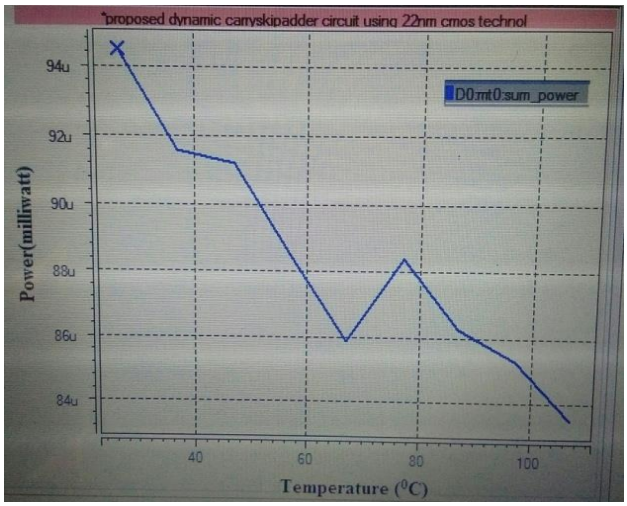

Fig-10: Power Vs Temperature of Dynamic Proposed Carry Skip Adder

Type of adders	Static conventional adder		Static proposed adder	
	Delay ((PS)	Power (micro watt)	Delay (PS)	Power (micro watt)
4BIT	101.4	45.3	_	_
8BIT	202.8	90.6	135.8	85.9
16BIT	405.6	181.2	271.6	171.8
32BIT	811.2	362.4	543.2	343.6
64BIT	1622.4	724.8	1086.4	687.2
128BIT	3244.8	1449.6	2172.8	1374.4
256BIT	6489.6	2899.2	4345.6	2748.8

Table -1: Performance of the Static Carry Skip Adder using 22nm Strained Silicon CMOS technology

Type of adders	Dynamic conventional adder		Dynamic proposed adder	
	Delay ((PS)	Power (micro watt)	Delay (PS)	Power (micro watt)
4BIT	95.4	30.5	-	-
8BIT	190.8	61	44.7	83.4
16BIT	381.8	122	89.4	166.8
32BIT	763.2	244	178.8	333.6
64BIT	1526.4	488	357.6	667.2
128BIT	3052.8	976	715.2	1334.4
256BIT	6105.6	1952	1430.4	2668.8

Table-2: Performance of Dynamic Carry Skip Adder Using 22nm Strained CMOS Technology

IV. CONCLUSIONS

In this paper we presented comparative the performance of high speed and low power analysis of carry skip adders using 22nm strained silicon CMOS technology. Dynamic CMOS technology uses supply voltage 0.8V and also it requires less number of transistors to design a256 bit carry skip adder .So, it occupies less area compared to Static CMOS technology. The dynamic architecture reduces the area of circuit by 50%compared to static CMOS technology and also speed of the circuit will be increased . The effect of temperature on the performance of dynamic adder studied using HSPICE software tool.

V. ACKNOWLEDGEMENT

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