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ADC Column-Parallel Readings for CMOS Image Sensors

N.Sindhura
Dept. of ECE
VVIT, Nambur
Guntur, India, A.P

Abstract:- The constant efforts to improve the capture and power efficiency of digital videos have resulted in a huge range of image sensor research activities over the last decade. Better lithography and solid state technologies enable the production of higher resolution image sensors. Conventional serial-read-out technology requirements follow the same curve and get harder to design, so it seems inevitable that parallelism will be used in read-out schemes to relieve the analog-read-out circuits and maintain the same capturing speed. However, this transfer requires additional parallel ADC designs, mainly related to achievable precision, area and capacity. Cyclic ADC (CADC) 12-bit column parallel readings for CMOS image sensors is present in this work. The study's aim is to cover the architectures of multiple subcomponents of the CADC and to analyze the CADC's intermediate depth. A couple of different structures of the DAC multiplying (MDAC) were revised and a first-sign CADC design is to be performed using a 1.5- bit modified MDAC flip-over. Three comparator architectures and an interpolation of dynamic sub-ADCs are introduced.

Keywords:- *12 Bit Cyclic ADC, CMOS Image Sensor, Column-Parallel Readout, MDAC, OTA.*

I. INTRODUCTION

The research aim was to search, examine and develop an algorithm for the implementation in the CMOS image sensor column, known as cyclic, ADC architecture. Enhancing image sensors with an increased resolution and frame rate makes traditional serial reading schemes difficult to design and often simply unavailable at particular readout speeds. A solution to this problem is possible by applying several parallel ADCs to loosen the speed demands of the otherwise autonomous data converter. However, in every technological problem, this solution has its advantages, disadvantages and challenges. One of the challenges in column-parallel ADCs is the narrow silicon area and the power consumption requirements. Most importantly, the low area requirements and the relatively high resolution and transformation rates achieved through this type of converter are the reasons why this study is conducted on cyclic ADCs.ADC error sources provide basic information for assessing and comparing existing devices. In some applications, ADC errors, such as gain and offset correction, can be corrected [1]. A 10-bit, 14ms/s CMOS system of pipeline ADC explained in [2]. This paper focuses exclusively upon the achievement of optical designs of power by the methodology (gm/ID). The idea is to use the biological current in this technique to control the power traffic off the op-amp cell [3]. The main architecture of the tight comparator was found to create more kickback noise from the most power efficient comparators. HSPICE comparator simulations carried out in0, 18μm technology prove their kickback noise efficiency and the charge coupled attractive devices [4, 5]. For a cyclic ADC for CMOS image sensors, the offset cancelation technique has been described. The ADC has an offset error of 1.5mv peak to peak, with a 62db SNR of 1 M. An image signal can be read at 3900 frames using the ADC array for a 256×256 pixel array [6]. The introduction of image sensors is explained in [7]. In addition, the cell provides greater flexibility in the CMOS linear trans-conductance cell than other previously proposed solutions.

THD is better than 0.3 percent for dynamic signal range ± 3v with fully differential configurations [8]. A CMOS 13-bit cyclic RSD analog to digital converter and ADC performance evolution was discussed in [9, 10]. Without the use of the matched condensers a technique of the algorithmic analog-digital transformation can be achieved at high resolution. This converter has a resolution of 12 bit and a sample rate of maximum 8 KHZ. The range is 2400 miles^2 of analog circuitry. It is estimated that the converter is built in less than 3000 miles^2 with the same technology. A higher resolution technique can be achieved with a better compensation technique [11]. For the CMOS image sensing system a low-power PGA and cyclic ADC are proposed. FPGA low capacity, amplification gain and level changer are implemented with constant input capacity. The single power-efficient op-amp is divided into different algorithmic cycles to reduce the cyclic ADC power consumption [12]. Low-power and wide-bandwidth cyclic ADC with capacitor and op- amp reuse techniques for CMOS image sensor applications discussed in [13]. The electricity consumption increases linearly in terms of speed. Use of power increases faster than this frequency and efficiency reduces. Selecting architectures parallel or pipeline can then reduce energy efficiency. Here sigma-delta technique is used to minimize power consumption [14]. A wide dynamic range CMOS image sensor with multiple exposure-time signal outputs and 12-bit column parallel cyclic analog to digital converters are discussed in [15]. A very column FPN and row temporal noise 8.9 m-Pixel, 60 fps CMOS image sensor with 14-bit column parallel ADC [16].

A ratio-independent algorithmic analog-digital converter combining current mode and dynamic techniques explained in [17].

II. ALGORITHMIC (CYCLIC) ADC

The cyclical ADC algorithm may also be called ADC pipeline evolution. It reuses one phase in principle to complete all sub-conversions. The main ADC diagram is shown in Fig 1. The message is sampled and stored for the MSB evaluation (on and on) first after the signal is flowed. The sampled initial voltage value is evaluated by the Sub-ADC, usually a 1.5-bit ADC flash compared with two thresholds. The Sub-ADC decision has been strobe by the RSD in a binary logic, which is fed further into the Sub-DAC by removing the DAC output from the fed-in voltage and solves the residual (unresolved) voltage by the sub-DAC.

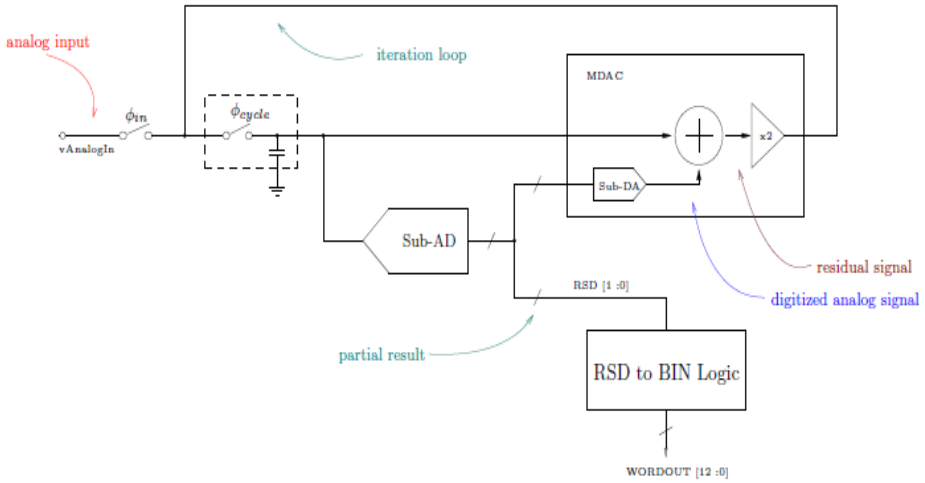

Fig 1:- A Functional Block Diagram of a RSD Cyclic ADC

For further LSB resolutions the rest has been amplified and returned. These cycles are repeated till the necessary resolution is reached. Fig 2 shows the MDAC's main schematic, which is designed around a transduction amplifier.

For applications with a small capacitance load, an OTA is a common choice because the MDAC stands behind the simplexes of an OTA circuit.

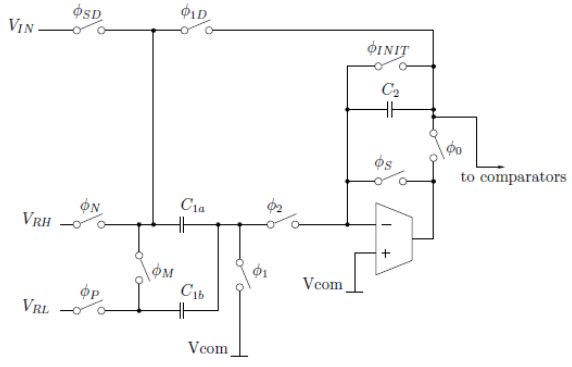

Fig 2:- Principal Schematic Diagram of the MDAC

We can examine the different sub-phases and conduct a charging redistribution analysis in order to assess the functionality of the MDAC. The four main MDAC operating modes are shown in Fig 3. Fig 3(a) before the signals are sampled; all the condensers are reset for short periods in order not to have a residual charge from prior conversions and to ensure that all conditions are equal for each CDS step. After this phase, Fig 3(b) the signal sampling may start. This means the load in the condenser is:

$$q_{1a}(t) = (Vin - Vcom + Vos)C1a \quad (1)$$

$$q_{1b}(t) = (Vin - Vcom + Vos)C1b \quad (2)$$

$$q_{2}(t) = (Vin - Vcom + Vos)C2 \quad (3)$$

During the next feedback phase, Fig 3(c), the sampled signal is amplified by two. Again, the accumulated offset will appear as a global ADC compensation for half the sample size, since condenser C2 saved offset in the previous phase and is connected during the feedback loop in the current phase, thus adding half the OTA offset. This is also possible because the amplifier is connected in the feedback loop and Fig 3(d) is the fourth phase of analog subtraction. We can write for the condenser charge during the feedback phase:

$$q_{1a}(t) = (Vo - Vcom)C1a \quad (4)$$

$$q_{2b}(t) = (Vo - Vcom)C1b \quad (5)$$

$$q_{2}(t) = (Vo - Vcom)C2 \quad (6)$$

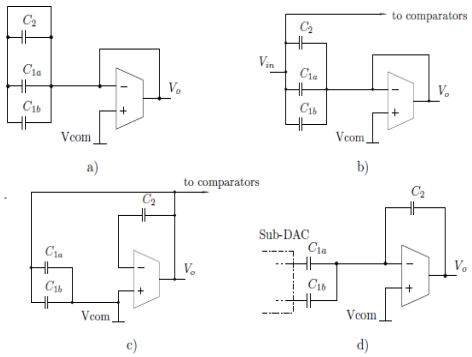

Fig 3:- Detailed MDAC Configuration for the Four Phases

➢ *Sub-AD Comparators*

The family of locked comparators can usually be split into two static and dynamic subgroups. The big noise "kickback" generated from the switch to the input is another drawback to discrete latch-based comparators. There are some benefits and disadvantages to the static locked comparator over the use of the dynamic comparator. As a column-parallel ADC's low energy consumption is vital, the low efficiency of this architecture is less attractive.

Comparing certain dynamic implementations, the architecture offers slightly better kickback noise performance and the significant disadvantage of this architecture, as also described in [5] is the increased input kickback noise. The low efficiency and relatively low speed of the static applications are a major disadvantage. The solution to the power efficiency problem appears to be dynamic implementations.

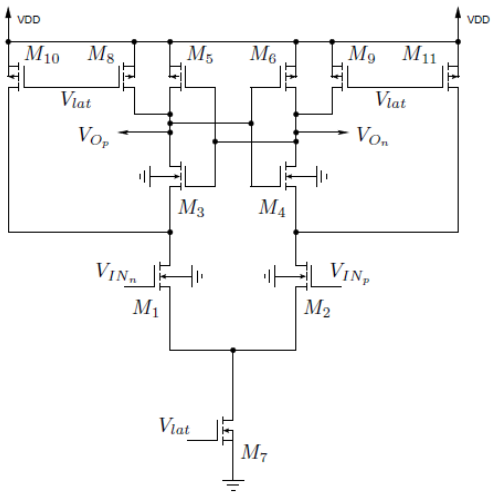

Fig 4:- A Dynamic Comparator Implementation

Two gates of the inverter are used as regeneration latch to show the dynamic implementation of the comparator. Only leakage currents via M7 contribute to total power use at this stage and the M7 transistor can be switched off completely when V $_{lat}$ is held down.M3, M5 and M4 are reset and the start-up conditions for both transistors M6, M8, M9, M10 and M11 are the same. When V $_{lat}$ is high, the M7 starts working, the M8, M9, M10 and M11 reset transistors are turned off and recovery starts. Figure 6 may have a relaxed CI effect because the M8, M9, M10 and M11 reset transistors cancel the load on the inverters to a large degree. M10 and M11 would load the M4, while M8 and M9 would load the M5 and M6. This section is intended to provide an overview of the MDAC switch study and the final decision. An overview of the clock-boosted or boot-strapped techniques will begin a short debate on the basic theory of switches. The approach and motivation for the executed size was presented with the transmission-gate switch. The Bootstrapped switch technology offers the same applicable gate overdrive voltage conditions in alternative to the clock boosted switch, for any input.

The Bootstrapped switch technology offers the same applicable gate overdrive voltage conditions in alternative to the clock boosted switch, for any input signal magnitude. The pull- out voltage is always constant, ensuring greater linearity compared to the clock boosted switch. It aims also to eliminate the serious problems of overvoltage in the boosted clock technology. A bootstrapped switch is shown [2] in Fig 5. The C $_{boot}$ condenser provides the required voltage and is moved to the gate of the transistor switch with M10 and M7 source terminals. The boot is recharged to VDD, M1 and M2 during the switch off period and is the same as the above- mentioned technological clock multiplier. The C $_{boot}$ tracking condenser must be loaded on a multi-directional basis.

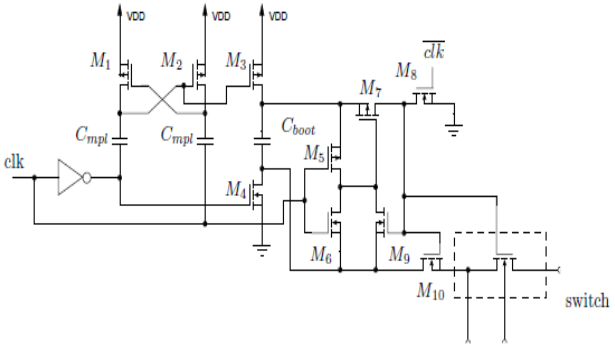

Fig 5:- A Bootstrapped Switch Implementation as Proposed By [2]

A study on the concept as a potential switch candidate was conducted and fundamental waveforms show the idea of the concepts based on the simulation are shown in Fig 6.It is easy to see that a good dynamic range of switches is provided by the bootstrapping technique, which follows both the input (source) and the output (drain). Load injected by the switch is also a disadvantage for all transistor switches. In informal, it is the same as the sample condensers used for the MDAC that are only used for clock and bootstrap multiplier. The above-mentioned disadvantages were the principal reason for the research and the focus on transmission gates as a possible solution.

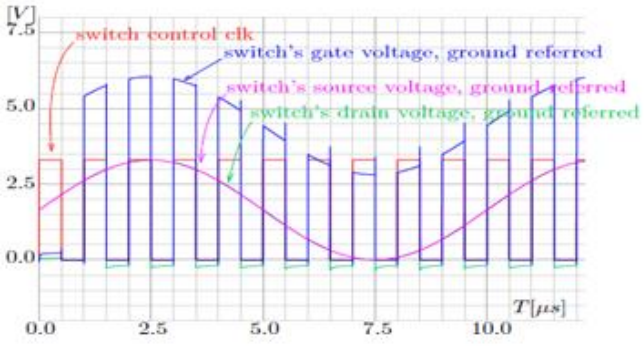

Fig 6:- The Bootstrapped Concept-A Simulated Visual Representation

III. RESULTS

Transient noise simulations were conducted in accordance with standard IEEE 1241[1], using multiple samples per code (non-histogram measurement), to estimate the converter's performance linearly. Fig 7 shows the plot of a comprehensive offset-correction non-linearity simulation based on a temporary noise simulation and 5 samples per code, meaning a maximum of 0.2 LSB INL resolutions. These results are based upon unparalleled sampling and feedback condensers for MIM should be noted.

Two clear hops can be observed on the comparator threshold voltage (code 1350 and 2500), a very common effect for 1.5-bit architectures. The current INL should in theory be invisible to the eye and more than acceptable for visual image sensing applications. The non-linearity of the differential was measured in compliance with IEEE 1241 because the integral non-linearity was based on five samples per code.

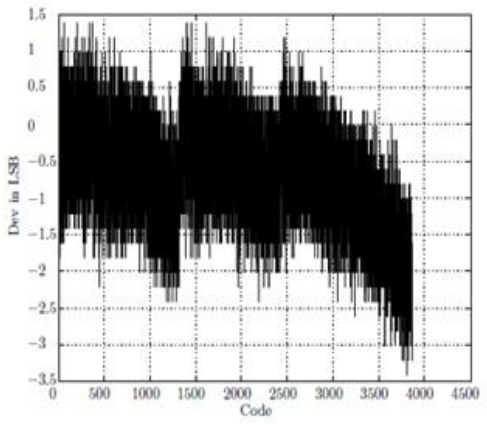

Fig 7:- Simulated Worst Case Corner Integral Non-Linearity

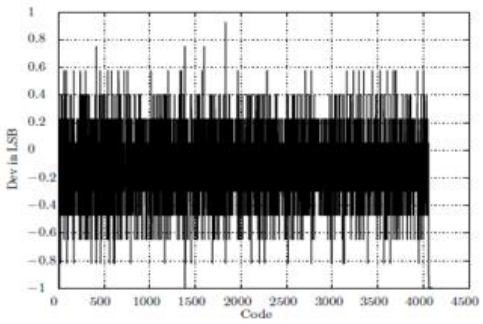

Fig 8:- Simulated Worst Case Corner Differential Non-Linearity

The differential non-linearity graph shows in Fig 8 a simulation of the worst-case transient noise corner. In some rare cases, the DNL exceeds 0.5 LSB which according to different literature sources are not completely secure. The data converter is completely monotonous. The DNL was measured at ± 0.8 LSB, but the distribution histogram of differential and integrated non-linear simulations is shown in the Fig 9 and 10 for more descriptive overviews.

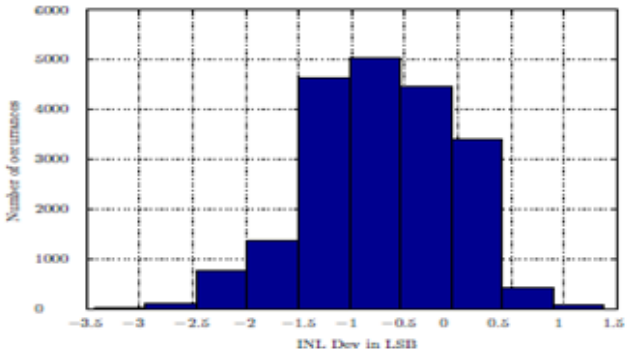

Fig 9:- Differential Non-Linearity Deviation Distribution

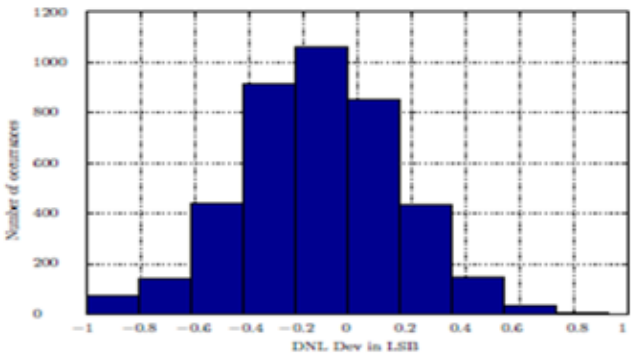

Fig 10:- Integral Non-Linearity Deviation Distribution

The maximum sampling speed is mainly associated with the maximum possible frame rate. According to the specifications, the minimum transformation speed is 130ksps. Fig 11 shows 100, 125, 150 and 166ksps conversion speeds of residual voltages adjustment. The OTA cannot be set to 12 bit accuracy after 160ksps and by lowering the clock period it seems to degrade conversion accuracy. The clocking system is a 50% duty cycle clock on a square wave.

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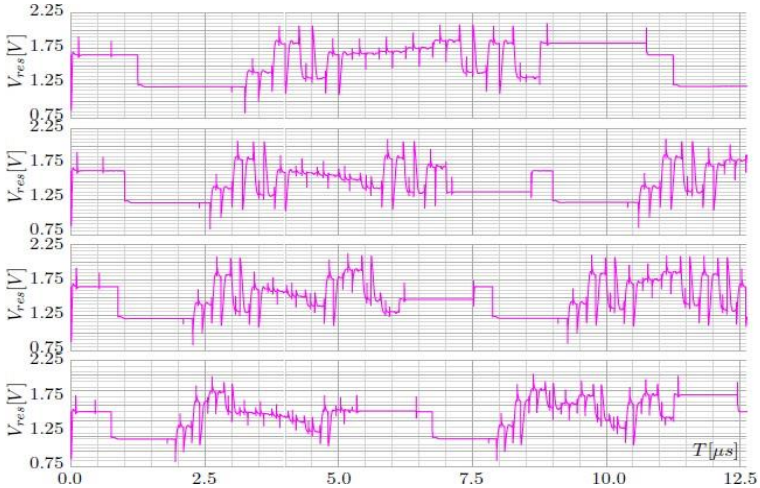

Fig 11:- Residue Voltage Settling at Conversion Speeds of 100, 125, 150 and 166ksps (From Top to Bottom) at Worst Case Corner:

Table 1 provides an overview of the converter's current status by summarizing the results for the designed conversion device. These should be taken only as indicative results, as device discrepancies, external reference tension and non-idealities do not exist in sub-AD reference generation in the current design state.

Parameter	Value	Unit
Technology	UMC 0.18μm G-02-MIXED MODE/RFCMOS18-1.8V/3.3V-1P6M	-
Resolution	14	Bits
Sampling Rate	< 152	kSps
Input Voltage Range	2	V
Integral Non-Linearity [1]	+1.8/-3.7	LSB
Differential Non-Linearity [2]	±0.6	LSB
Random Noise [3]	368	μV
Power Supply, TYP	3.5	V
Power core @ 3V3, 70 °C, TYP	74	μW
Power core+logic @ 3V3, 70 °C, TYP	194	μW
EnergyperConversionCycle@3V3,70 °C, TYP	15	μJ
Reference Voltage H	2.37	V
Reference Voltage L	1.2	V

Table 1:- Summarized Performance Results of the Designed Converters

IV. CONCLUSION

Three architectures for comparison were investigated and their advantages and disadvantages were compared with the current application. A selected interpolative dynamic Sub-AD comparator module was developed in addition to all the digital control and feedback logics in the MDAC. A couple of different structures of the DAC multiplying (MDAC) had revised and a first-sign CADC design was performed using a 1.5-bit modified MDAC flip-over. Finally, weak spot that degrade the performance of the design has been analyzed. The results achieved demonstrate that the OTA of the MDAC is the principal component of the ADC speed limitation. By following the direct precision parameters of the conversion device as an integral and differential linearity, the sampling and feedback condensers appear to be the most critical elements of its influence. Linearity of the converter the condenser mismatch reduction technologies are apparently of major importance and further study of possible techniques for condenser flipping is still a future task.

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