Adaptive Nonlinearity Estimation of Time Interleaved Analog-to-Digital Converter using Recursive Least Square Technique

Sedki Younis Computer and Information Eng. Dept. College of Electronics Engineering Ninevah University Mosul. Iraq Abdulrahman Kh. Alhafid Electrical Department College of Engineering University of Mosul Mosul, Iraq Omar Mowaffak Alsaydia Computer and Information Eng. Dept. College of Electronics Engineering Ninevah University Mosul, Iraq

Abstract:- The calibration of time interleaved analogto-digital converter (TIADC) through estimation and compensation of the channel mismatches is mandatory task to attain the required resolution of individual converters in TIADC system. This paper considers the problem of nonlinearity mismatch identification of TIADC configuration using adaptive algorithm. The adaptive recursive least square (RLS) algorithm is proposed for the estimation of nonlinearity parameters of TIADC. Simulation results demonstrated the superiority of the RLS technique for fast and accurate background estimation of polynomial nonlinearity model in TIADC system when compared with normalized least mean square (N-LMS) based adaptive estimation. The added computational complexity of the RLS is marginal due to the small-scale of the estimation problem while attaining the fast and precise estimation required for real-time realization.

Keywords:- Time Interleaved Analog-To-Digital Converter (TI-ADC), Recursive Least Square (RLS), Filters, Estimation and Compensation.

I. INTRODUCTION

Analog to Digital Converter (ADC) is an essential component in various systems including communication systems and high-speed digital signal processing applications such as micro devices, measurements and wireless sensor networks. Analog components cannot provide the required system constraints of power and cost reduction in addition to the process variations in the manufacturing phase that requires flexible design margins to maintain the chip yields high.

For example, most of the transmitter/receiver signal processing in any communication system are implemented in digital domain and represent the current trend for implementation of modern systems due many reasons just to mention, adaptability and cost. However, the ADCs are nonlinear devices and must operate in high-speed environment and provide enough dynamic range.

For advanced application with high sampling rate requirements, the using of a single channel analog-to-digital converter (ADC) may be inadequate, as sampling with the pace of the signal cannot be performed in addition to high power consumption limitations [1, 2].

In order to meet the required speed of operation for measuring and recording the signal characteristics with sufficient speed and high resolution in modern electronic systems, the time interleaved analog-to-digital converter (TIADC) is emerged as a potential approach to mitigate the current limitations of a single ADC by distributing the load across many converters. The block diagram depicted in Fig. 1 represents an ideal time-interleaved ADC with M converters each operating with sampling period of MTs and spacing of Ts between each converter where Ts is the required sampling period. The basic idea of TIADC operation is the round-robin algorithm so that the sampling rate required by each converter is reduced with a factor of M allowing for more control of the sampling accuracy and precision in addition to the overall reduction of the power consumption when compared with high-speed single channel ADC.



Fig 1:- Time-Interleaced ADC Realization with M Converter [6]

An improvement of M in the sampling rate is achieved through circulatory operation of multiple low sampling rate sub-ADCs in parallel configuration. Although the sophisticated configuration of TIADC solve some problems of single channel ADC in fast speed systems. However, a new set of problems is introduced. Attaining the upper bound performance of TIADC is limited by any channel mismatches among the individual sub-ADCs which deteriorates the performance of the TIADC converter and

ISSN No:-2456-2165

results into inaccurate sampling process. For example, the clock timing skew due to the differences in the signal path length represent a significant source of error. Although the system designers tried to solve this problem through various optimization, however the physical layout introduce unavoidable errors. Additionally, the channel mismatches such as the bandwidth mismatch, gain and offset mismatch are another source of destructing errors where significant efforts have been devoted by the researchers to deal with channel mismatch problems. Moreover, the nonlinearity mismatch resulted from the analog front-end circuitry imperfection add another mismatch with the sub-ADC. The channel nonlinearity distortion introduce additional degradation of the dynamic performance of the TIADC specifically in high-speed applications. Therefore, the calibration of TIADC mismatches is an essential operation to attain the high performance aimed with TIADC [6].

II. TIADC CALBIRATION TECHNIQUES

The TIADC calibration usually done through estimation of the mismatch or nonlinearity parameters and compensation for signal recovery. In order to mitigate the performance degradation in accuracy and dynamic range of TIADC, the correction of channel mismatch is performed either using data aided (training sequences) or non-data aided (blind) techniques. The methods that use some predefined input signals as training sequence (such as DC, ramp, sinusoidal signals) are called foreground channel mismatch estimation (calibration). On the other hand, the background estimation methods (blind estimation) rely on the intrinsic characteristics of the TIADC output signal with predefined assumption of the input signal such as oversampling, frequency spectrum nulls and wide sense stationary behavior [1].

In the literature, the problem of mismatch estimation and TIADC calibration is well studied and various methods are presented and significant efforts have been demonstrated to solve the problem. Most of the stat-of-the-art research discusses the modelling and mitigation the effect of offset, timing, frequency response and gain mismatches. Typical channel mismatches calibration techniques may not be sufficient to attain the required performance improvement; therefore, the nonlinearity mismatches should be considered to further improve the calibration process [2].

In this paper, nonlinearity mismatch problem is considered for TIADC system. The sophisticated nature of the nonlinearity operations requires advanced signal processing algorithms for the estimation of mismatch parameters. An efficient recursive-least-square (RLS) adaptive estimation algorithm is presented in this paper for fast background estimation of the nonlinearity parameters.

III. MODELLING OF NONLINEARITY MISSMATCH IN TIADC

The two-channel TIADC with nonlinearity model is depicted in Fig. 2 with overall (effective) sampling frequency of $f_s=1/T_s$. The sampling rate for each sub-ADC is $2T_s$ and both are working in an interleaved manner resulting in a phase interval of T_s . The polynomial method is used to model the nonlinearity mismatch for smooth approximation of the input nonlinearity. The nonlinear transfer characteristics for each sub-ADC $T_m(x)$ of L order is given as:

$$T_m(x) = x(t) + \sum_{l=2}^{L} C_m^l x(t)$$

Where C_m^l refers to the *l*th nonlinearity coefficient of the *m*th channel and C_m^0 is equal to one based on the assumption that offset and gain mismatch (which represents the zero order term and first order term respectively) between the channels are estimated and calibrated before ahead. By noting that the order of the nonlinearity *L* is device specific and usually depends on the specification of the system therefore, it should be specified according to the minimum value such that to attain the required performance with low computational complexity [6].



Fig 2:- Two Channel TIADC with Nonlinearity Missmatch[2]

Assuming that the sampling process does not introduce aliasing where bandlimited analog signal x(t) to Nyquist sampling frequency is considered (i.e. $X(j\omega)=0$ for $|\omega| \ge \frac{\pi}{T_s}$ where $X(j\omega)$ represents the continuous time Fourier transform of x(t)). Denoting the frequency components resulting of the *l*th nonlinearity mismatch term as $Y_n^l(e^{j\omega T_s})$, then the discrete time Fourier transform (DTFT) of the considered two-channel TIADC output can be described as

$$Y(e^{j\omega}) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} \sum_{l=0}^{L} \frac{1}{(2\pi)^{l-1}} Y_n^l(e^{j\omega T_s}) \dots \dots \dots \dots (1)$$

Where

$$Y_n^l(e^{j\omega}) = \frac{1}{2} \sum_{m=0}^{1} X^{*l}(e^{j\omega}) C_m^l e^{-jkm\pi} \dots \dots \dots (2)$$

ISSN No:-2456-2165

And $X^{*l}(e^{j\omega})$ represents the *l*-fold convolution of $X(j\omega)$

To facilitate the estimation process, the output signal of the TIADC can be represented as the desired signal $X(e^{j\omega})$ and the error signal resulted due to the *L*-order polynomial mismatch $E(e^{j\omega})$ where

$$Y(e^{j\omega}) = X(e^{j\omega}) + E(e^{j\omega}) \qquad \dots \dots (3)$$

Following the derivation presented in [2], the error signal due to the nonlinearity mismatch is given as

$$E(e^{j\omega}) = \sum_{l=2}^{L} \frac{1}{(2\pi)^{l-1}} \left(\frac{X^{*l}(e^{j\omega})C_0^l + X^{*l}(e^{j(\omega-\pi)})C_0^l}{2} + \frac{X^{*l}(e^{j\omega})C_1^l - X^{*l}(e^{j(\omega-\pi)})C_1^l}{2} \right) \dots (4)$$

Where C_0^l and C_0^l represents the *l*th polynomial component of the first and second channel respectively.

IV. RLS BASED NONLINEARITY PARAMETER ESTIMATION FOR TIADC

The estimation of nonlinearity parameter is basically based on the input free band principle where only the distortion signal due to the nonlinearity mismatch is existed. Coinciding with the common practice of transition bands of digital filter, a slight oversampling should be employed. A generic block diagram for the nonlinearity parameter estimation algorithm of TIADC used in this paper is shown in Fig. 3.



Fig 3:- Block Diagram of the RLS Based Nonlinearity Estimation for TIADC

The output of the TIADC is the input to the nonlinearity distortion extraction unit where a high pass digital filter of impulse response (*h*) is adopted to extract the distortion signal in the input free band region as shown in Fig. 4 (a). The output of the nonlinearity distortion extraction (high pass digital filter) denoted as $e_d(n)$.

The error signal due to the nonlinearity mismatch given in equation (4) can be reformulated as

$$E(e^{j\omega}) = \sum_{l=2}^{L} \frac{1}{(2\pi)^{l-1}} (X^{*l}(e^{j\omega})S_l + X^{*l}(e^{j(\omega-\pi)})D_l) \qquad \dots (5)$$

Where

$$S_l = \frac{1}{2} (C_0^l + C_1^l) \qquad \dots (6)$$

And

$$D_l = \frac{1}{2} (C_0^l - C_1^l) \qquad \dots (7)$$

For real time implementation of the estimation procedure, a time domain processing is preferable. Therefore, the vector form of the equation given (5) in the time domain based on the assumption that $y(n) \approx x(n)$ (i.e. blind estimator, the input signal x(n) is not available) can be given as

$$e(n) \approx S(Y_y) * h + D(Y_y(-1)^n) * h \dots \dots (8)$$

Where

$$S = \begin{bmatrix} S_2 & S_3 & \dots & S_L \end{bmatrix} \qquad \dots \dots (9)$$

$$D = \begin{bmatrix} S_2 & S_3 & \dots & S_L \end{bmatrix} \qquad \dots \dots (10)$$

And

$$Y_x = [y^2(n) \ y^3(n) \ \dots \ y^L(n)]^T \ \dots \ (11)$$



Fig 4:- (a) Nonlinearity Distortion Error Extraction (b) Nonlinearity Error Prediction Model

The approximation given in equation (8) for the error signal is used as a prediction model for the nonlinearity error as shown in Fig. 4 (b) where the nonlinearity coefficients given in (9) and (10) are adjusted using recursive least square adaptive algorithm as follows

1

$$e(n) = e_d(n) - \hat{e}_d(n)$$
(12)

$$g(n) = P(n-1)y(n)\{\lambda + y^{T}(n)P(n-1)y(n)\}^{-1} \qquad \dots \dots (13)$$

$$P(n) = \lambda^{-1} P(n-1) - g(n) y^T(n) \lambda^{-1} P(n-1) \dots \dots (14)$$

$$\tilde{S}_l(n) = \tilde{S}_l(n-1) + e(n)g(n) \qquad \dots (15)$$

Where λ is the forgetting factor and $P(0) = \delta I$ where *I* is the identity matrix and δ is initialization value.

V. SIMULATION RESULTS

The performance of nonlinearity estimation algorithm presented in this paper is evaluated through simulation. Two-channel TIADC with third order polynomial nonlinearity transfer characteristics is modeled in MATLAB. The polynomial coefficients of the TIADC are selected as $C_0 = [1, -0.001, 0.0035]$ and $C_1 = [1, 0.0020, -0.0015]$, respectively, which are within the typical range given in [5]. For nonlinearity distortion extraction, digital FIR is designed with 0.8π starting passband frequency with equi-ripple and linear phase characteristics as shown in Fig. 5. In addition, 20% of oversampling of the input signal is maintained throughout the simulation.



Fig 5:- High Pass Filter Magnitude Response used in the Simulation

The adaptive RLS algorithm initialized with the following parameters: forgetting factor λ =0.999 and regularization parameter δ =0.1. The convergence curve of the estimated nonlinearity parameters is shown in Fig. 5. It is obvious that few hundred samples are needed for the adaptive algorithm to converge to the actual values. In addition, the nonlinearity parameters are settled with stable operation for the adaptive system.



Fig 5:- The Estimated Nonlinearity Parameters Versus Time (Sample Index)

The performance of the RLS based estimation is compared with the Normalized Least Mean Square (N-LMS) based estimation presented in [1] in terms of mean square error (MSE) of the overall estimated parameters. It is clear that the RLS based estimation provides fast estimation when compared with N-LMS based estimation. The MSE of the estimated parameters falls down to less than 10⁻³ after few hundered samples while N-LMS requires more than 10⁴ samples to reach the same MSE of 10⁻³.



Fig 6:- The MSE versus Time (Sample Index)

VI. CONCLUSIONS

Nonlinearity mismatches estimation problem in TIADC system is considered. An adaptive blind (background) estimation for the nonlinearity parameters is formulated using RLS technique. Simulation results for the two-channel TIADC illustrated that fast convergence, stable operation and accurate estimation can be obtained using the adaptive RLS scheme. The accuracy and convergence is tested in terms of MSE and the proposed scheme showed its superiority when compared with N-LMS. In addition, the added complexity is marginal because small scale of the estimation problem. Therefore, it can be considered for real time implementation.

REFERENCES

- [1]. Yinan Wang, Håkan Johansson and Hui X.: 'Adaptive Background Estimation for Static Nonlinearity Mismatches in Two-Channel TIADCs', IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 62, NO. 3, MARCH 2015.
- [2]. V. Divi and G. W. Wornell, "Blind Calibration of Timing Skew in Time-Interleaved Analog-to-Digital Converters," in *IEEE Journal of Selected Topics in Signal Processing*, vol. 3, no. 3, pp. 509-522, June 2009.
- [3]. Jyoti Dhiman, Shadab Ahmad, Kuldeep Guliai: 'Comparison between Adaptive filter Algorithms (LMS, NLMS and RLS)', International Journal of Science, Engineering and Technology Research (IJSETR) Volume 2, Issue 5, May 2013.
- [4]. Yinan Wang, Håkan Johansson, Hui Xu and Zhaolin Sun.: 'Joint Blind Calibration for Mixed Mismatches in Two-Channel Time-Interleaved ADCs', IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-I: REGULAR PAPERS, VOL.62, NO.6, JUNE 2015
- [5]. Yinan Wanga, Hui Xua, Håkan Johanssonb, Zhaolin Suna and J. Jacob Wiknerc: 'Digital estimation and compensation method for nonlinearity mismatches in time-interleaved analog-to-digital converters', Digital Signal Processing 41 (2015) 130–141.
- [6]. K. M. Tsui and S. C. Chan: 'A Novel Iterative Structure for Online Calibration of M-Channel Time-Interleaved ADCs', IEEE TRANSACTIONS ON INSTRUMENTATION AND MEASUREMENT, VOL. 63, NO. 2, FEBRUARY 2014.
- [7]. Li, J.; Pan, J.; Zhang, Y. Automatic Calibration Method of Channel Mismatches for Wideband TI-ADC System. Electronics 2019, 8, 56.