

UVT and PQ Theory based Generalised Unified Power Quality Conditioner for Voltage Sag and Swell Compensation

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Abstract:- Power quality has been a big problem for both energy suppliers and their consumers. For consumers, the economic effects of power disturbances will vary from few hundred dollars for the restoration or removal of home equipment to millions of dollars for the lack of manufacturing and cleaning. In the case of services, system failures will lead to consumer frustration, loading and income losses. Generalised unified power quality conditioner (GUPQC) is the modern custom power device which deals with voltage and current imperfections simultaneously in three bus or feeder distribution systems. This paper presents modelling, analysis and simulation of GUPQC consisting of one Distribution static compensator (DSTATCOM) and two Dynamic voltage restorer (DVR) has been made to compensate the first feeder current imperfections and second & third bus voltage imperfections. Instantaneous active and reactive theory (PQ) based control strategy is used for DSTATCOM and Unit vector template theory based control strategy is used for DVR. The results obtained in SIMULINK on a three bus or feeder distribution systems show the effectiveness of the proposed configuration.

Keywords:- Power Quality, Generalised Unified Power Quality Conditioner (GUPQC), Unit Vector Template (UVT), Instantaneous Active And Reactive Theory (PQ), Distribution Static Compensator (DSTATCOM), And Dynamic Voltage Restorer (DVR).

I. INTRODUCTION

In the present complex electronics environment numerous issues can happen due to poor power quality. Along with this, it has gotten important to furnish a powerful arrangement with more prominent level of exactness just as with quick speed of response. Active filtering compensation has proved the best strategy for reducing enormous power quality issues [1]. So as to alleviate the power quality aggravations and to give altered arrangements [2-3], newer gadgets dependent on power electronics hardware called "custom power devices", have been created. Current solutions for load related issues and supply voltage problems can be addressed by unified power quality conditioner (UPQC) [4-5]. It is obtained by consolidating DSTATCOM and DVR to give a solution for different power quality

issues. The DSTATCOM improves the current profile and the DVR improves the voltage profile.

A universal active power line conditioner, a universal power quality conditioning system and a universal active filter can also be referred to as UPQC. It is an Active Power Filter (APF) series cascade connection and shunt connected by a standard DC connection capacitor [6]. By means of a series transformer, the DVR is connected in series to the supply line. The DVR prohibits disturbances of the source side voltage from reaching the load side to generate the load voltage at the desired magnitude and frequency [7].

Whereas DSTATCOM is connected parallel to the load, it reduces the current problems associated with the load side to make the source current purely sinusoidal [8]. Interline dynamic voltage restorer (IDVR)[9-10], interline voltage controller (IVOLCON)[11-12], IUPQC with two VSCs[13] are some of the custom interline power units. As seen in Figure-1, the generalised unified power quality conditioner[14] can be used to secure the equipment and other operating devices in the three bus /feeder distribution system.

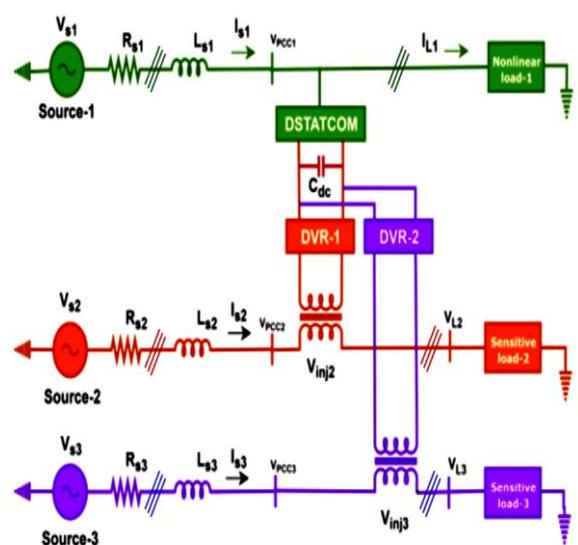


Figure-1: Generalised Unified Power Quality Conditioner

II. CONTROL STRATEGY OF DVR

Unit vector template based algorithm is used to control the DVR. Unit vector template (UVT) as proposed in [15] is used as the control technique of the series APF sequence. The distorted supply is used to extract the UVT. The Figure-2, shows the method of extraction. In order to achieve this, the DVR insert voltages opposite to the source voltages distortion and/or unbalance present and these voltages cancel each other, resulting in a balanced and required voltage on the load side supply voltages. UVT control strategy is used to obtain the load reference voltage, which is compared with load voltage signals. The error obtained from the above is fed to the hysteresis controller. The hysteresis controller will produce necessary gating signal required for the series inverter as shown in below figure-2. The control strategy used for the hysteresis controller is defined in [16] had been used. Pattern of switching the inverters will be specified by the hysteresis band controller. In the extraction of error signal, the hysteresis controller places a vital role. The error signal obtained from the comparison of the load side reference voltage and the instantaneous load side voltage signals.

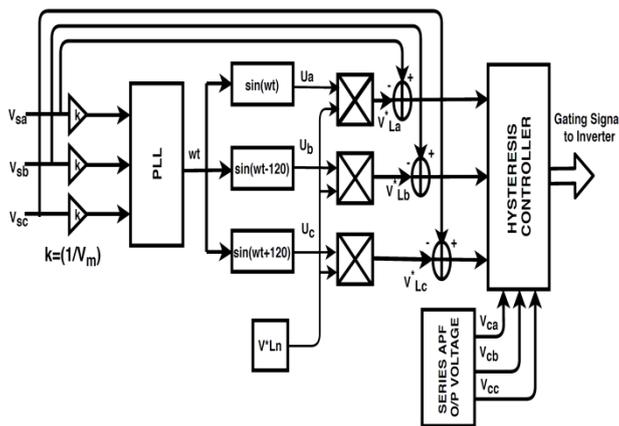


Figure-2: UVT Control Strategy of Dynamic voltage restorer

III. CONTROL STRATEGY OF DSTATCOM

In order to generate required compensating signal for DSTATCOM, p-q theory is used which shown in figure-3. The equations (1) and (2) are used to translate to the α-β-0 coordinates from the three phase voltages and currents [17].

$$\begin{bmatrix} V_{in_0} \\ V_{in_\alpha} \\ V_{in_\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{in_a} \\ V_{in_b} \\ V_{in_c} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} i_{in_0} \\ i_{in_\alpha} \\ i_{in_\beta} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{in_a} \\ i_{in_b} \\ i_{in_c} \end{bmatrix} \quad (2)$$

The active power (Ps), reactive power (qs) and the zero sequence components drawn by the load are obtained from equation (3). Immediately the theoretical and actual powers are calculated. The presence of oscillating and average components in the instantaneous power can be indicated in the equation (4).

$$\begin{bmatrix} P_0 \\ P_s \\ q_s \end{bmatrix} = \begin{bmatrix} V_{in_0} & 0 & 0 \\ 0 & V_{in_\alpha} & V_{in_\beta} \\ 0 & -V_{in_\beta} & V_{in_\alpha} \end{bmatrix} \begin{bmatrix} i_0 \\ i_{in_\alpha} \\ i_{in_\beta} \end{bmatrix} \quad (3)$$

$$p_s = \bar{p}_s + \tilde{p}_s ; q_s = \bar{q}_s + \tilde{q}_s \quad (4)$$

Where \bar{p}_s direct component of active power; \tilde{p}_s is a fluctuating component of active power; \bar{q}_s is a direct component of reactive power; \tilde{q}_s is a fluctuating component of reactive power. Complete reactive power (q_s) and the fluctuating portion of active power are chosen as power comparisons and current comparisons and are used to compensate for harmonic and reactive power by using equation (5). There will be no zero sequencing power (p_0) as the load is called balanced.

$$\begin{bmatrix} i_{Co\alpha}^* \\ i_{Co\beta}^* \end{bmatrix} = \frac{1}{V_{in_\alpha}^2 + V_{in_\beta}^2} \begin{bmatrix} V_{in_\alpha} & -V_{in_\beta} \\ V_{in_\beta} & V_{in_\alpha} \end{bmatrix} \begin{bmatrix} -\tilde{p}_s + \bar{P}_{loss} \\ -q_s \end{bmatrix} \quad (5)$$

\bar{P}_{loss} is the signal obtained from the voltage regulator, which is used as average real power [18]. This can also be defined as active power corresponding to the switching and resistive losses of the UPQC [19]. The PI controller connected in the voltage control loop processes the error signal by comparing the DC-link capacitor voltage with the reference value. It minimises the steady state error of the voltage through DC link capacitor. The compensating currents ($i_{Co\alpha}^*, i_{Co\beta}^*$) needed to satisfy the load demand for power are seen in equation (5). These currents are shown in the α-β coordinates. Equation (6) is used to obtain the required phase current ($i_{Coa}^*, i_{Cob}^*, i_{Coc}^*$) needed for mitigation. These phase currents are reflected in the a-b-c axis obtained from the mitigation current in the α-β coordinates.

$$\begin{bmatrix} i_{Coa}^* \\ i_{Cob}^* \\ i_{Coc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{Co\alpha}^* \\ i_{Co\beta}^* \end{bmatrix} \quad (6)$$

Figure-3, shows the p-q theory is suitable for ideal 3-phase systems and not suitable for main voltages which are non-ideal [20]. $V_{in_\alpha}^2 + V_{in_\beta}^2$ is not constant and current & voltage harmonics are inserted into instant active and reactive powers in the non-ideal voltage condition's. Due to this compensation current equal to the current harmonics is not possible to produce from the DSTATCOM. In order to overcome these restrictions, the instantaneous active and reactive powers are calculated after the supply voltages are filtered. Figure-4, shows the voltage harmonic filter. The Park transformation is used to transform the instantaneous voltage into d-q coordinates as shown in equation (7).

$$\begin{bmatrix} V_{in,d} \\ V_{in,q} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} V_{in,a} \\ V_{in,b} \\ V_{in,c} \end{bmatrix} \quad (7)$$

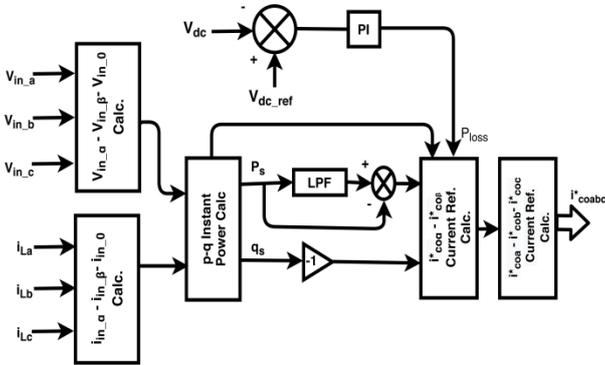


Figure-3: Control block diagram of shunt APF

The d-q voltage influences are filters by the 5th order low pass filter with a cut-off frequency of 50 Hz. The equation (8), gives the α - β coordinates obtained from the filtered components. The non-ideal supply voltages are transformed to a sinusoidal shape using LPF in d-q coordinates.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \sin(\omega t) & \cos(\omega t) \\ -\cos(\omega t) & \sin(\omega t) \end{bmatrix} \begin{bmatrix} V_{in,d} \\ V_{in,q} \end{bmatrix} \quad (8)$$

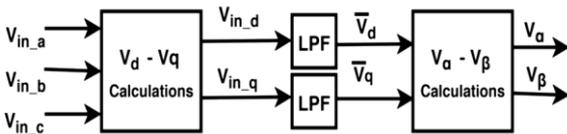


Figure-4: Voltage harmonic filtering block diagram

The p-q control algorithm is used to obtain the reference currents, which in turn will be converted in to the switching strategies for inverter in the shunt compensator. The reference and instantaneous currents are compared. After the comparison the resultant obtained will be fed to the hysteresis of the PWM band which generate the necessary voltage source inverter switching pattern. The resultant obtained is the error signal between the reference and injected current of the DSTATCOM.

IV. GUPQC COMPENSATION PERFORMANCE

Harmonics are not desired in almost all distribution systems components because they have a hostile effect on the transformer output, rotating electrical machines and end user devices. Not only this presence of harmonics in the distribution system there performance and working characteristics of the measuring devices and protective instrument will change. Due to all these reasons, harmonics compensation or reduction in the distribution is very much essential. The below four simulation case studies are demonstrated to show the GUPQC performance. In these studies, mitigation of voltage harmonics, sag and/or swell in

the bus-2 and bus-3 and distorted current generated due to non-linear loads in the bus-1 are demonstrated.

V. CASE STUDY-1: VOLTAGE AND CURRENT HARMONIC COMPENSATIONS

The load-1 was consist of combination of linear (unbalanced RL-load) and non-linear loads (three-phase diode bridge rectifier accompanied by DC-side RL load), load current-1 (I_{L1}) consists of two components, non-active current component (due to linear load) plus harmonic components (non-linear load). Fig. 5 (a) shows highly distorted load current due to this source currents distortion is avoided by shunt compensator at $t=0$ sec as shown in Fig.5(b). Consequently, the source current retains as balanced and sinusoidal as seen in Fig. 5(c).

Figure-6 shows the load current total harmonics distortion which is about 12.12%, this distortion will come back to the source and cause serious problems to all other components. Due to DSTATCOM has which will reduce the THD to 2.69% as per IEEE 519 standards and also prevent the current flowing into the bus-1's source side. That, in turn makes the others users connected to the same bus.

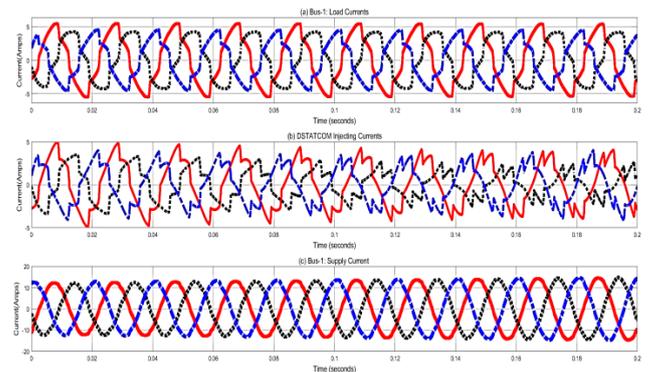


Figure 5: Current harmonic compensations at bus-1 (a) Load currents, (b) DSTATCOM injecting currents and (c) Supply currents

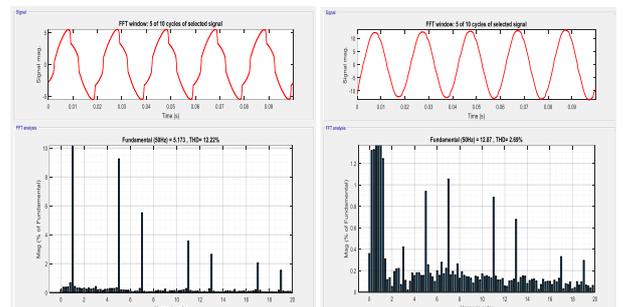


Fig. 6: THD spectrum of the load and source current of bus-1

In order to show the performance of GUPQC, source voltages at bus-2 and bus-3 are distorted. The 20% magnitude of 3rd harmonic at bus-2 and 10% magnitude of 5th harmonic are introduced. The DVR-1 and DVR-2 at their respective busses will compensate these source side voltage distortions.

Figure-7(a) to (c) and Figure-8(a) to (c) shows the three phase source, compensation and load voltages of bus-2 and bus-3 respectively. Due to presence of harmonics at source side of bus-2, which is shown in Fig. 7(a), GUPQC's DVR-1 in bus-2 came in to operation at time t=0 sec as shown in Fig. 7(b). As a result, bus-2 load side voltages are observed to be sinusoidal, as shown in Fig. 7(c).

Similarly, due to presence of harmonics at source side of bus-3, this is shown in Fig. 8(a), GUPQC's DVR-2 in bus-3 came in to operation at time t=0 sec as shown in Fig. 8(b). As a result, bus-2 load side voltages are observed to be sinusoidal, as shown in Fig. 8(c).

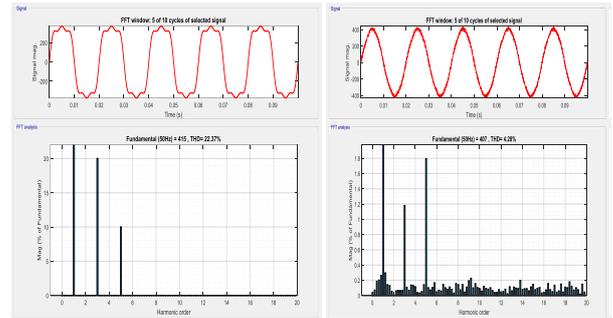


Fig. 10: THD spectrum of the source and load voltage of bus-3

The performance of GUPQC series compensations can be seen in Figure-9 and 10 to improve the frequency spectrum and reduce the load side voltage after the mitigation is clearly demonstrated. The THD values of source voltages at bus-2 and bus-3 is 22.36% and 22.37%. These THD values are reduced to 4.12% and 4.28% at load side voltages at their respective buses.

VI. CASE STUDY-2: SAG AND VOLTAGE HARMONICS COMPENSATION AT BUS-2 & 3

Today, end customers of distribution networks are affected by supply systems disturbances due to variations of supply voltages and current harmonics generated from nonlinear loads, which will propagate to the supply from load. Depending on the variation duration in terms rise and the fall in voltage amplitude, the variations may be categorized as voltage sag / swell, interruptions, under voltage and over-voltage. Power engineers very much concerned in locating and identifying the source of disturbance with voltage sag and swell in the utilities of the distribution network and end customers. In order to mitigate these, they need an immediate suitable solution.

In order to check the GUPQC compensation ability in terms of mitigating the voltage sag and harmonics. At bus-2, source voltages are disturbed by inserting 20 % magnitude 3rd harmonic and 10% magnitude 5th harmonic during the time intervals from t=0.05 sec to t=0.15 sec with voltage sags of 30% nominal supply side voltage values as shown in Fig. 11 (a) to (c). Similarly at bus-3, source voltages are disturbed by inserting 20 % magnitude 3rd harmonic and 10% magnitude 5th harmonic during the time intervals from t=0.05 sec to t=0.15 sec with voltage sags of 20% nominal supply side voltage values as shown in and Fig. 12 (a) and (c).

Due to disturbance in the bus-2, DVR-1 immediately comes into operation as shown in Fig 11 (b), instantly when voltage sag was initiated, harmonic and the in-phase sag components both are compensated by the series compensator. Fig. 11 (c), shows the voltages of load side, which are restored to the required sinusoidal value, by DVR-1 due to supply voltage distortions in terms of voltage harmonics and sag. Similarly, disturbance in the bus-3, DVR-2 immediately comes into operation as shown in Fig 12 (b), instantly when voltage sag was initiated, harmonic and the in-phase sag components both are compensated by

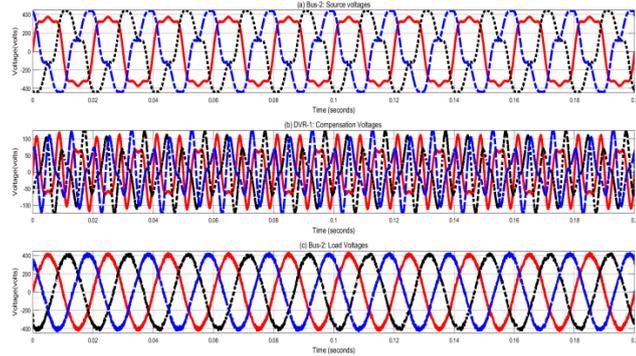


Figure 7: Voltage harmonic compensations at bus-2 (a) Source voltages, (b) DVR-1 compensation voltages and (c) Load voltages

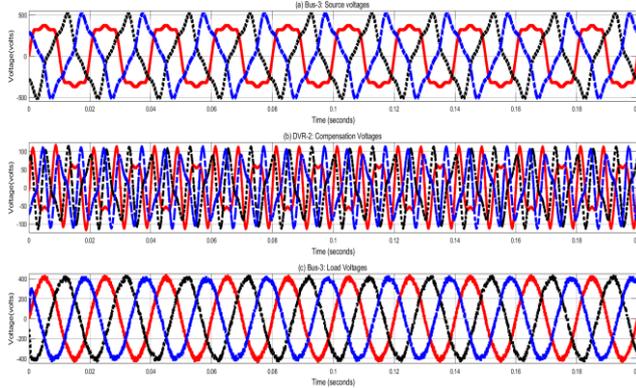


Figure 8: Voltage harmonic compensations at bus-3 (a) Source voltages, (b) DVR-2 compensation voltages and (c) Load voltages

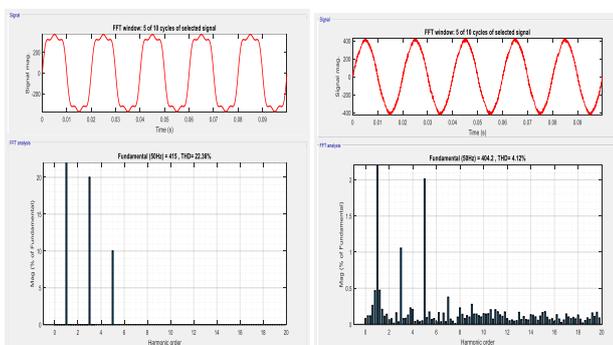


Fig. 9: THD spectrum of the source and load voltage of bus-2

the series compensator. Fig. 12 (c), shows the voltages of load side, which are restored to the required sinusoidal value, by DVR-2 due to supply voltage distortions in terms of voltage harmonics and sag.

From the above case study, the compensation performance of GUPQC, in mitigation of voltage sag and the injection of the desired voltage have been clearly shown. DC-link capacitor voltage needs to be maintained stable during the voltage sag. The required voltage to maintain stable can be done by suitable effective control strategy. As predicted, the deviations in the supply side voltages and the voltage sag of the two buses were balanced by the GUPQC's excellent compensating characteristics on the basis of the new controller scheme. The effect of the voltage sag on bus-2 and bus-3 on customers is mentioned table-1.

Table 1: Measured voltages of GUPQC during voltage harmonics and Sag

Bus	Condition	Source Voltage	Injecting Voltage	Load Voltage
2	SAG 30	248	184	412
3	SAG 20	287	138	411

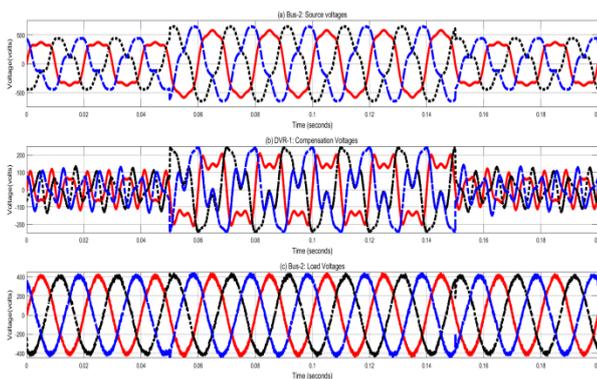


Figure 11: Voltage harmonic and sag compensations bus-2 (a) Source voltages, (b) DVR-1 compensation voltages and (c) Load voltages

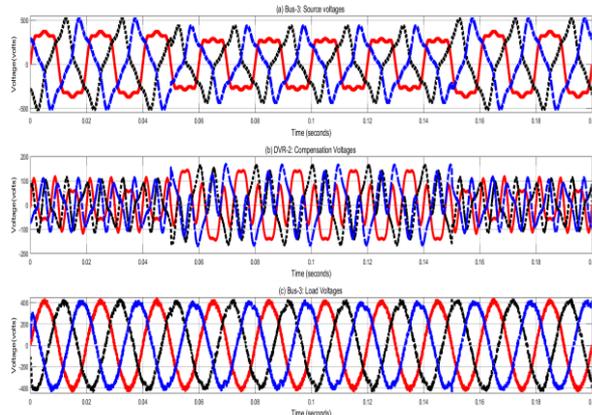


Figure 12: Voltage harmonic and sag compensations bus-3 (a) Source voltages, (b) DVR-2 compensation voltages and (c) Load voltages

VII. VOLTAGE HARMONICS AND VOLTAGE SWELL COMPENSATION

In this case study compensation performance of GUPQC will be tested for increased voltages. Supply voltages of bus-2 and bus-3 are subjected to 50% voltage swell of the nominal supply voltage at the interval from $t=0.05$ sec to $t=0.15$ sec as shown in Figs. 13 (a) to (c) and Figs. 14(a) to (c). In order to compensate the voltage swell of the bus-2, DVR-1 injected the required out-of phase voltage swell components in order to cancel the supply side voltage increase which occurs at the load-2 terminal as shown in Fig.13 (b). It can be seen that injected voltage will reduce the effect of voltage swell. Fig. 13(c), shows the load voltage of the sensitive load-2 which is harmonic free and at the desired level.

Likewise, in order to compensate the voltage swell of the bus-3, DVR-2 injected the required out-of phase voltage swell components in order to cancel the supply side voltage increase which occurs at the load-3 terminal as shown in Fig.14 (b). It can be seen that injected voltage will reduce the effect of voltage swell. Fig. 14(c), shows the load voltage of the sensitive load-3 which is harmonic free and at the desired level. The effect of the supply voltage swell on bus-2 and bus-3 at customer's premises is described in Table-2.

Bus	Condition	Source Voltage	Injecting Voltage	Load Voltage
2	SWELL 50	644	222	425
3	SWELL 50	670	243	427

Table -2: Measured voltages of GUPQC during voltage harmonics and Swell

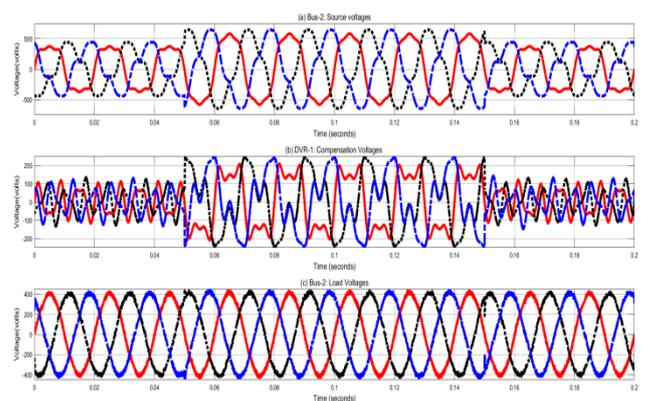


Figure 13: Voltage harmonic and swell compensations of bus-2 (a) Source voltages, (b) DVR-1 compensation voltages and (c) Load voltages

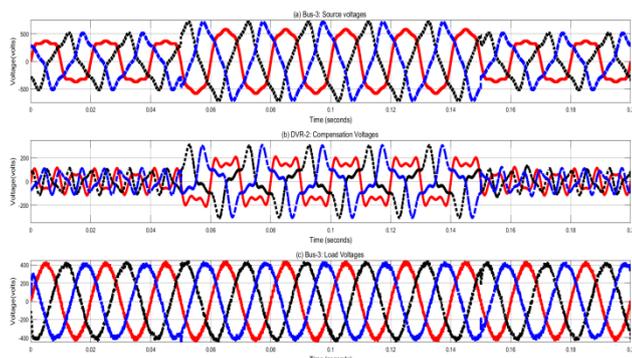


Figure 14: Voltage harmonic and swell compensations of bus-3

(a) Source voltages, (b) DVR-2 compensation voltages and (c) Load voltages

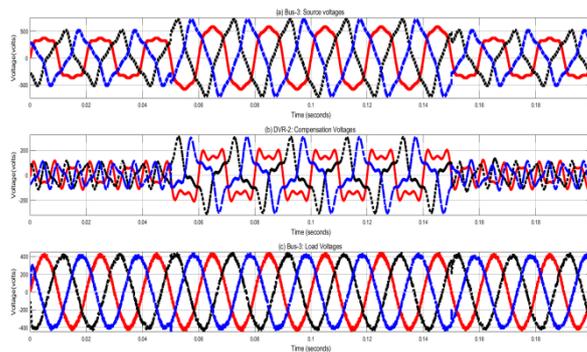


Figure 16: Voltage harmonic and swell compensations of bus-3

(a) Source voltages, (b) DVR-2 compensation voltages and (c) Load voltages

VIII. VOLTAGE HARMONICS AND VOLTAGE SAG / SWELL COMPENSATIONS

In this case study, 30% magnitude voltage sag of supply voltage of bus-2 and 50% magnitude voltage swell of supply voltage of bus-3 are subjected in the time interval from t= 0.05 sec to t= 0.15 sec as shown in Figs. 15 (a) to (c) and Fig. 16 (a) to (c).

Due to sag at the bus-2, DVR-1 responded rapidly and applied the required compensation voltages as shown in Fig. 15(b), as result the load-2 voltage was effectively maintained harmonic free and the desired level as shown in Fig.15 (c). Similarly, DVR-3 applied the compensation voltage as shown in Fig. 16 (b) and the Load-3 voltage as seen in Fig. 16 (c) was also converted to the sinusoidal form and at the same frequency. The effect of voltage sag / swell on bus-2 and bus-3 at customer’s premises is illustrated in Table-3.

Table-3: Measured voltages of GUPQC during sag at bus-2 and swell at bus-3

Bus	Condition	Source Voltage	Injecting Voltage	Load Voltage
2	SAG 30	246	184	410
3	SWELL 50	670	243	421

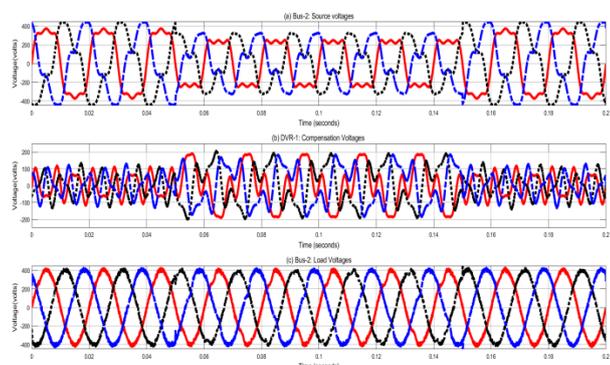


Figure 15: Voltage harmonic and sag compensations of bus-2

(a) Source voltages, (b) DVR-1 compensation voltages and (c) Load voltages

IX. CONCLUSION

This work proposes control scheme for GUPQC based on UVT for DVR and PQ theory for DSTATCOM. MATLAB/SIMULINK environment is used to develop and simulate GUPQC model. From the simulation study one can see that harmonics and sag/swell in supply side and load side current harmonics are easily taken care of by the use of the proposed control scheme. From the above results, it can also be found that the values of supply side current and load voltage harmonics are well below norms of IEEE 519.

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