ISSN No:-2456-2165

Counter Design for Monitoring Shopping Mall Entrances During Covid-19

Tamana Baba
Department of electrical and computer engineering
International Islamic university of Malaysia
Kuala lumper, Malaysia

Syed Zainab Altaf
Department of electronics and communication engineering
SMVDU
Katra, India

Abstract:- In this paper, a 7-bit up down counter is designed to monitor the human-traffic entering and leaving the shopping mall entrances to maintain a maximum number of 99 people inside the mall to promote social distancing. This counter is cleared and reset to 0 every morning. Whenever the sensed data collected by IR sensors fed to the counter reaches 99 during the day, it will be displayed, and no further people will be allowed to go in until people start leaving the mall and the count is reduced from 99.

Keywords:- *Up Down Counter; Reset; Increament; Decreament; Covid-19.*

I. INTRODUCTION

The current outbreak of the corona virus disease has spread rapidly worldwide. An extremely effective method to stop this virus from spreading is social distancing. To govern the protection against the disease, the world health organization (WHO) recommended that countries should improve the identification, reporting and recording of COVID-19 cases and practice isolation, introduce traffic control and suspend large gatherings [1]. Keeping this in mind the mall operators have to take appropriate measures to maintain social distancing and allow a specific number of people at a time to enter a mall. For this purpose, a digital counter has been designed that keeps track of people entering and leaving the mall. It allows maximum of 99 people to enter a shopping mall. The up-down counter meets the need of counting in bidirectional manner. It finds its application in following the SOP's of covid-19 as it involves both enter as well as exit monitoring. The design, VHDL coding and simulations have been performed in QUARTUS II.

II. LITERATURE REVIEW

Sequential circuits like counters, which are made up of flip-flops, are the basic building blocks of the VLSI systems. The major issue with VLSI systems is power dissipation. So, the choice and design of counter for various applications should be as such that it consumes least power and makes the VLSI system energy efficient. In recent years, researchers have proposed various designs of counters, which operate in the optimized way as compared to the conventional binary counters. In [2], a power efficient design of synchronous counters that reduces the power consumption due to clock distribution for different flip-flops and offers high reliability is proposed. In [3], a design of 64bit up down counter & its implementation on FPGA is presented. In [4], an area, power and speed efficient structure for 3-bit asynchronous up counter for VLSI designing is proposed. In this paper number of transistor count is reduced by 69.56%, power is reduced by 46.05% and speed is increased by 49.8% compare to conventional design.

Information processing using Neural Network Counter can result in faster and accurate computation of data due to their parallel processing, learning and adaptability to various environments. In [5], r, a novel 4-Bit Negative Edge Triggered Binary Synchronous Up/Down Counter using Artificial Neural Networks trained with hybrid algorithms is proposed. In [6], author presents the design of asynchronous and synchronous digital counters using a novel reversible gate. This design intends to optimize the counter in terms of number of reversible gates, delay, and garbage outputs and thus complexity of the circuit reduces.

III. METHODOLOGY

A. Pins and signals used

A 7-bit binary up down counter which will count a maximum up to 99 (1100011) has been designed. 'Reset' is used to reset the counter every morning to 0. 'Up_down' is used to indicate whether people are going in or coming out. The coming out of people is indicated when 'Up_down' is high. At this time, the counter is decremented by 1 and when 'Up_down' is low, it indicates going in of people and at this time counter is incremented by 1. 'counter' is used to show the count of the counter. If the number of people in the mall is 99, then the counter will stop its operation and will display 99(1100011). It will resume its operation only when 'Up_down' is high (people come out of the mall). All these operations are performed when 'Clk' is Units.

B. Flow chart

"Fig. 1" shows the flow chart of the project.

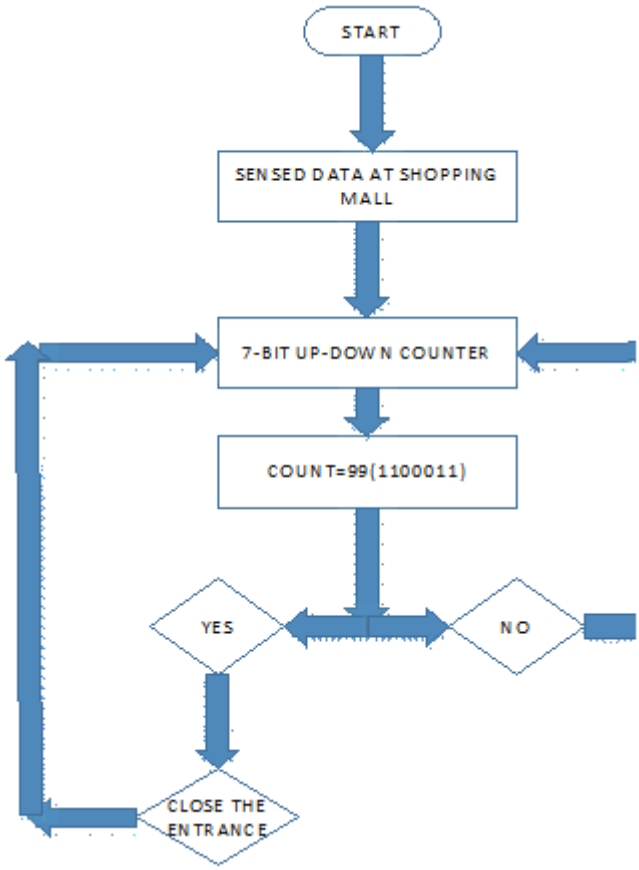

Fig. 1. Flow chart

C. Block diagram

The block diagram of the project is shown in figure 1. Any operation is performed only when 'Clk' is given to the counter. The 'Up_down' and 'reset' are inputs to the counter while the 'counter' is the output signal representing the count.

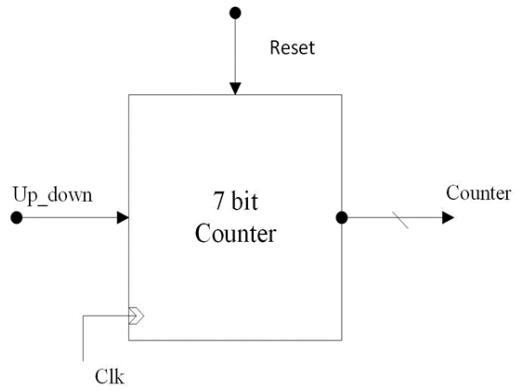

Fig. 2. Block Diagram of 7 bit bidirectional Counter

D. Pseudo code

Algorithm 1: pseudo code for up-down counter

Preset value 1=0000000;
Preset value 2=1100011;
Call the library = IEEE.STD_LOGIC1164.ALL;
and library =IEEE.STD_LOGICUNSIGNED.ALL;
Initialize counter by input clk= rising_edge; // enter gate is open
// at the beginning
Input Reset =0000000;
For all count = 0 to 98
If input up-down=low;
Counter is incremented
Elseif input up-down= high;
Counter is decremented
End if
End for
For count =99
If input up-down=low;
Counter is unchanged // enter gate is closed
Elseif input up-down= high;
Counter is decremented
End if
End for

IV. RESULTS

A. Top Module RTL

The pre-optimized design in terms of generic symbols and all the gate level connections can be seen in figure 2.

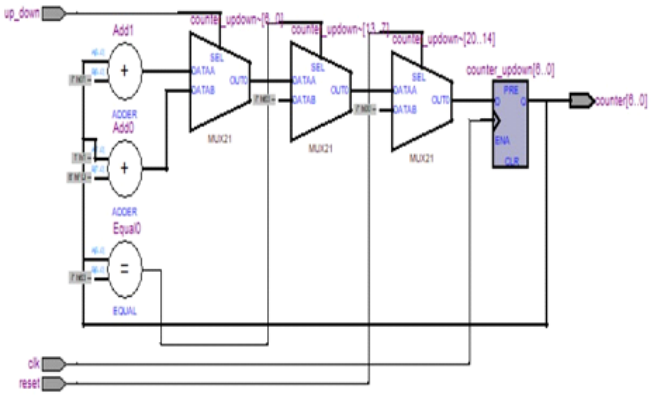

Fig. 3. Top Module RTL

B. Simulation Waveforms

We can see in the waveforms how the counter output is incremented every time 'Up_down' is low and how it is decremented when 'Up_down' is high on every positive clock edge. We can also see that once the count reaches 99, counter will continue to display 99 and will not resume its operation until the count is decremented. We can see that when reset is high, the count is set to 0.

ISSN No:-2456-2165

The simulation results for four different cases of pedestrians entering the mall is shown below.

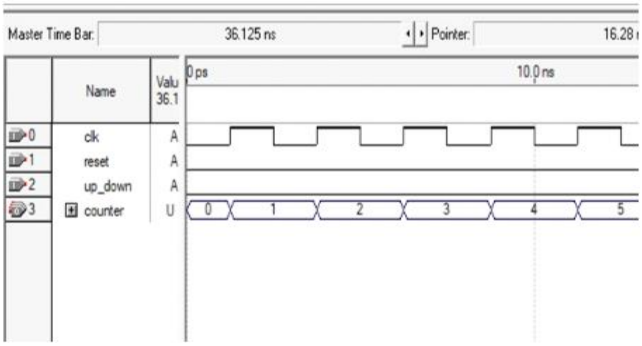

Fig. 4. Case 1 waveform : Counter initially counting the number of people entering the mall.

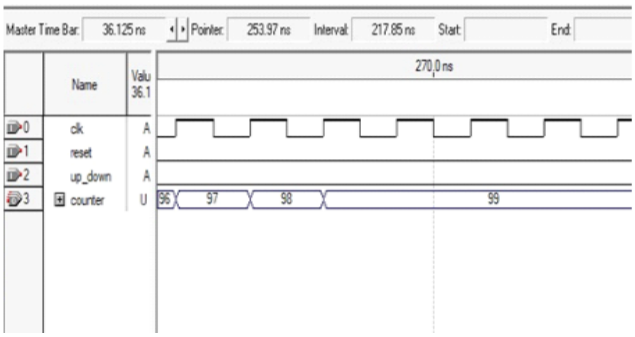

Fig. 5. Case 2 waveform Counter counting the number of people till 99 and will continue to display number till the some number of people exit the mall.

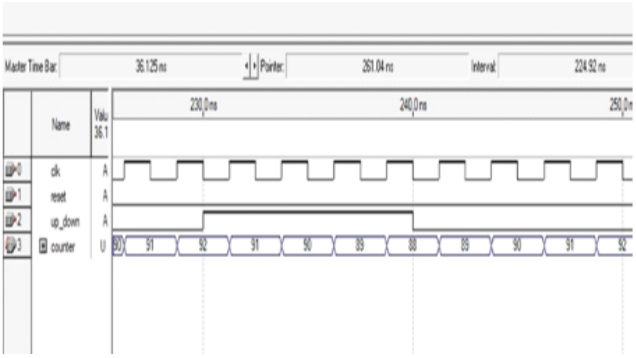

Fig. 6. Case 3 waveformCounter starts countig people again when up-down pin goes high

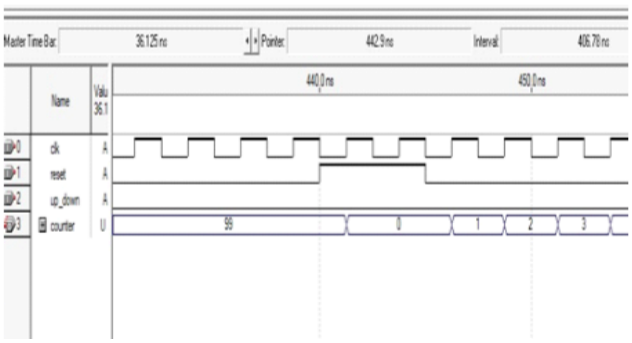

Fig. 7. Case 4 waveform: Counter keeps count of people who randomly come in and out of shopping mall gate.

V. CONCLUSION

In order to gain recovery in all sectors including healthcare, education and business from current pandemic situations the up/down counter designed above will be of great help. As depicted from the simulation results the counter will be helpful to regulate and manage the crowd in hotspot areas during the outbreak of any virus. The up-down counter discussed in this paper works for the population of up to 99, allowing only 99 people at a time to enter the shopping mall and closing the door for the rest until the number falls again from 99. To incorporate the sense of civilized behavior during the pandemic the use of the technology like an up-down counter to manage the crowd is essential.

FUTURE WORK

This design can be further optimized using low power and energy efficient bidirectional counter in the near future to also serve the purpose of energy harvesting.

REFERENCES

[1]. N. el-Guebaly, “COVID-19 and social distancing,” *Can. J. Addict.*, vol. 11, no. 2, pp. 4–6, Jun. 2020, doi: 10.1097/CXA.0000000000000081.

[2]. R. Katreepalli and T. Haniotakis, “Power efficient synchronous counter design,” *Comput. Electr. Eng.*, vol. 75, pp. 288–300, May 2019, doi: 10.1016/j.compeleceng.2018.01.001.

[3]. R. K. Pundir, “Design of 64 bit Integer Multiplier for Low Power Consumption.” Accessed: Feb. 26, 2021. [Online]. Available: https://www.researchgate.net/publication/224928055.

[4]. A. Thakur and R. Mehra, “Power and speed efficient ripple counter design using 45 nm technology,” in *1st IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems, ICPEICES 2016*, Feb. 2017, doi: 10.1109/ICPEICES.2016.7853183.

[5]. R. T. Yakkali and N. S. Raghava, “Neural Network Synchronous Binary Counter Using Hybrid Algorithm Training,” *Image, Graph. Signal Process.*, vol. 10, pp. 38–49, 2017, doi: 10.5815/ijigsp.2017.10.05.

[6]. R. Singh and M. K. Pandey, “Design and optimization of sequential counters using a novel reversible gate,” in *Proceeding - IEEE International Conference on Computing, Communication and Automation, ICCCA 2016*, Jan. 2017, pp. 1393–1398, doi: 10.1109/CCAA.2016.7813936.