ISSN No:-2456-2165

Review of Recently Proposed Multilevel Inverter Topologies

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Abstract:- In recent years, multilevel inverters have attracted tremendous interest in the industry for the application in medium voltage and high power situations. The multilevel inverter (MLI) has a number of advantages, including the ability to operate at both fundamental and lower switching frequencies, the ability to draw low-distortion input current, and low total harmonic distortion (THD) in the output waveform without the use of a filter circuit. Multilevel inverter have been widely used in power factor compensators, interfacing with renewable energy sources, variable speed control of high power drives, electrical braking systems of the vehicles, back to back frequency link systems and DC power source utilizations. In this article, the brief review of classical multilevel inverter topologies are presented. The demonstration provides a new direction in the option of particular topology for multilevel inverter to relevant applications in the real world.

Keywords:- *Multilevel Inverter, THD, Power Drives.*

I. INTRODUCTION

Many industrial applications have become more power-hungry over time. Using high-power sources for all industrial loads may be lucrative for some motors, but it may cause damage to other loads. As a result, in high-power and medium-voltage applications, multilevel inverters are available. A multilevel inverter is a power electrical device that uses many lower level DC voltages as an input to produce the desired alternating voltage level at the output. The traditional topologies are classified into three main groups: diode-clamped multilevel inverter (DCI), flying-capacitor multilevel inverter (FCI), cascade H-bridge multilevel inverter (CHBI). Quality of voltage and current waveform in inverter is being analysed by calculating the THD only. In case of inverter design, low quantity THD means highly accurate sine wave. So the output voltages have more steps when the number of levels in the inverter is increased, resulting in a stair case waveform with lower overall harmonic distortion. We can also reduce the THD by increasing the switching frequency because if we increase the switching frequency the higher order harmonic is automatically eliminated. This paper emphasizes the investigation about the categories of multilevel inverter topology.

II. MULTILEVEL INVERTER TOPOLOGIES

As previously stated, with the introduction of multilevel inverters, the so-called traditional topologies (such as diode clamped, flying capacitors, and cascaded H-bridge) drew the most attention from academia and industry. Despite this, no one architecture appears to be optimal, as multilevel solutions are significantly influenced by application and cost considerations. A given topology may be useful in some circumstances but completely unsuitable in others due to its inherent properties. As a result, the best remedy is frequently offered on a case-by-case basis. As a result, in addition to exploring classical topologies, researchers continued to develop additional topologies. Some of these literatures are briefly summarized below:

A. cross connected sources based multilevel inverter (CCS-MLI)

When compared to traditional MLIs, this design has the same number of dc voltage sources and fewer switches to generate the same output levels. For single phase five-level inverter output voltage, this topology is adequately illustrated in [1]. Figure 1 shows a schematic diagram of the CCS-MLI. It comprises of three sets of complimentary switches (S_1, S_1'), (S_2, S_2'), and (S_3, S_3'), and two input dc levels of identical magnitudes (V_{dc}). The lode voltage is denoted by the letter $V_L(t)$. Table 1 lists the valid switching states, labelled Φ_k (k = 0 to 7).

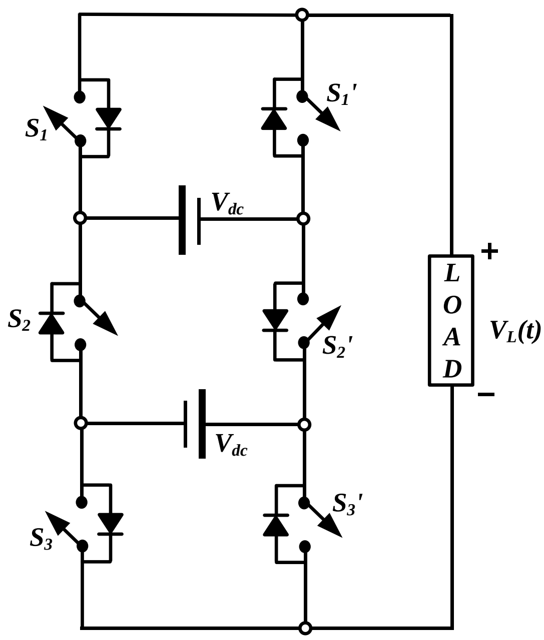

Fig. 1. Basic structure of CCS-MLI [1].

ISSN No:-2456-2165

Table 1. Valid switching states for CCS-MLI shown in Fig. 1

State	ON state switches	V_L(t)
Φ_0	S_1, S_2, S_3	0
Φ_1	S_1', S_2', S_3'	0
Φ_2	S_1, S_2', S_3'	+V_{dc}
Φ_3	S_1', S_2', S_3	+V_{dc}
Φ_4	S_1', S_2, S_3	-V_{dc}
Φ_5	S_1, S_2, S_3'	-V_{dc}
Φ_6	S_1, S_2', S_3	2V_{dc}
Φ_7	S_1', S_2, S_3'	-2V_{dc}

B. Developed H-bridge multilevel inverter

The created H-bridge, a basic unit of topology proposed by Babaei et al. [4], is shown in Fig. 2. Six switches S_1, S_2, S_3, S_4, Sa, S_b and two dc voltage sources of equal magnitude V_{dc} [V1 = V_2 =V_{dc}] make up the basic unit. Based on the different switching patterns of the basic unit, Table 2 illustrates the generated five-level output voltage. The basic unit can be improved for greater voltage levels.

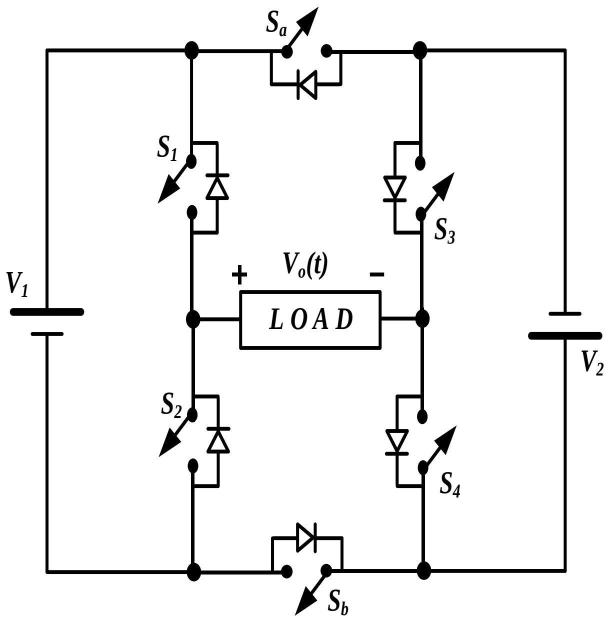

Fig. 2. Developed H-bridge structure [4].

Table 2 Valid switching states for the topology shown in Fig. 2

State	ON state switches	V_L(t)
Φ_0	S_1, S_a, S_3	0
Φ_1	S_2, S_b, S_4	0
Φ_2	S_1, S_b, S_4	+V_{dc}
Φ_3	S_2, S_b, S_3	+V_{dc}
Φ_4	S_1, S_a, S_4	-V_{dc}
Φ_5	S_2, S_a, S_3	-V_{dc}
Φ_6	S_1, S_b, S_3	+2V_{dc}
Φ_7	S_2, S_a, S_4	-2V_{dc}

C. Cascaded multilevel inverter

Odeh et al. [5] present a topology for cascaded MLI. In comparison to typical architectures, the proposed structure significantly reduces the number of power switches. The basic unit's inverter circuit is shown in Fig. 3. It consists of three input isolated dc sources of identical value [V_1 = V_2 = V_3 = V_{dc}], two sets of complementary switches (S_1, S_1') and (S_2, S_2'), as well as three additional switches (S_3, Sx, S_4). Vo(t) is the output voltage specification. The different switching combinations, referred to as α_i (i = 0 to 6), are listed in Table 3.

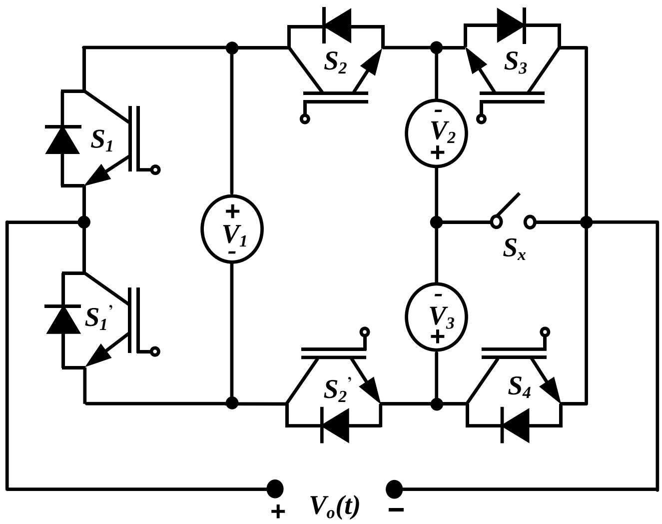

Fig. 3. Basic unit of topology for cascaded MLI [5].

Table 3 Valid switching states for the topology shown in Fig. 3

State	ON Switches		V_o(t)
α_0	S_1, S_2, S_3	S_1', S_2', S_4	0
α_1	S_1', S_2', S_x	S_1, S_2', S_4	+V_3, +V_1
α_2	S_1', S_2', S_3	S_1, S_2', S_x	V_2+V_3, V_1+V_3
α_3	S_1, S_2', S_3		V_1+V_2+V_3
α_4	S_1', S_2, S_3	S_1, S_2, S_x	-V_1, -V_2
α_5	S_1, S_2, S_4	S_1', S_2, S_x	-V_2-V_3, -V_1-V_3
α_6	S_1', S_2, S_4		-V_1-V_2-V_3

D. symmetrical and asymmetrical MLIs

The configurations of symmetrical and asymmetrical MLIs are presented with the objective of reducing the number of devices, complexity and improving the overall system performance [6]. Figure 4 shows a power circuit for an inverter based on the proposed concept, which includes a symmetrical source configuration. It comprises of three input dc links of equal magnitudes [V_1 = V_2 = V_3 = V_{dc}] and seven power switches viz. P_1, P_2, P_3, P_4, P_5, P_6 and P_7. Table 4 shows the list of all valid switching states for the new configuration of MLI.

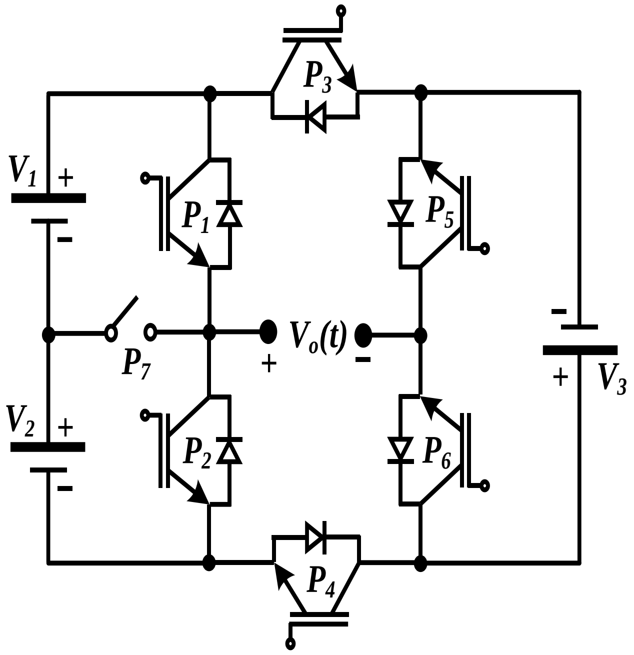

Fig. 4. Configuration of MLI as proposed in [6].

Table 4 Valid Switching States for the topology shown in Fig. 4

State	ON Switches		$V_o(t)$
σ_0	P_1, P_4, P_5		$V_1+V_2+V_3$
σ_1	P_5, P_4, P_7	P_6, P_4, P_1	V_2+V_3, V_1+V_2
σ_2	P_4, P_7, P_6	P_5, P_4, P_2	V_2, V_3
σ_3	P_1, P_3, P_5	P_2, P_4, P_6	0
σ_4	P_7, P_3, P_5	P_1, P_3, P_6	$-V_1$, $-V_3$
σ_5	P_7, P_3, P_6	P_2, P_3, P_5	$-V_1-V_3$, $-V_1-V_2$
σ_6	P_2, P_3, P_6		$-V_1-V_2-V_3$

E. seven-level inverter topology

Figure 5 depicts the basic unit of topology proposed by Hsieh et al. [7] for a seven-level inverter. It is made up of eight unidirectional switches S1, S2, S3, S4, S5, S6, S7, and S8 as well as four diodes D1, D2, D3, D4. Three input dc voltage sources of equal magnitude are used in the topology. The basic unit's switching pattern is depicted in Table 5. The unit is duplicated and connected in series to boost the output voltage level. This topology offers advantages such as reduced switching losses as well as reduced voltage ratings of power switches.

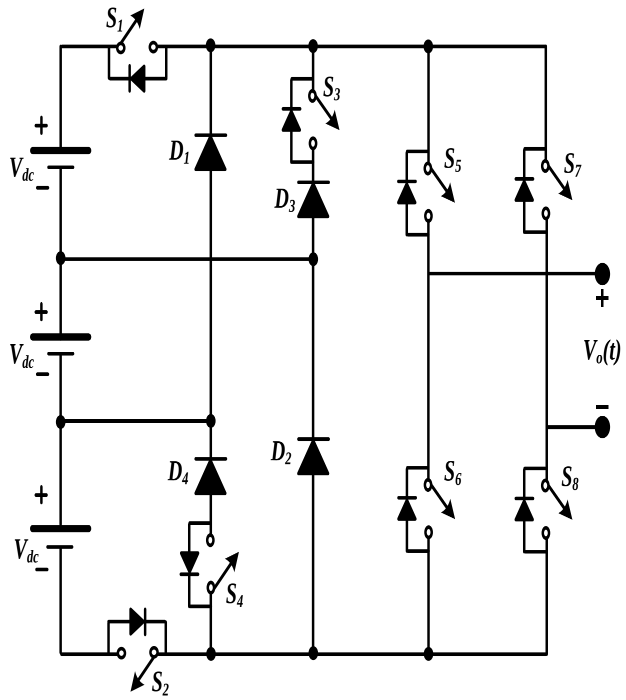

Fig. 5. Topology for seven level inverter [7].

Table 5 Switching combinations for the topology shown in Fig. 5

State	ON state switches	$V_o(t)$
Φ_0	S_5, S_7	0
Φ_1	S_6, S_8	0
Φ_2	S_1, S_5, S_8	$+V_{dc}$
Φ_3	S_1, S_4, S_5, S_8	$+2V_{dc}$
Φ_4	S_1, S_2, S_5, S_8	$+3V_{dc}$
Φ_5	S_2, S_6, S_7	$-V_{dc}$
Φ_6	S_2, S_3, S_6, S_7	$-2V_{dc}$
Φ_7	S_1, S_2, S_6, S_7	$-3V_{dc}$

F. E-type module of MLI

Samadaei et al. [8] introduced an E-type module of MLI with reduced devices as shown in Fig. 6. This topology can generate thirteen levels with eight switches S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8 and four unequal dc sources V_1, V_2, V_3, V_4 (two $2V_{dc}$ and two $1V_{dc}$) where S_7, S_8 are bidirectional switches in common emitter form. Without the use of an H-bridge, the module can generate negative levels. Table 6 demonstrates the various switching states for various input dc voltage source combinations.

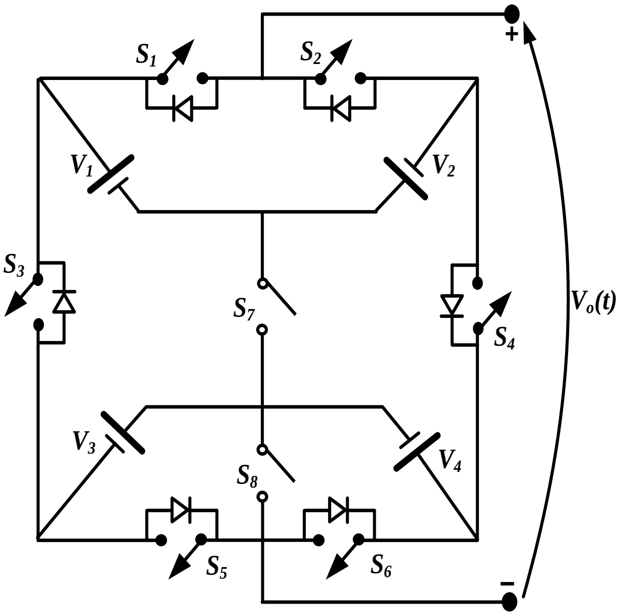

Fig. 6. E-type module of MLI [8].

Table 6 Various possible switching combinations for the module shown in Fig. 6

State	ON state switches	$V_o(t)$
Φ_0	S_1, S_3, S_5	0
Φ_1	S_2, S_4, S_6	0
Φ_2	S_1, S_6, S_7	$+V_{dc}$
Φ_3	S_1, S_7, S_8	$+2V_{dc}$
Φ_4	S_1, S_5, S_7	$+3V_{dc}$
Φ_5	S_1, S_4, S_6	$+4V_{dc}$
Φ_6	S_1, S_4, S_8	$+5V_{dc}$
Φ_7	S_1, S_4, S_5	$+6V_{dc}$
Φ_8	S_2, S_5, S_7	$-V_{dc}$
Φ_9	S_2, S_7, S_8	$-2V_{dc}$
Φ_{10}	S_2, S_6, S_7	$-3V_{dc}$
Φ_{11}	S_2, S_3, S_5	$-4V_{dc}$
Φ_{12}	S_2, S_3, S_8	$-5V_{dc}$
Φ_{13}	S_2, S_3, S_6	$-6V_{dc}$

III. CONCLUSION

Multilevel inverters are the industry's preferred solution for applications involving high voltage and high power. A multilevel converter is required to provide a power output from a medium voltage source. Multilevel inverters are a variation on the two level inverter concept. More than two voltage levels are combined in multilevel inverters to generate a smoother stepped output waveform. The voltage levels are directly related to the smoothness of the waveform. The waveform becomes smoother as the voltage level rises, but the complexity rises as well. Six different types of multilevel inverter topologies are discussed in this article. Based on the review, it can be determined that by reducing or reordering the DC input voltages, the multilevel inverter's power switch count can be reduced.

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