Implementation of Turbo Coder Using Verilog HDL for LTE

V S Sneha
M. TECH VLSI (S4)
NCERC, Trissur, Kerala, India
Nithin Joe
Assistant Professor ECE Dept
NCERC, Trissur, Kerala, India

Abstract:- **In many communication systems, turbo codesare employed to repair errors. Turbo codes demonstrate high error correction when compared to other error correction methods. A Very Large Scale Integration is suggested in this study. VLSI architecture for the Turbo encoder implementation, Interleaves and de interleaves, and soft-in-soft-out decoders are employed. This study employs a technique that for the encoder portion, includes two recursive systematic convolutional (RSC) encoders , a Block interleaver and the decoder part involve Soft Output Virtebi Algorithm (SOVA) decoder. A convolutional code is a sort of error-correcting code used in communications that creates parity signals by sliding a Boolean polynomial function across a data stream. The word "convolutional coding" comes from the sliding application, which depicts the encoder's "convolution" across the data. Convolutional codes sliding properties make it easier to do trellis decoding with a time-invariant trellis. Convolutional codes can be maximum-likelihood soft-decision decoded with a manageable level of complexity thanks to time invariant trellis decoding. The Viterbi algorithm, also known as the Viterbi path, is a dynamic programming approach for determining the greatest probability estimate of the most probable series of hidden states that leads to a series of observed events. The quantity of times needed to decode the bits is been reduced in this methodology. A block interleaver accepts a set of symbols and rearranges them, without repeating or omitting any of the symbols in the set. The number of symbols in each set is fixed for a given interleaver. Turbo encoding, as well as decoding simulations are done using Modelsim software.**

Keywords:- *Turbo Codes; Interleaver; Viterbi Algorithm; SOVA.*

I. INTRODUCTION

When data is transported from a source system to a destination system in a communication system, errors may be present in the signal that is received at the source end. To get the original message back, rectification is needed. Turbo codes, first made available in 1993, symbolise a channel coding methods make a quantum leap, and the tide is turning a plus for current digital communication. Using turbo codes one of the potent error-correcting codes currently in use. Booster codes has motivated the programming community with the potential for using an iterative decoding method. To obtain close channel capacity, use simple constituent code. Turbo encoder and turbo decoder are components of the turbo coder architecture. Two Recursive Convolutional Encoders (RSC) and an interleaver make up the encoder. As a result of the employment of a pseudo-random interleaver in this study, the interleaved version of the code tends to be lengthy and chaotic, which improves the performance of random codes. RSC encoders are used in turbo code implementation rather than traditional convolutional encoders because they provide low weight parity codes. This system employs an Soft Output Virtebi Algorithm (SOVA) decoder. Data that has been turbo-encoded with mistakes that are created on purpose and then certified as error- free after decoding. Turbo codes are a series of high- performance forward error correction (FEC) codes that were developed in the 1990s and 1991s but weren't formally presented until 1993. Turbo codes were originally known as Turbo codes in French. The Shannon limit, also known as the maximum channel capacity, refers to the greatest coding rate at which reliable communication is still possible in the presence of a specific noise level. They were the first practical codes to approach this limit. Turbo codes are employed in 3G/4G mobile communications (like UMTS and LTE), in (deep space) satellite communications, and in other applications where programmers need to achieve dependable data transfer over bandwidth- or latency-constrained communication links while contending with data-corrupting noise.

II. METHODOLOGY

A. Architecture of Turbo Coder

The Turbo coder architecture is made up of a turbo encoder and a turbo decoder. Using pseudorandom interleavers and convolutional encoders (RSC) makes up the turbo encoder. A third of the workforce is employed by LTE. Fast code with simultaneous concatenation rate. Various RSCs work on two unique sets of data. The first is given original data second encoder gets the interleaved data from the first version of the data entered. Interleaving is a technique that scrambles the data bits. a significant effect on a decoder's performance when the interleaving method is used, is seen. The outputs from RSC1 and RSC2 encoders as well as systematic input consists of a 24 bitoutput. The output of the turbo encoder, which is a 24 bit out put that is composed of the RSC1 and RSC2 encoder outputs as well as systematic input. This will be sent to the Turbo deco der through the channel.

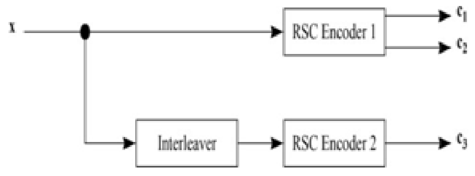

Fig2.1 Block diagram of Turbo Coder

A r = 1/3 turbo code encoder is shown in Figure 2.1.

While the second RSC encoder discards its systematic sequence and only produces the recursive convolutional c3 sequence, the first RSC encoder outputs the systematic c1 and recursive convolutional c2 sequences.

B. *Recursive Systematic Convolutional (RSC) Encoder*

By feeding back one of its encoded outputs to its input, the non recursive nonsystematic (conventional) convolutional encoder is transformed into the recursive systematic convolutional (RSC) encoder. A typical convolutional encoder is shown in Figure 2.2. The generator sequences g1 = [111] and g2 = [101] are used to represent the traditional convolutional encoder, which may also be expressed more succinctly as G=[g1, g2].

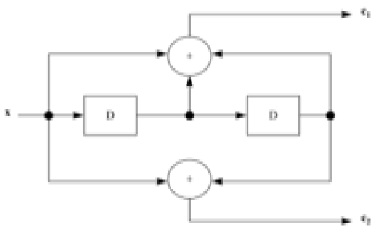

Fig 2.2 Conventional convolutional encoder with r=1/2 and K=3

The first output (represented by g1) is sent back to the input in the RSC encoder of this standard convolutional encoder, which is represented as G=[1, g2 / g1]. In the diagram above, 1 stands for the systematic output, g2 for the feedforward output, and g1 for the feedback to the RSC encoder's input. The finished RSC encoder is displayed in Figure 1.3.According to [Bat93], excellent codes can be produced by s etting the feedback of the RSC encoder to a primitive polynomi al since this adds randomness to the turbo code by generating maximum-length sequences.

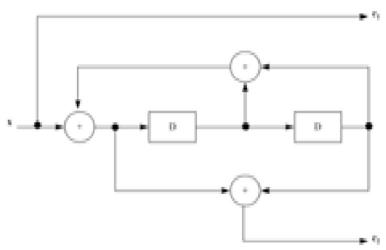

Fig 2.3 The RSC encoder obtained (from fig 1.2) with r=1/2 and K=3.

C. *Interleaver Design*

Between the two component encoders for turbo codes, there is an interleaver. The input sequences are given randomization thanks to the interleaver. For RSC Encoder 1, the input sequence x generates the low-weight recursive convolutional coding sequence c2. The interleaver permutes the input sequence x to prevent RSC Encoder 2 from creating another low-weight recursive output sequence obtain an alternative sequence that, ideally, results in a high-weight recursive convolutional Coding pattern c3. The coding weight of the turbo code is therefore minimal when coupled from Low- weight code from encoder 1 and high-weight code from encoder 2.

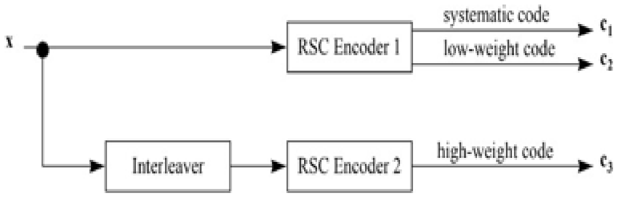

Fig 2.4 The interleaver increases the code weight for RSC Encoder 2 as compared to RSC Encoder

D. *Block Interleaver*

The block interleaver is the interleaver that communication systems employ most frequently. It reads out rows from left to right and top to bottom and writes in columns from top to bottom and left to right. A block interleaver is seen in Figure 2.5.

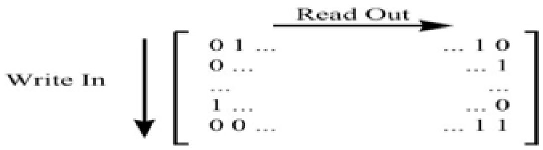

Fig 2.5 Block Interleaver

E. *Soft Output Viterbi Algorithm (SOVA)*

Because of its straightforward implementation, the Viterbi algorithm (VA) is a popular technique for maximum likelihood decoding that can be employed in the majority of real-world scenarios. However, one of its drawbacks is that it is unable to deliver soft-decision outputs. Contrary to soft-output decoders, combining two VA decoders results in a significant performance loss. The SOVA produces a soft (or real) dependability number corresponding to each decoded bit rather than decoded bits (i.e., hard judgments). Other system components (like a serially concatenated convolutional coding system) can exploit these soft outputs to enhance overall performance.

Fig 2.6 Block diagram of SOVA

The turbo decoding algorithm's iterative design principle in between the two SISO component decoders that are shown Figure 2.7. It consists of two decoders, those that work simultaneously to enhance and improve the estimated number of original data bits. Secondly, the SISO decoder decodes the convolutional either the first or second CE's code is produced. A fast iteration is equivalent to one pass of the primary component decoder, which a trip through the second component decoder follows.

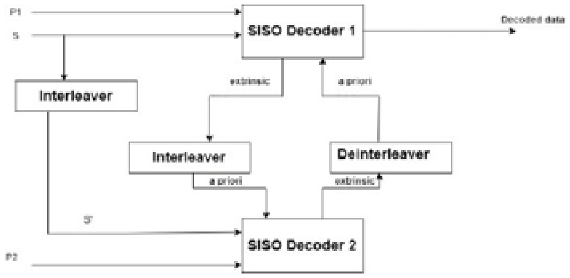

Fig2.7 Block diagram of Turbo Decoder

III. RESULT AND DISCUSSIONS

Verilog HDL is the coding language employed in this proposed system and the timing analysis has been performed using Modelsim Software.

F. Simulation Output of Turbo Encoder

Figure 3.1 shows the simulation output of turbo encoder. Signals st1 and st2 represents clock and reset signals respectively. The signal x represents the input signal of the system. For RSC Encoder 1, the input sequence x generates the low-weight recursive convolutional coding sequence c2. The interleaver permutes the input sequence x to prevent RSC Encoder 2 from creating another low-weight recursive output sequence obtain an alternative sequence that, ideally, results in a high-weight recursive convolutional Coding pattern c3. The coding weight of the turbo code is therefore minimal when coupled from Low-weight code from encoder 1 and high -weight code from encoder 2. While the second RSC encoder discards its systematic sequence and only produces the recursive convolutional c3 sequence, the first RSC encoder outputs the systematic c1 and recursive convolutional c2 sequences.

G. Simulation Output of Turbo Decoder

The turbo decoding algorithm's iterative design principle in between the two SISO component decoders. It consists of two decoders, those that work simultaneously to enhance and improve the estimated number of original data bits. Secondly, the SISO decoder decodes the convolutional either the first or second CE's code is produced. A fast iteration is equivalent to one pass of the primary component decoder, which a trip through the second component decoder follows.

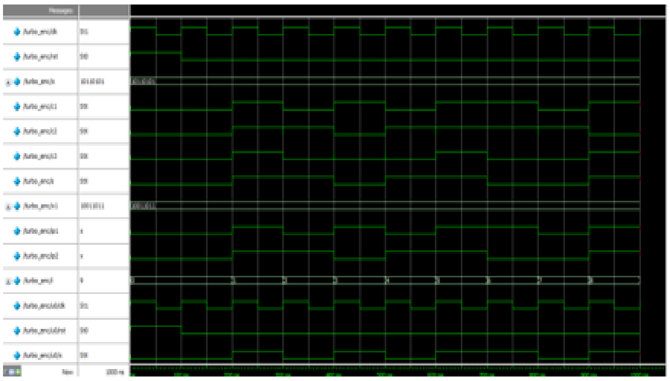

Fig 3.1 Simulation output of Turbo Encoder

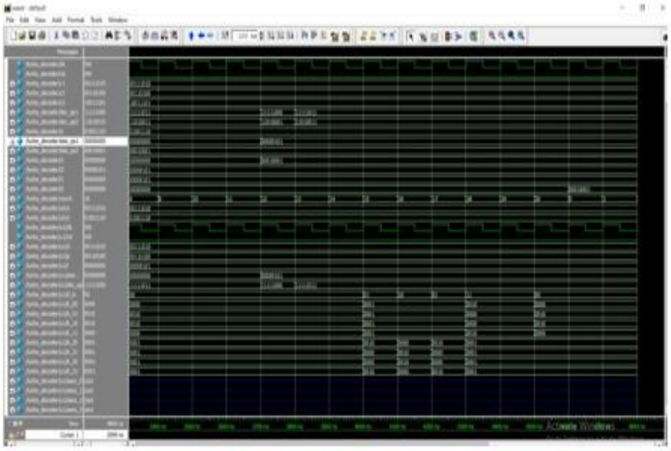

Fig 3.2 Simulation Output of Turbo Decoder

IV. CONCLUSION

Turbo encoder and turbo decoder are components of the turbo coder architecture. Two Recursive Convolutional Encoders (RSC) and an interleaver make up the encoder. As a result of the employment of a pseudo-random interleaver in this study, the interleaved version of the code tends to be lengthy and chaotic, which improves the performance of random codes. RSC encoders are used in turbo code implementation rather than traditional convolutional encoders because they provide low weight parity codes. Good codes can be obtained by setting the feedback of the RSC encoder to a primitive polynomial, because the primitive polynomial generates maximum-length sequences which adds randomness to the turbo code This system employs an Soft Output Virtebi Algorithm (SOVA) decoder. Data that has been turbo-encoded with mistakes that are created on purpose and then certified as error-free after decoding. The optimal decoding technique, known as the Viterbi decoding method, identifies the most likely pattern from the incoming data using the maximum likelihood decoding (MLD) algorithm. This makes Viterbi decoding method most efficient when compared to the other existing decoding methods .

REFERENCES

[1]. V. Kavinilavu1, S. Salivahanan, V. S. Kanchana Bhaaskaran2 , Samiappa Sakthikumaran, B. Brindha and C. Vinoth ”Implementation of Convo- lutional Encoder and Viterbi Decoder using Verilog HDL ”, IEEE 3rd International Conference on Electronics Computer Technology,2011

[2]. Aswathy Narayanan ; Senthil Murugan ; Ramesh Bhakthavatchalu, ”Low Latency Max Log MAP based Turbo Decoder”, International Conference on Communication and Signal Processing (ICCSP),2019

[3]. C. Tanriover ; B. Honary ; Jun Xu ; Shu Lin”, ”Improving turbo code error performance by multifold coding”,IEEE Communications Letters, 2002

[4]. Shweta Ramteke ; Sandeep Kakde ; Yogesh Suryawanshi , ”HDL Imple- mentation of Turbo Decoder Using Soft Output Viterbi Algorithm”,2015.

[5]. J.H. Han ; A.T. Erdogan ; T. Arslan ,”Power and area efficient turbo decoder implementation for mobile wireless systems”, IEEE Workshop on Signal Processing Systems Design and Implementation,2005

[6]. Cheng-Chi Wong ; Ming-Wei Lai ; Chien-Ching Lin ; Hsie-Chia Chang

[7]. ; Chen-Yi Lee,”Turbo Decoder Using Contention-Free Interleaver and Parallel Architecture”,IEEE Journal of Solid-

[8]. State Circuits”,2010

[9]. Yaqin Shi ; Ming Zhan ; Jie Zeng , ”FPGA Implementation and Power Estimation of a Memory-Reduced LTE-Advanced Turbo Decoder”, IEEE International Conference on Internet of Things (iThings) and IEEE Green Computing and Communications (GreenCom) and IEEE Cyber, Physical and Social Computing (CPSCom) and IEEE Smart Data (SmartData), 2018.

[10]. E. Boutillon, C. Douillard, and G. Montorsi , ”Iterative decoding of concatenated convolutional codes: Implementation issues”,Proc. IEEE, vol. 95, no. 6, pp. 1201–1227,June, 2007

[11]. Rami Klaimi ; Charbel Abdel Nour ; Catherine Douillard ; Joumana Farah ,”Low-complexity decoders for non-binary turbo codes” ,IEEE 10th International Symposium on Turbo Codes Iterative Information Processing (ISTC), 2018

[12]. Maria Kovaci ; Horia Balta,”Performance of trellis termination meth- ods for RSC component encoders of turbo codes”, 10th International Symposium on Electronics and Telecommunications,IEEE,2012