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Realization of TMD Circuits: Inverter, and Operational Amplifier

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Abstract:- The scaling of conventional silicon transistors has become increasingly complex due to the degradation of carrier mobility and increase in wire resistance. As a result, researchers have started to investigate various unique materials to meet ITRS goals. Two-dimensional (2D) materials such as CNTs, graphene, GNRs, and TMDs with chemical MX2 forms (e.g., MoS_2) have received significant attention. Among them, TMDs have a 1-2 eV band gap by default, making them a promising candidate for future transistors. In this work, we proposed a MoS_2 transistor model and study the voltage-current (I-V) properties of single-layer MoS_2FETs. The compact MoS_2FET model is introduced and implemented in SPICE for circuit simulations to determine the efficiency of MoS_2FET-based circuits. The proposed model is simplified to reduce computational difficulty and is compatible with SPICE.A monolayer MoS_2 has low leakage current and a significantly larger band gap than a 10-nm tube. In this article, we analysed a single-layer MoS_2 transistor system in accordance with the ITRS specifications and test and verify the results against various channel dimension values and technical requirements. Section II provides more information on MoS_2 transistor modelling and introduces the proposed versatile, SPICE-compatible platform. The experimental results are discussed in Section III, and the conclusions are drawn in Section IV. Overall, this study contributes to the development of high-performance transistors based on 2D materials, particularly TMDs, which have the potential to revolutionize the field of wearable electronics and sensors.

Keywords:- *Transition Metal dichalcogenides (TMD's), Molybdenum disulfide (MoS_2), MoS_2 inverter, SPICE modelling.*

I. INTRODUCTION

The unique electronic properties of Transition Metal Dichalcogenides (TMDs) make them potential candidates for the substitution of Silicon in electronic applications. Molybdenum disulfide (MoS_2), in particular, is a promising material due to its sufficient bandgap, which is lacking in graphene, and its ability to become a channel substrate of transistors. The lack of a bandgap in graphene makes it unsuitable for digital applications due to its inability to fully cut off current, leading to increased static power dissipation. To meet the demands of the electronics sector for faster systems with reduced power consumption, 2D TMDs with a wide bandgap are needed that can support high on/off ratios while retaining high charge carrier mobility and scalability to thinner dimensions.[1,2]

MoS_2 is a promising material in this regard, and this article presents the design of a MoS_2 transistor device capable of addressing the effects of scaling MoS_2 transistor dimensions to 16-nm. The circuit level analysis of MoS_2 transistor circuits is reported through SPICE simulations, which enable the exploration of space and the measurement of process transitions at the circuit level. The MoS_2 transistor model is introduced and simplified to reduce computational difficulty and become compatible with SPICE. The simulations calculate circuit levels to determine the efficiency of MoS_2FET-based circuits, enabling the optimization of device creation, output prediction, and low-power switching circuits.[3,4,5,6]

Verilog-A is a hardware description language used to model and simulate analog and mixed-signal circuits. It is often used to model semiconductor devices like FETs, including MoS_2 and CNT devices. In this article, the Verilog-A models are being used to simulate the electrical behavior of MoS_2 devices. These models are tuned to the specific technology that will be used to manufacture the FETs, meaning that they take into account the specific physical characteristics of the materials and the manufacturing process used to create them. The simulations are performed using a commercial integrated circuit software simulator like SPICE simulator. This software allows the Verilog-A models to be incorporated into larger circuit designs, allowing the behavior of the FETs to be studied in the context of a larger circuit. The simulations can help identify potential issues with the design, optimize performance, and validate the functionality of the FETs before they are fabricated. Overall, this article highlights the potential of MoS_2 as a substitute for Silicon in electronic applications and presents a comprehensive analysis of MoS_2 transistor circuits using SPICE simulations.

II. MOS_2 INVERTER AND OPERATIONAL AMPLIFIER MODELLING

Inverter and operational amplifier circuits are fundamental building blocks in digital and analog circuits, respectively. The MoS_2 FET can be used to implement these circuits due to its excellent electronic properties. To design and optimize the performance of MoS_2-based inverters and operational amplifiers, Verilog-A models were implemented using a commercial integrated circuit software simulator. The

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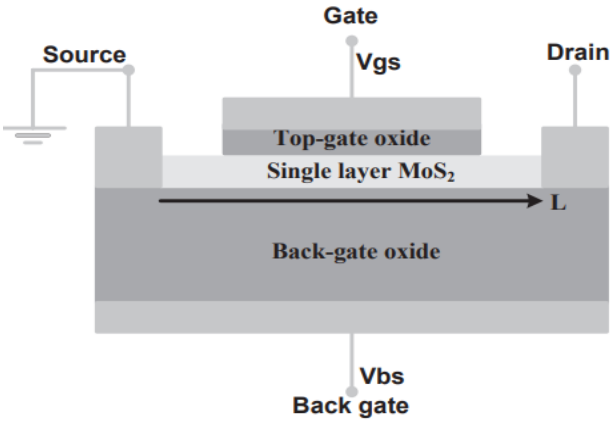
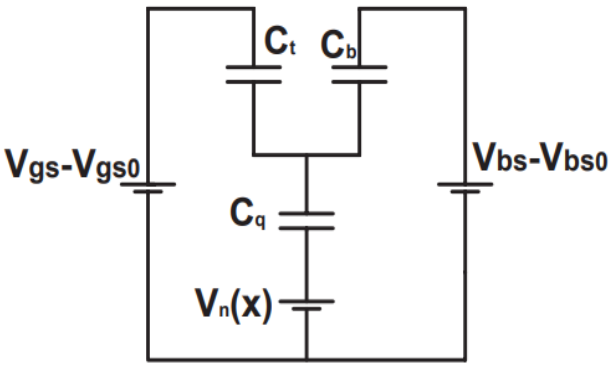
MoS_2 inverter circuit consists of a single MoS_2 FET and a load resistor. The input signal is applied to the gate of the MoS_2 FET, and the output signal is taken from the drain of the FET. The load resistor is connected between the drain of the FET and the supply voltage. By changing the value of the load resistor, the gain and switching speed of the inverter can be optimized. The Verilog-A model of the MoS_2FET includes the threshold voltage, mobility, and saturation velocity parameters, which are specific to the MoS_2 material. The MoS_2 operational amplifier circuit consists of two MoS_2 FETs and two load resistors. The input signal is applied to the gate of the first MoS_2 FET, and the output signal is taken from the drain of the second MoS_2FET. The second MoS_2FET acts as a current source, and the load resistors are connected between the drains of the FETs and the supply voltage. The Verilog-A model of the MoS_2FETs includes the same parameters as the inverter circuit, and the parameters of the load resistors are also included in the model. The electrical simulations of the MoS_2 inverter and operational amplifier circuits were performed using the Verilog-A models in the commercial integrated circuit software simulator. The simulations were used to optimize the performance of the circuits by changing the values of the load resistors and the bias voltages. The results of the simulations were analyzed to determine the gain, bandwidth, and power consumption of the circuits. The optimized MoS_2-based inverters and operational amplifiers can be used in various digital and analog circuits.

The MoS_2 transistor is a promising candidate for digital implementations as it has a reasonable bandgap of 1.8 eV for single layer with HfO_2 dielectric in top-gated configuration FET, ensuring that the transistor off-state is essentially off with a high-drive shift, which is crucial for rapid switching. On the other hand, graphene FETs do not have high Ion/Ioff ratios and are not suitable for faster switching digital circuits. While graphene can be converted into nanoribbons and converted into a GNRFET with a higher Ion/Ioff ratio, it has shown a significant degradation of its efficiency and reduces the mobility. As the transistor channel length decreases, the short channel effect comes into play, where the variation in the electrical field must be taken into account both through the channel and normal to the channels. The TMD's thinner channel and with a weak dielectric value help mitigate the short channel effect. The analysis also showed that the MoS_2 transistor current is mostly limited by the high Rc (contact resistance) between the TMD's and metal, which would be the primary point when TMDFETs are scaled down. The SPICE model of MoS_2 transistor crossection is shown in Figure 1, with the terminals represented as gate (G), drain (D), source (S), bottom gate or bulk (B), and the drain current Ids.





(a)
(b)

Fig 1 (a) Cross section of single layer MoS_2 transistor. (b) Transistor equivalent capacitive circuit.

The effect of power densities and leakage current with scaling can have significant impacts on the performance of CMOS circuits. As the size of transistors is scaled down, the power density increases, which can lead to higher temperatures and reduced reliability. Additionally, the leakage current in MOS_2FETs can increase with scaling, which can further increase power consumption and reduce battery life. The total power consumed by an MOS_2FET circuit block is the sum of the AC power and DC power. The AC power is the sum of the power due to charging and discharging of nodes, which is known as switching power (Ps). Assuming for every clock cycle, a logic gate goes through one complete charge/discharge cycle, the switching power can be calculated as Ps = αCswVdd^2f_clk, where α is a corrective activity factor, Csw is the total switching capacitance, Vdd is the supply voltage, and f_clk is the clock frequency. The activity factor α is less than 1, as most gates do not switch for every clock cycle. The short-circuit power (Psc) is the power consumed when there exists a momentary direct current path between rail to rail (i.e., Vdd and GND) during switching. This occurs when both the n-MoS_2FET and the p-MoS_2FET are momentarily turned on during a transition, resulting in a conducting path between Vdd and GND which allows the short-circuit current to flow directly through an inverter. The short-circuit power of an unloaded inverter can be expressed as

$$Psc = \beta(Vdd-2Vth)\ ^3/(\tau ir*Tp)$$

where β is a parameter that depends on the technology and the inverter layout, Vth is the threshold voltage, τir is the input rise (fall) time, Tp is the time period of input.

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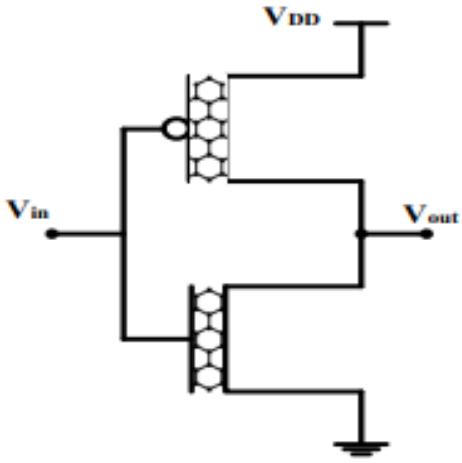
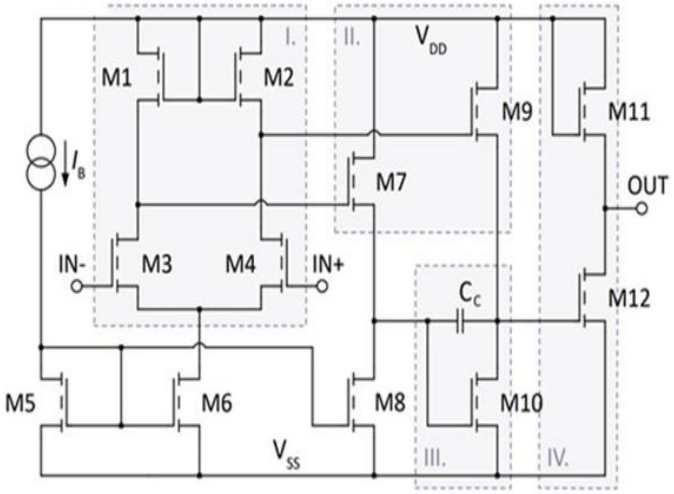
In general, the short-circuit power increases as Vdd or the input rise time (or input fall time) is increased, and as Tp or the threshold voltage is lowered. However, the strengths of these dependencies may be modulated significantly by the transistor's capacitive effects. To reduce the power consumption of MOS_2FET circuits, various techniques such as voltage scaling, clock gating, and power gating can be used. These techniques can help to reduce both the AC and DC power consumption and improve the overall energy efficiency of the circuit.[7]



(a)

Fig 2. Inverter circuit using MoS_2FET



(b)

Fig 3. Operational Amplifier using MOSFET

A MOS_2 op-amp (operational amplifier) is an electronic circuit that amplifies and processes analog signals. It is made up of MOS2FET (metal oxide semiconductor 2D field effect transistor) devices and passive components such as resistors, capacitors, and diodes. Compared to traditional silicon-based op-amps, MOS_2 op-amps offer several potential advantages including higher carrier mobility, lower power consumption, and reduced leakage current. However, they also present some unique challenges such as higher contact resistance and variability in device performance due to the 2D nature of the material. Some common topologies for MOS_2 op-amps include the two-stage amplifier, folded cascode amplifier, and fully-differential amplifier. The choice of topology depends on the desired performance specifications such as gain, bandwidth, and input/output impedance. The key parameters of a MOS_2 op-amp include gain, bandwidth, input/output impedance, input offset voltage, input bias current, input common-mode range, slew rate, and power consumption. These parameters can be calculated using various models and equations based on the specific circuit design and transistor dimensions. MOS_2 op-amps have potential applications in various areas such as analog signal processing, sensor interface circuits, and low-power portable devices. However, further research is needed to optimize their performance and reliability and to develop scalable fabrication techniques for large-scale integration.

The total power consumption of a MOSFET-based operational amplifier (op amp) can be calculated using the following formula

Total Power = Vcc * Iq + Po

Where Total Power is the total power consumption in watts, Vcc is the supply voltage in volts, Iq is the quiescent current in amperes, Po is the output power in watts

The first term in the equation, Vcc * Iq, represents the power consumed by the op amp when there is no output signal. This is known as the quiescent power, and it is a constant power consumption that is always present regardless of the output signal. The second term in the equation, Po, represents the power consumed by the op amp when there is an output signal. This is also known as the dynamic power consumption, and it varies depending on the output signal. The total power consumption is important to consider when designing power-efficient circuits, especially in battery-powered applications where power consumption is a critical parameter.[8,9]

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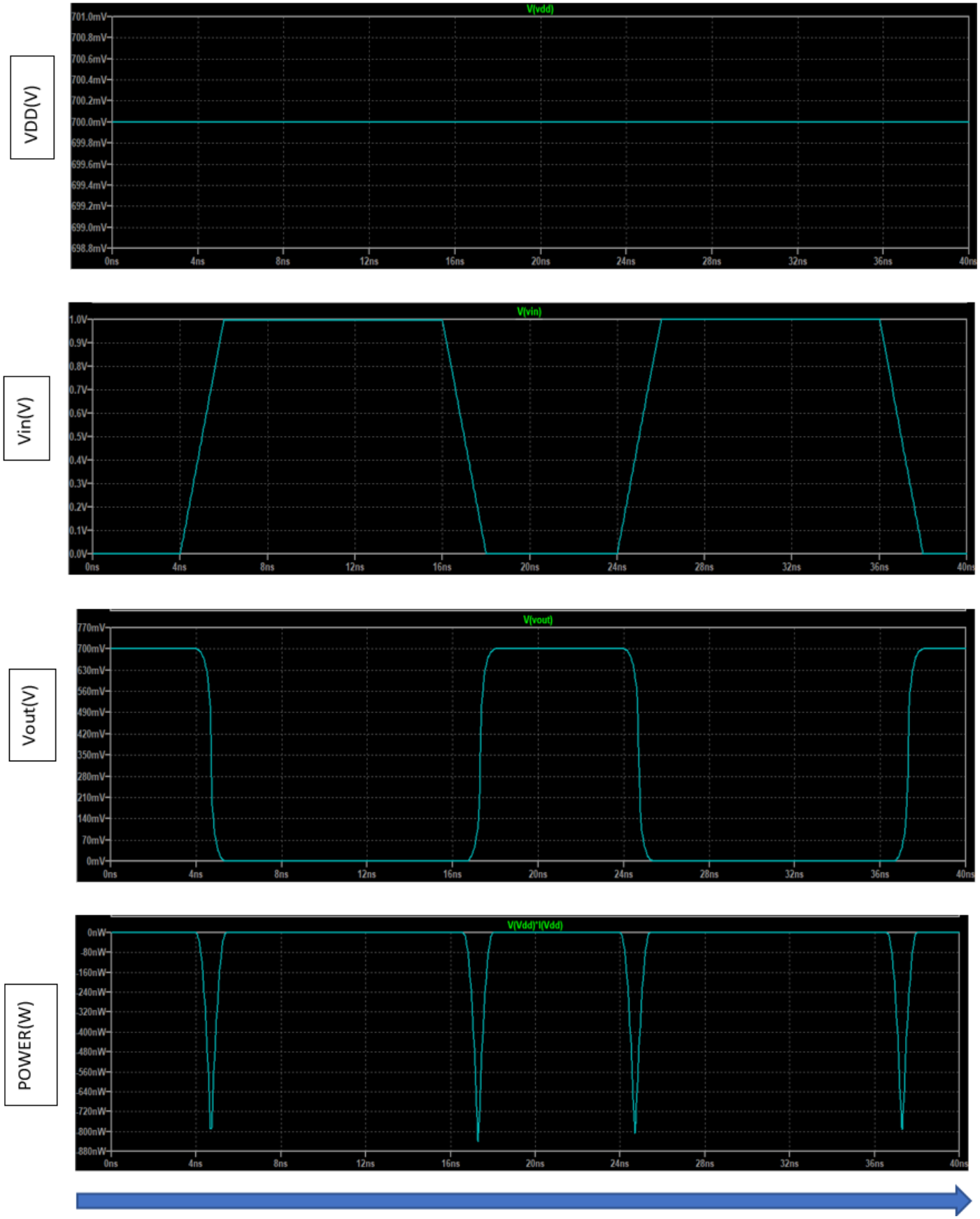

Time scale of 0-40ns

Fig 4. Inverter based on MoS_2 transistor. Vdd, Vin, Vout, power.

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Table 1 technology parameters used in the model of inverter

Technology Node	vdd(v)	vth(v)
16nm	0.7	0.29
10nm	0.65	0.27
7nm	0.6	0.25

Table 2 technology parameters used in the model of op-amp

Transistors	w(µm)	l(µm)	w/l
m1, m2	5	10	0.5
m3-6, m8, m10, m12	150	5	30
m7, m9	5	20	0.25
m11	25	5	5

III. SIMULATION RESULTS

We simulated the mos_2fet inverter by considering the channel lengths 0.016 µm,1.010 µm and 0.007 µm. spice simulations are carried out by using the spice model and tested the inverter. in an attempt to have an accurate simulation describing the mos_2fet, we have used parameter sets from table 1. in our simulations, mos_2fet characteristics are verified from channel lengths 0.016 µm, 0.010 µm, 0.007 µm. the models are simulated for vdd values from 0.6 v to 1 v to check the results of threshold voltages.

the results of the simulation of the operational amplifiers using the dimensions shown in the table 2. the bias current was set using an external current source and adjusted for best performance of the device around typical values of ib=5-10µa. large-signal d.c. sweeps were performed to determine the characteristics of the OPA under static conditions, and the voltage at the positive input was swept twice from negative to positive voltage and back (differential mode dm). the resulting curve did not exhibit any measurable hysteresis, and the swing of the output voltage showed a gain of 33db and a large voltage swing of almost 15v, with the best device showing a low-frequency gain of 36db. however, these gain values were smaller than what is typically obtained in commercial OPAs (>60db). to test the common-mode rejection ratio, a concurrent sweep of both inputs was performed, which should result in a constant output. small variations during manufacturing can cause asymmetries in the circuit that result in a non-zero slope of the output voltage. however, the cm measurement showed only insignificant changes in the output voltage, and a cm rejection ratio of ~50db was extracted. the frequency response of the device was characterized using low-amplitude sine waves of varying frequency, yielding a maximum gain of 33db rolling off at ~5 khz and a unity-gain transition frequency of ft=0.3mhz. the high-frequency operation of the devices was mainly limited by the current driving capabilities of the transistors, but a more advanced design could significantly increase the operation frequency. the OPA was found to have a phase margin of less than 60°.

IV. CONCLUSION

The single layer mos_2 transistor designed with 7nm, 10 nm, 16 nm, technology mos_2fets are modelled and analysed for their suitability for circuit levels by considering an inverter. the designed single layer mos_2 transistor and the systematic simulations for versatile inverter were carried out and verified. from the observations the mos_2fet utilizes much less power and outperforms si based cmos designs. this work can serve as a basis for designing large-scale electronic circuits using mos_2 with ease.

The designed and characterized operational amplifier (OPA) based on n-type enhancement-mode fets using the 2d semiconductor mos_2 as the active material. the low variability of the constituent components is crucial for the design of larger and more complex circuits. although the gain and bandwidth of the OPA are not as high as commercial silicon devices, it can already perform similarly to amplifiers based on other thin-film semiconductor technologies. moreover, the applicability of the OPA in typical feedback circuits and monolithic integration of a tmd photodetector with a tmd amplifier. this approach could provide a viable path to the future application of 2d semiconductors in analogue electronics with the development of more fault-tolerant circuit designs, improvements in processing and material quality, and the creation of cmos technology in 2d materials.

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