ISSN No:-2456-2165

Investigation and Comparative Study of a New Well Balanced Switches Losses Distribution Inverter

Mouna ESSAADI, Mohamed KHAFALLAH,
Laboratory: Energy & Electricals Systems (LESE).
ENSEM, Hassan II
University BP 8118, Oasis, Casablanca, Morocco.

Hamid CHAIKHY
Ecole Nationale des Sciences Appliquees,
Universite Chouaid Doukkali, El Jadida 24002, Morocco

Abstract:- This paper presents a comparative analysis between three levels neutral point clamped inverter (3L_NPC), and three levels neutral piloted point inverter (3L_NPP). Those different topologies are compared by simulation in term of many performances, as switches loss distribution which is well balanced and reduced for 3L_NPP inverter, unlike the 3L_NPC inverter. Finally, a summary of the comparative analysis is presented.

Keywords:- *Multilevel Inverter, 3L_NPC Inverter , 3L_NPP, Switches Loss Distrubution.*

I. INTRODUCTION

Due to the high global energy demand, huge consumption of fossil fuels has increased. Then, by the dint of greenhouse gases the atmosphere and the environment have been influenced. Therefore, development of almost zero pollution alternatives as electric vehicles require nowadays special attention. The fast progress of those modern vehicles requires high performances inverters [1-6]. Thanks to many benefits that increases multilevel inverters power density, this new generation of inverters have currently acquired scholar's attention. High equivalent switching frequency, low voltage stress, low THD, high efficiency, reduced electromagnetic interference (EMI) are the main advantages of multilevel inverters compared to Two levels inverters. [7-10]

3L_NPC (Figure.1) inverter is widely used in high power medium voltage applications [11] [12]. The major disadvantage of this topology is the unequal loss distribution among the switches; however, it also generates unequal junction temperature distribution which confines the inverter maximum output power [13]. Moreover, as the levels of the inverter increase the unequal switching of the semiconductor devices also increase and so the voltage unbalance between the DC link capacitors. As the neutral point is actively piloted, 3L_NPP (Figure.2) is an attractive topology which can overcome the unequal loss distribution problem of the 3L_NPC inverter and improve the power ability [14-16]. In 3L_NPP inverter topology, two switches connected in series are added for the purpose of clamping instead of clamping diodes as in 3L_NPC. In this work, 3L_NPC and 3L_NPP inverter will be presented in detail and compared by simulation in term of total losses and efficiency.

II. 3L_NPC INVERTER

To overcome the different drawbacks of two levels inverter, the 3L_NPC inverter is presented. [17]

➢ *Structure:*

The structure of the three levels 3L_NPC inverter is shown in Fig.1

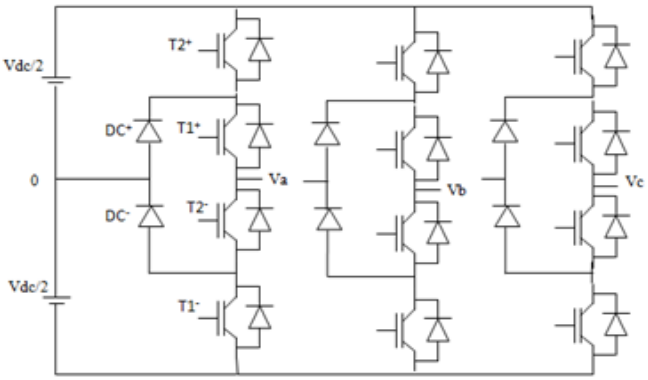

Fig 1 Three Levels 3L_NPC Inverter

➢ *Principle:*

3L_NPC inverter gives three voltage levels : Vdc/2, 0, -Vdc/2.(Fig.1). Table.1 summarizes switching states which gives three levels voltage.

Table 1 Basic Switching of 3l_Npc Inverter

Voltage level	**Voltage Va**	**Switching state**			
		T2+	***T1+***	***T2-***	***1-***
1	**Vdc/2**	1	1	0	0
0	**0**	0	1	1	0
-1	**-Vdc/2**	0	0	1	1

➢ *Control Strategy:*

As shown in Fig.2, a pulse width modulation (PWM) with two triangular carriers is used to control the switches as presented in table.1. The voltage Va and Vab are presented in Fig 5

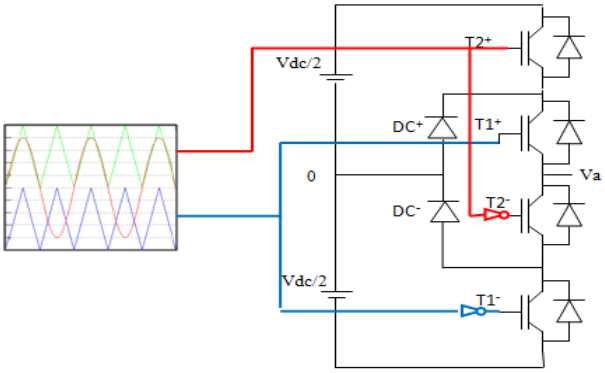

Fig 2 Two Carriers PWM Control Strategy of 3L_NPC Inverter

III. 3L_NPP INVERTER

➢ *Structure:*

The structure of the three levels 3L_NPP inverter is shown in Fig.3

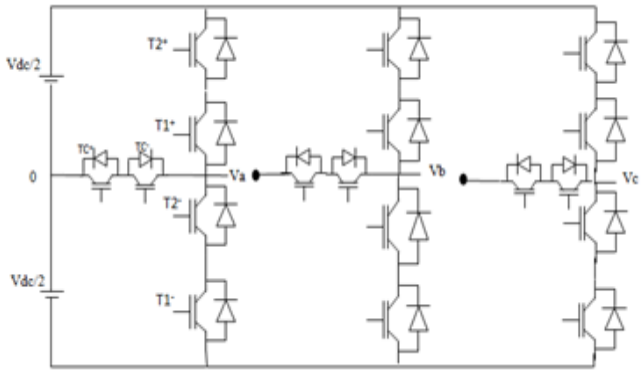

Fig 3 Structure of the 3L_NPP Inverter

➢ *Principle:*

3L_NPP inverter gives three voltage levels : Vdc/2, 0, -Vdc/2.(Fig.3). Table.2 summarizes switching states which gives three voltage levels [2]

Table 2 Basic Switching of 3L_NPP Inverter

Voltage level	**Voltage Va**	**Switching state**					
		T2+	***T1+***	***TC+***	***T2-***	***1-***	***TC-***
1	**Vdc/2**	1	1	1	0	0	0
0	**0**	0	0	1	0	0	1
-1	**-Vdc/2**	0	0	0	1	1	1

➢ *Control Strategy:*

As shown in Fig.4, a pulse width modulation (PWM) with two triangular carriers is used to control the switches as presented in table.2.

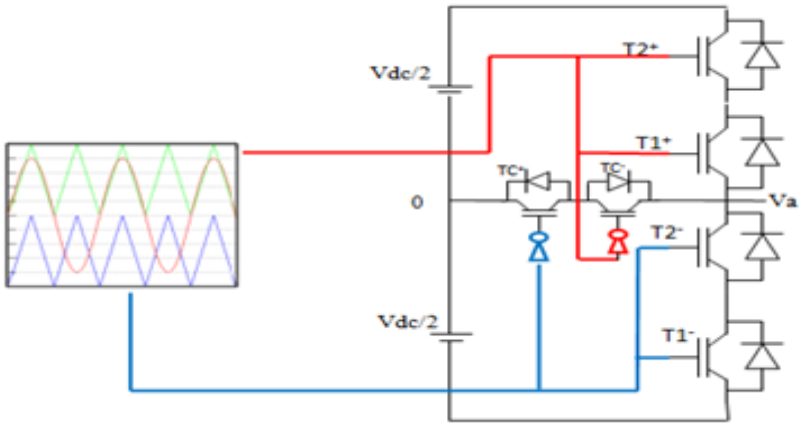

Fig 4 Two Carriers PWM Control Strategy of 3L_NPP Inverter

As presented in Fig.4 T2+ and T1+ are simultaneously controlled, knowing that switches have not always the same characteristics one of the two switches may be in off state before the other. So, one of them will assume a very important voltage which can deteriorate it. A balancing system must be used in this case. The voltage Va and Vab are presented in Fig 5.

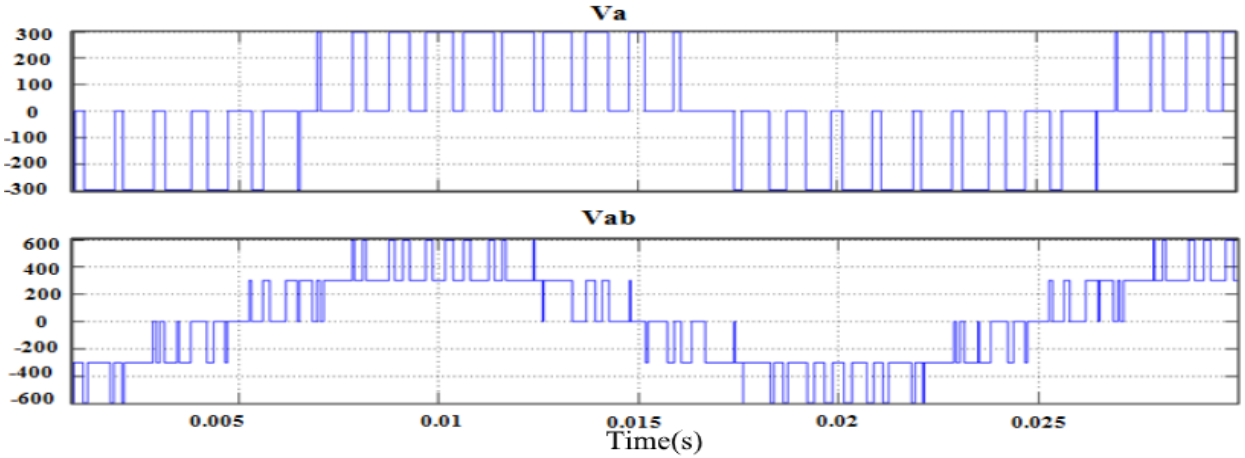

Fig 5 Three Voltage Levels in the 3L_NPC and 3L_NPP Inverter

IV. TOTAL LOSSES IN THE INVERTER

Total Losses in the Inverter are Defined in (Eq.1):

$$P_{total} = P_{switch} + P_{cond} \quad \text{(Eq.1)}$$

➢ *Conduction Losses:*

Average transistor conduction losses are defined in (Eq.2):

$$P_{cond}(T_i) = V_{cesat} I_{cAVG} + R_s I_{cRMS}^2 \quad \text{(Eq.2)}$$

- V_{cesat} : The threshold voltage, I_{cAVG} : Average value of the IGBT instantaneous commutation current, R_s : On-state resistance of the IGBT, I_{cRMS} : RMS value of the IGBT instantaneous commutation current.
- V_{cesat} and R_s are directly extracted from inverter's datasheet
- I_{cAVG} and I_{cRMS} are measured from Matlab/Simulink model of the inverter.

Average clamping diode and anti-parallel diode conduction losses are defined respectively in (Eq.3) and (Eq.4):

$$P_{cond}(D_{clamping}) = V_{sc} I_{dcAVG} + R_{dc} I_{dRMS}^2 \quad \text{(Eq.3)}$$

$$P_{cond}(D_{antiparallel}) = V_{si} I_{diAVG} + R_{di} I_{diRMS}^2 \quad \text{(Eq.4)}$$

- V_{sc}: Forward voltage drop for clamping diode
- V_{si}: Forward voltage drop for anti parallel diode
- R_{di}: On-resistance of the anti parallel diode
- R_{dc}: On-resistance of the clamping diode
- I_{dcRMS}: On –state clamping diode RMS current.
- I_{diRMS}: On –state anti-parallel diode RMS current
- I_{dcAVG}: On –state clamping diode average current.
- I_{diAVG}: On –state anti-parallel diode average current.

V_{sc},V_{si}, R_{di} and R_{dc} are directly extracted from inverter's datasheet. I_{dcRMS}, I_{diRMS}, I_{dcAVG} and I_{diAVG} are measured from Matlab/Simulink model of the inverter.

➢ *Switching Losses:*

Average transistor switching losses are defined in (Eq.5):

$$P_{com}(T_i) = F_{pwm}(E_{on} + E_{off}) \quad \text{(Eq.5)}$$

Average diode switching losses are defined in (Eq.6):

$$P_{com}(D_i) = F_{pwm}(E_{rr}) \quad \text{(Eq.6)}$$

F_{pwm}: switching frequency, E_{on}: On-state energy of the transistor, E_{off}: Off state energy of the transistor, E_{rr}: reverse recovery energy, E_{on}, E_{off} and E_{rr} are extracted from invert's datasheet.

V. SIMULATION RESULTS AND DISCUSSION

3L_NPC and 3L_NPP topologies are simulated in Matlab/Simulink environment. To obtain simulation results of Fig.6 control strategies of Fig.2 and Fig.4 are used. Parameters of IGBTs and diodes are based on the Miniskiip 3L_NPC inverter's Datasheet from Semikron.[19]

As presented in Fig.6 The two topologies present practically the same current distortions and for both the voltage present clearly tree levels. But the differrence is in the loss distribution where the 3L_NPP topology present more balanced losses compared to the 3L_NPC topology because the two clamped diodes are replaced by the two IGBT's. Both 3L_NPP and 3L_NPC inverters have a very good efficiency (98.5%) compared to the classical two levels inverter (95%).

Table 3 Comparison Between 3L_NPC And 3L_NPP Topology

Inverter Topology	3L_NPC	3L_NPP
ADVANTAGES	Can be used for more than 3 levels	Balanced loss distribution
DISADVANTAGES	Unbalanced loss distribution	Need a voltage balance system for the series connected IGBTs

VI. CONCLUSION

In this paper a comparative analysis between two multilevel topologies: 3L_NPC and 3L_NPP have been presented. This work began by explaining the structure, the principle and the control strategy of the 3L_NPC and 3L_NPP.The paper presents later a discussion based on the simulation results presented in the same work. It's clear that, in term of equal losses distribution and even reduction of switching losses, 3L_NPP still better than 3L_NPC topology, even if this one reduces off-state voltage and switching frequency compared to two levels inverter. Surely 3L_NPP topology is a very attractive topology but has disadvantages like balancing system for series switches.

REFERENCES

[1]. Bughneda, M.Salem , A. Richelli , D. Ishak and S. Alatai, Review of Multilevel Inverters for PV Energy System Applications , Energies 2021, 14, 1585. https://doi.org/10.3390/en14061585

[2]. Y. ye , (Member, IEEE), G. zhang, J. huang, S. chen, and X. wang, Comparative Analysis of Hybrid NPP and NPC Seven-Level Inverter With Switched-Capacitor, volume 9, 2021 85852--- 85863 IEEE ACCESS

[3]. Nema, P.; Nema, R.; Rangnekar, S. A current and future state of art development of hybrid energy system using wind and PV-solar: A review. Renew. Sustain. Energy Rev. 2009, 13, 2096–2103.

[4]. L. Franquelo, J. Rodriguez, J. Leon, S. Kouro, R. Portillo, and M. Prats, ''The age of multilevel converters arrives,'' IEEE Ind. Electron. Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.

[5]. Z. Yao, Y. Zhang, and X. Hu, ''Transformerless grid-connected PV inverter without common mode leakage current and shoot-through problems,'' IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 67, no. 12, pp. 3257–3261, Dec. 2020.

[6]. Omer, P.; Kumar, J.; Surjan, B.S. A Review on Reduced Switch Count Multilevel Inverter Topologies. IEEE Access 2020, 8, 22281–22302.

[7]. G.Chen, J.Yang, A Modified Modulation Strategy for an Active Neutral-Point-Clamped Five-Level Converter in a 1500 V PV System Electronics 2022, 11, 2289. https://doi.org/10.3390/electronics11152289

[8]. Swetha and V. Sivachidambaranathan, A Nonlinear Controller for Neutral Point Piloted (T-Type) Multilevel Inverter-Based Three-Phase Four-Wire DSTATCOM K. Hindawi International Transactions on Electrical Energy Systems Volume 2022, Article ID 7899765, 16 pages https://doi.org/10.1155/2022/7899765

[9]. Prathaban, A.V.; Dhandapani, K.; Abubakar, A.I.S. Compact Thirteen-Level Inverter for PV Applications. Energies 2022, 15, 2808.

[10]. Gupta, K.K.; Ranjan, A.; Bhatnagar, P.; Sahu, L.K.; Jain, S. Multilevel Inverter Topologies with Reduced Device Count: A Review. IEEE Trans. Power Electron. 2016, 31, 135–151.

[11]. J. Rodriguez, S. Bernet, P. Steimer, and I. Lizama, "A survey on neyutral-point-clamped inverters," IEEE Trans. Ind. Electron., no.7, pp. 2219-2230, July 2010.

[12]. J. Rodriguez, J. Lai, and F. Peng, "Multilevel Inverters; a survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., Vol.49, no. 4, pp. 724-738, Aug. 2002.

[13]. T. Bruckner, S. Bernet and P. Steimer, "Feed farward loss control of three level active 3L_NPC converters", IEEE Trans. On Ind. Appl., vol. 43, no. 6, pp. 1588-1596, Dec. 2007

[14]. V. Guennegues ; B. Gollentz ; F. Meibody-Tabar ; S. Rael ; A converter topology for high speed motor drive applications; 13th European Conference on Power Electronics and Applications, 2009. EPE '09, Barcelona.

[15]. C.Benzazah, M. Ait Lafkih, L.Lazrak, Comparative study between two topologies three phases inverters conventional two-level and three level with two methods different of control, SPWM and SWM International Journal of Innovation and Applied Studies ISSN 2028-9324 Vol. 9 No. 2 Nov. 2014, pp. 841-852© 2014 Innovative Space of Scientific Research Journals.

[16]. N.Schibili, T.Nguyen, A.Rufer, IEEE trans, A Three-Phase Multilevel Converter for High-Power Induction Motors On Power Elect. Vol. 13 N°.5(1998).

[17]. P. Mehta, A. Kunapara Investigations on a 3L_NPC Multilevel Inverter used for Even loss Balancing International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169 Volume: 3 Issue: 2 025– 027 February 2015.

[18]. A.Nabae A new neutral-point-clamped PWM inverter , IEEE Transactions on Industry Applications, vol. IA-I7, Septembre/Octobre 1981.

[19]. Staudt, Technical explanation 3L SKiiP28MLI07E3V1 Evaluation Inverter, 2014, semikron international GmbH P.O.

[20]. Nuremberg • Germany.

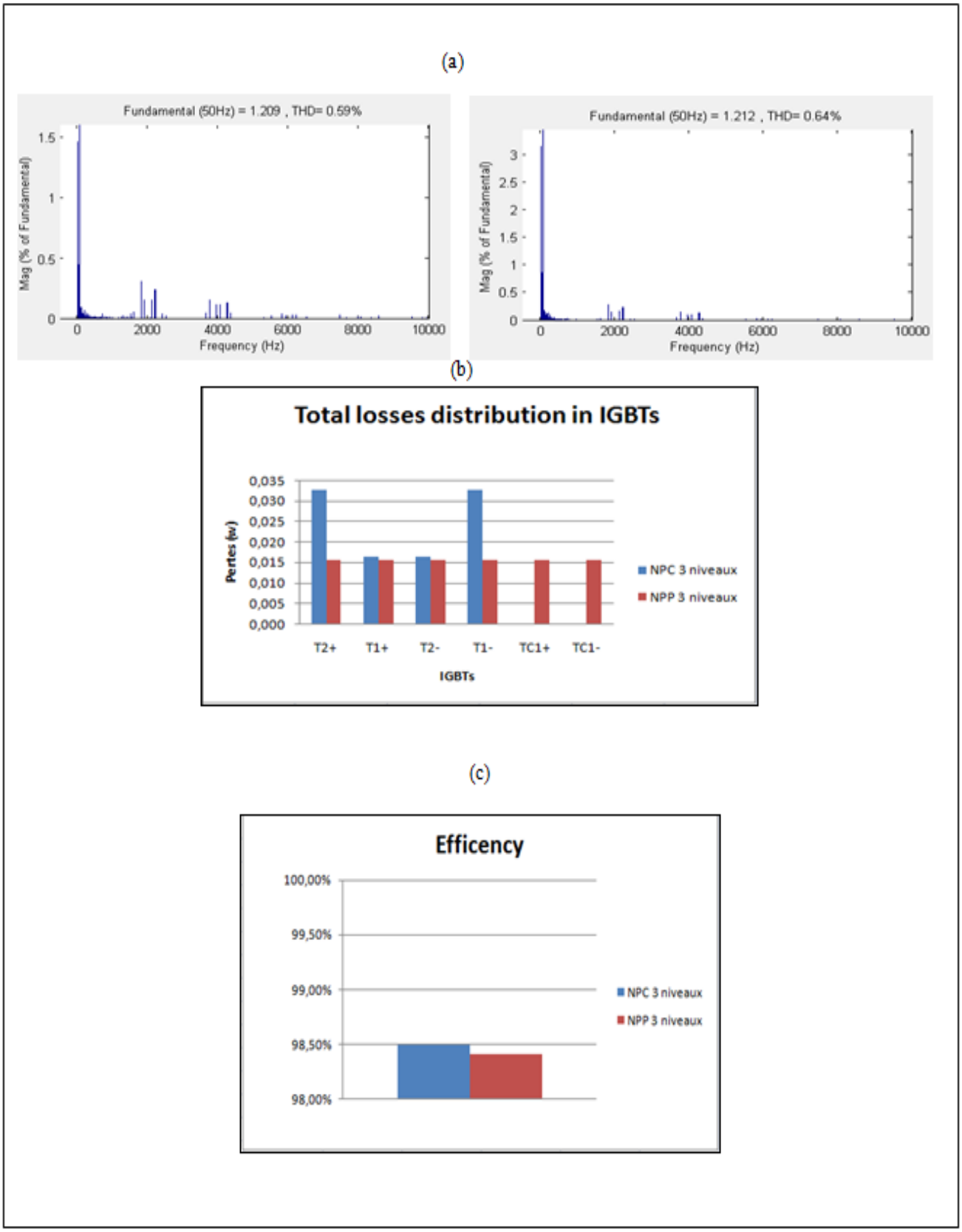

Fig 6 Comparison Between the 3l_NPC and 3l_NPP Inverters in Term of (A) THD (B) Losses Distribution in IGBTS and (C) Efficiency