PCB Stackup Design for Modern Electronics

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Abstract:- Printed Circuit Boards (PCBs) Stackup is the arrangement of different layers to make up a PCB and it involves determining the number of layers, their order, and the materials used for each layer. The Stackup design plays an important role in the PCB design, as it directly impacts the performance, signal integrity, durability, reducing the electromagnetic emissions, and overall functionality of the electronic device. It is core related to the PCB Material and lamination process based on layer count, prepreg/Core material, thickness of each layer's, copper weight, via type, drilling type, layers ordering, and high-speed impedance control requirements. As modern AI/AR electronic products become more compact and complex, careful consideration of the PCB stackup becomes even more critical. In this article, we explore the key factors and strategies for optimizing PCB stackup to achieve enhanced signal integrity and performance.

Keywords:- *PCB Laminations, Copper Weight, Signal Layers, Lamination Materials, Power Plane, Strip Line, Micro-Strip Line, Impedance Control, EMI, EMC, Single Ply-Dual Ply, DK, TG, and CTE.*

Stackup design in Printed circuit boards requires careful consideration of whether it is a Low-Speed/High-Speed or Power supply-based design. Low-speed or DC general application products may not require impedance-controlled Stackup and high-speed laminate materials. Generally, FR4 is the commonly used low-cost material that will be globally available to buy in the market which will save time in terms of procuring material.

The design of a PCB Stackup plays a pivotal role in determining the overall performance, signal integrity, and reliability of electronic devices. Impedance-controlled High-speed Stackup design is the critical part of the High-speed Printed Circuit Board

The process involves identifying the application, circuit type, PCB thickness, number of layer requirements, laminate material selection, Via/Drilling types, manufacturing feasibility, and Signal/Power layer construction including symmetrical stacking, and reliability considerations.

The laminate materials affect the overall dielectric constant and loss tangent, which directly impact signal propagation and signal integrity. High-frequency designs may benefit from low-loss materials. Required symmetrical Stackup design to improve mechanical stability, reducing the risk of warping. Staggering signal layers can minimize signal coupling and crosstalk between adjacent layers.

It's important to note that the PCB Stackup design will depend on the specific requirements of the product design. Consult with a PCB fabricator based on material availability in the region which meets the regulations and standards for PCB manufacturing. Using simulation and PCB design tools is the best way to ensure the best Stackup for the design based on the application. Impedance control with Power Plane /Signal Layers stack calculation and manufacturability is an important factor when designing Stackup.

I. PCB STACKUP LAYERS

PCB Stackups can be classified into various types based on the number of layers and their order in the Stackup. The first consideration for the PCB Stackup is determining how many layers are needed. This includes application, signal speed, power, and GND/Power plane requirements.

➢ *Single-Layer Stackup*

Single-sided PCBs Consist of a single conductive layer and substrate material on one side. The Stackup structure starts with a soldermask layer, a conductive layer, and a thick FR4 Prepreg/Core material (usually 1.6mm thickness). Ideal for simple and low-cost applications with minimal complexity, such as simple Power supplies, switches, and sensors. This is a low-cost/easily manufacturable option with single-side component assembly. SMT and through-hole components assembly can be done on the single-layer PCB Stackup with the through-hole Drill.

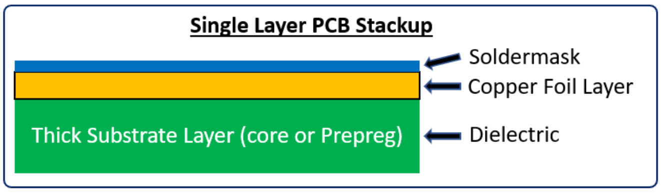


Fig 1 Single-Layer Stackup

➢ *Double-Layer Stackup*

Double-sided PCBs Consist of a dual conductive layer on both sides of the PCB (Top and Bottom) separated by substrate material (Commonly FR4 Prepreg/Core). The Stackup structure contains a Soldermask Top/Bottom, conductive layers Top/Bottom layers (usually copper/Aluminum), and a thick FR4 Prepreg/Core material (usually 0.5 to 1.6mm thickness). Ideal for most industrial product applications such as Power supplies, Industrial Controllers, switches, Power converters, and sensors. This type of Stackup is easy to manufacture and can do both top and bottom side assembly. SMT and through-hole components assembly can be done on the Double-layer PCB Stackup with the through-hole Drill.

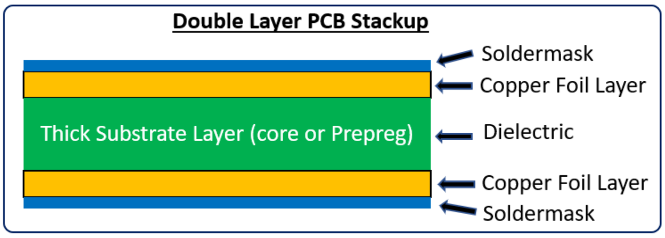


Fig 2 Double-layer Stackup

➢ *Multi-Layer Stackup*

Multilayer PCB stackup contains top and bottom layers and there are no limits for inner layers. The Standard PCB Stackup is available on the market from 2 to 24 layers (In some cases up to 32 layers) depending on how complex and the application requirements. With advanced technology like the Laser Imaging process, layer count can go up to 64 layers with higher costs. Multi-layer Stackup consists of dual outer conductive layers (Commonly copper) on both sides of the PCB (Top and Bottom), The inner layers will be also copper layers separated by substrate material (Prepreg/Core based on application requirements).

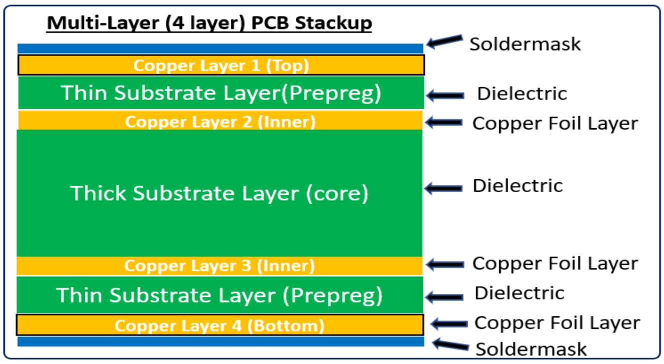


Fig 3 Multi-Layer Stackup 1 (4-Layer)

Figure 3 shows a typical 4-layer stack-up known as an entry-level stackup, Ideal for any industrial product, and the PCB thickness varies from 0.5mm to 1.6mm based on design application. Through hole Vias/Drill widely used for this type of Stackup.

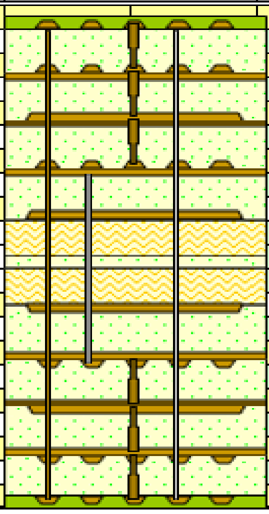
Layer	Cu Thick. (mils)	Cu Foil wt (oz)	Stackup Figure	DK	Lam. Thick. (mils)	Material
1	2.05	.375 oz				Foil .375 oz
				2.97	4.01	Prepreg Tachyon 100G 1078(75)
2	0.65	.375 oz				Foil .375 oz
				2.97	3.84	Prepreg Tachyon 100G 1078(75)
3	0.65	.375 oz				Foil .375 oz
				2.97	3.81	Prepreg Tachyon 100G 1078(75)
4	1.15	.375 oz				Foil .375 oz
				2.97	3.95	Prepreg Tachyon 100G 1078(75)
5	0.60	0.5 oz				
				3.15	14.00	Core Tachyon 100G 14.00mils 3x3313
				3.04	10.20	Prepreg Tachyon 100G 1078(70.5)
				3.15	14.00	Core Tachyon 100G 14.00mils 3x3313
6	0.60	0.5 oz				
				2.97	3.95	Prepreg Tachyon 100G 1078(75)
7	1.15	.375 oz				Foil .375 oz
				2.97	3.81	Prepreg Tachyon 100G 1078(75)
8	0.65	.375 oz				Foil .375 oz
				2.97	3.84	Prepreg Tachyon 100G 1078(75)
9	0.65	.375 oz				Foil .375 oz
				2.97	4.01	Prepreg Tachyon 100G 1078(75)
10	2.05	.375 oz				Foil .375 oz

Fig 4 Multi-Layer Stackup 2 (10- Layer)

Figure 4 shows a typical Multilayer (10-layer) stack-up with Isola Tachyon 100G lamination material, Ideal for impedance-controlled PCB lamination with a combination of core/Prepreg materials. Balanced stacking is recommended to build this type of multi-layer PCB Stackup. Vias/Drill can be through holes or Micro-Vias/Blind/Buried. PCB thickness for this type of Stackup can vary based on the layer count and application requirements vary from 0.5mm to 3mm.

When complex routing space and signal integrity are required, multilayer PCB stackup meets these demands. Multilayer Stackup has multiple conductive and insulating materials to create a complex network connection.

II. PCB STACKUP TYPES

The choice of PCB Stackup depends on the design's complexity, performance requirements, signal speeds, thermal considerations, and cost constraints. Designers must carefully evaluate the application needs to select the most suitable PCB Stackup for optimal performance and reliability.

There are several types of PCB stack-ups available, each tailored to meet specific design requirements and application needs. Here are some common types of PCB Stackups:

ISSN No:-2456-2165

A. Rigid PCB Stackup

The Rigid PCB stackup refers to the arrangement and composition of layers in a printed circuit board (PCB) that do not have flexibility or bending capabilities. Rigid PCBs are commonly used in a wide range of electronic devices and applications where the board is not subjected to significant bending, flexing, or mechanical stress. This is known as the standard PCB stack-up widely used in most electronics products that include several layers, each serving specific functions and containing various components and traces. There are a few elements in a PCB stack-up.

➢ *External Layers (Top and Bottom)*

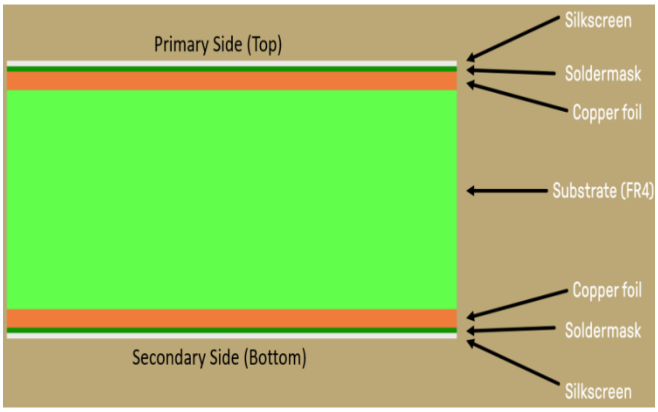


Fig 5 PCB Stackup Outer Layers

Fig-5 shows the typical external layers construction with Silkscreen, soldier mask, and copper foil.

- *Signal Layers:*

The external signal layers whether it is the top or bottom contain conductive material, commonly copper with 0.5Oz to 2.5Oz copper weight based on application.

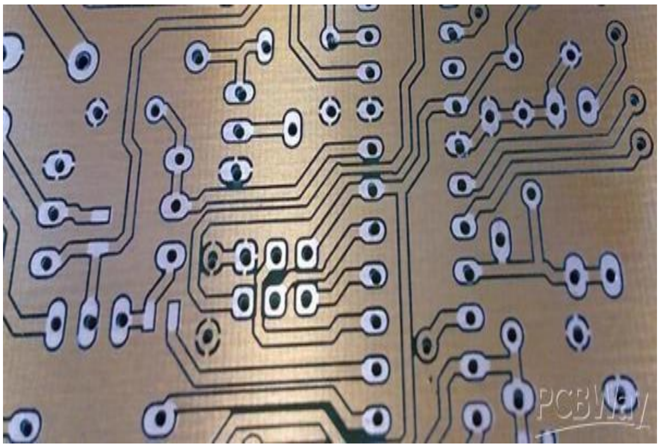


Fig 6 Outer Layers of Copper

Fig-6 shows a PCB outer layer conductive copper Layer without a solder mask.

- *Soldermask Layer:*

Solder mask layers (Solder resist) are applied to the top and bottom layers to cover the exposed copper traces and pads to protect from oxidation and to prevent solder bridges from the adjacent solder pads.

Fig-7 Shows the Soldermask with different color options on PCBs, The Soldermask comes in different color options like Red, Blue, White, Black, and Green, and it often comes with 18um to 25um thickness.

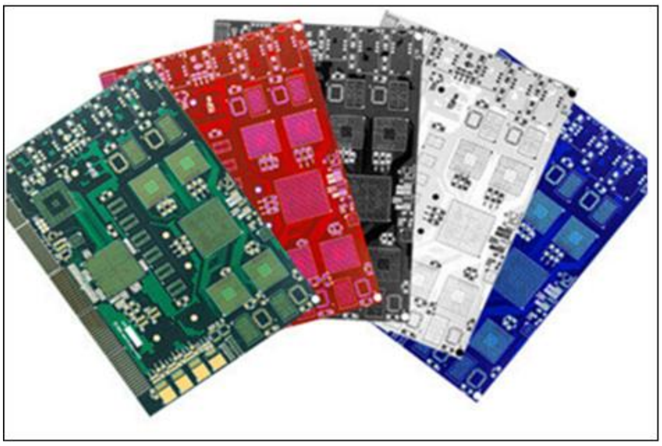


Fig 7 Solder Mask in PCBs

- *Surface Finish:*

The surface finish is a coating applied to exposed copper areas to prevent oxidation and improve solderability. Common surface finishes include HASL (Hot Air Solder Leveling), ENIG (Electroless Nickel Immersion Gold), and immersion tin. In some cases, like the Finger edge connector, gold plating is recommended.

- *Silkscreen Marking Layer:*

This layer uses completely white ink to represent component outlines, Pin numbers, Test points, Logos, markings, and reference Designators (REFDES).

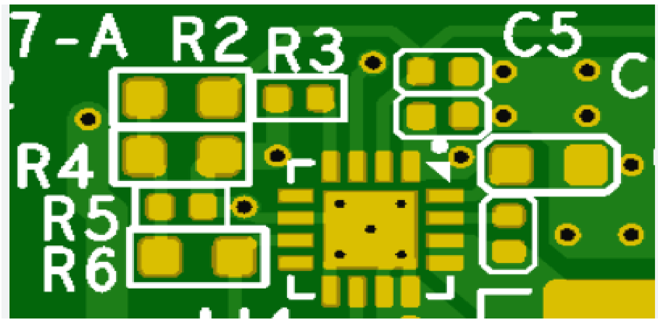


Fig 8 Silkscreen Marking in PCBs

Fig-8 shows the Silkscreen marking for the Components. There are several methods to print silkscreen on the board like Screen printing, Inkjet Printing, and Laser Printing.

➢ *Internal Layers*

Internal layers can be combinations of signal, power, and insulating dielectric layers.

- *Signal Layers:*

The Internal layers contain a conductive material, often copper weight with 0.5Oz to 1Oz based on the impedance and power requirements for electrical Signal routing.

ISSN No:-2456-2165

- *Power Plane Layers:*

The Internal layers contain conductive material, often copper with 0.5Oz to 2Oz copper weight based on power requirements for Power supply and ground electrical performance.

- *Prepreg Layers:*

Prepreg known as pre-impregnated, is a layer of fiberglass cloth impregnated with uncured epoxy resin, but without any attached copper foil. They separate signal and plane layers, providing electrical insulation and helping to define the overall board thickness and impedance requirements. Prepreg layers are positioned between the core and signal or plane layers, also prepreg acts as an insulator and adhesive in the stack up.

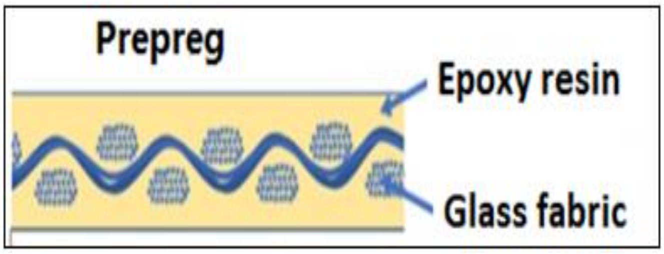


Fig 9 Prepreg Material

Fig-9 shows a prepreg material with Glass fabric and epoxy resin, in high temperatures the lamination process causes the epoxy resin in the prepreg to flow the layer together resulting in a solid and rigid board.

- *Core Layer:*

The core layer is often the central layer of the PCB stack-up for mechanical support/rigidity. This core material typically contains a thick, rigid substrate material with thin copper on both sides. It provides structural integrity to the PCB and serves as the foundation for the other layers such as Signal/GND.

The core layer may also include additional signal traces and the core layer will do a counterpart to increase or decrease the PCB thickness requirement for mechanical stability.

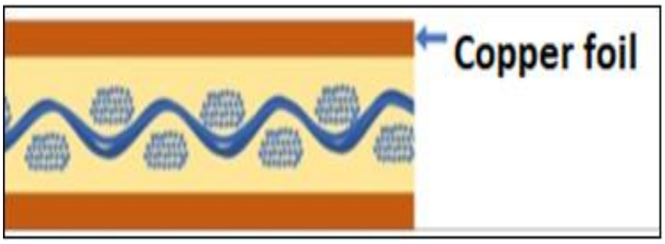


Fig 10 Core Material

Fig-10 shows a typical core laminate material made of a thin layer of copper foil bonded to a rigid substrate material. The copper foil on the core can serve multiple purposes such as providing a ground plane or a signal layer. In multi-layer PCBs, there can be multiple core layers with prepreg layers between each core layer and the outer copper layers.

B. *Flex PCB Stackup*

A Flex PCB is Designed for applications requiring flexibility, such as wearable devices or curved surfaces. Utilizes flexible substrate laminate materials, such as polyimide, and may have single or multiple flexible layers. It is composed of an insulating substrate, a conductive layer and there is an adhesive between the layers.

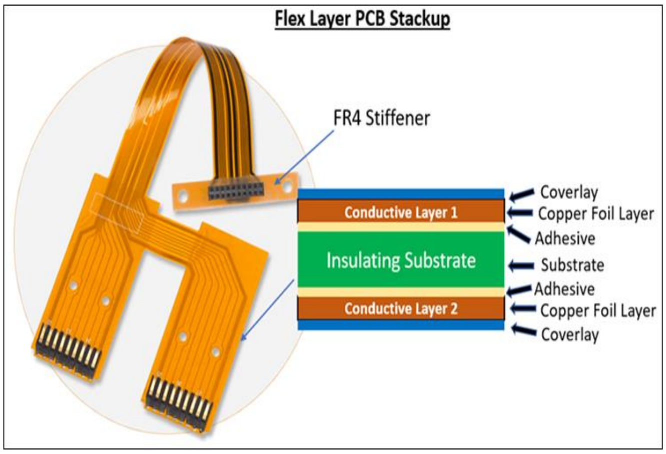


Fig 11 Flex PCB Stackup

Fig-11 shows the fundamental structure of the Flex PCB stack-up. Like Rigid PCB stack-up, Flex PCB stack-up requires external conductive signal Layers, surface finish, Silkscreen layer, and Soldermask. A few elements differ from the rigid stack-up listed below.

- *Coverlay:*

Flex PCB circuit required Soldermask with great bendability due to the flexibility. Coverlay serves as a Soldermask on the Flex PCB to protect the outer conductive layer.

- *Substrate Material:*

The base material used in most of the Flex PCBs is Polyimide (PL). This material is very tough, very flexible, and has high heat resistance.

- *Adhesive*:

This is an acrylic or epoxy material to bonds the Flex PCB insulating material and the conductive layer by applying pressure and heat.

- *Stiffener:*

Flex PCB is a thin and flexible area that cannot hold components for assembly. A piece of stiffener can (Commonly FR4/Polyimide) be added to the flex PCB to provide rigidity for a specific area for component assembly on a flex PCB. A stiffener added to the Flex PCB is for mechanical support and assembly purposes only as a final fabrication process with adhesive.

C. *Rigid-Flex PCB Stackup*

Designed for applications requiring rigid/flexibility, Rigid-Flex PCB is a flexible hybrid circuit board combining elements of both flexible and rigid circuit boards. The shape of the rigid-flex is like a spring, if you stretch or compress it, it will return to its original state. This is a multilayer stack structure with a combination of three or more layers of rigid and two or more layers of flex areas that bond together (Fig-12: 2-layer Flex and Four-Layer Rigid configuration). The same as the above Rigid and flexible circuit board Stack-up design rules apply to the Rid-Flex PCB stack-up.

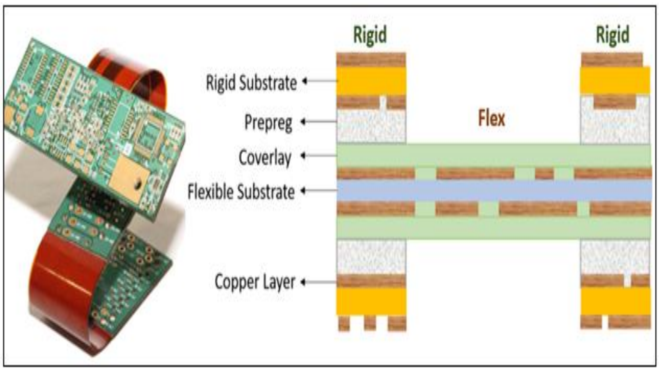


Fig 12 Rigid-Flex Multi-Layer Stackup

Rigid-flex PCBs are used in applications where the PCB must maintain electrical connections while being able to bend or flex to fit into non-standard or space-constrained geometries. The stack-up of a rigid-flex PCB is more complex than that of a purely rigid or Flexible PCB due to the combination of flexible and rigid materials. The arrangement and composition of layers in both rigid and flexible sections will be different, the Solder mask will be in the Rigid area where the flex area will be covered by Coverlay and adhesive and in some cases need stiffener.

III. PCB STACKUP OVERVIEW

Based on the Application requirements like Industrial, commercial, aerospace, defense, and medical PCB stack-up are demonstrated. It is tailored to the specific requirements of the PCB design, considering factors like signal integrity, thermal management, and mechanical flexibility. Here is the overview of PCB stack-up based on applications.

- *Standard PCB Stackup*

This is the most common type of PCB Stackup and is based on standard FR-4 (Flame Retardant 4) dielectric material. Typically used for low-to-medium complexity designs and offers good electrical and mechanical properties. Consists of signal layers and power/ground planes, often with a 2-layer to 8-layer configuration.

- *High-Speed PCB Stackup*

This is the widely used PCB Stackup for modern electronics products. Designed for high-frequency applications such as high-speed digital or RF circuits.

Utilizes specialized low-loss dielectric materials with a lower dielectric constant (εr) and low-loss tangent (δ) to minimize signal attenuation. This may include additional ground planes and specific layer ordering to improve signal integrity and reduce EMI.

- *Backplane PCB Stackup*

A backplane PCB Stackup is used for high-performance computing and networking applications. Backplanes serve as a central interconnection hub, providing a high-speed pathway for data transmission between various plug-in modules or daughter cards within a system. The stack-up of a backplane PCB is designed to handle high-speed signals, manage power distribution, and maintain signal integrity across multiple interconnected boards.

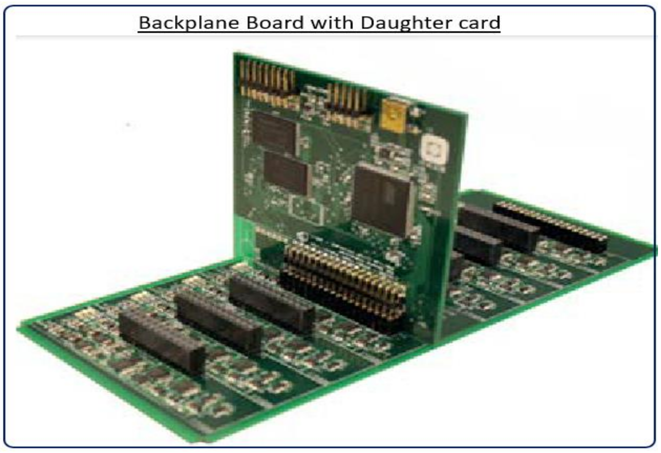


Fig 13 Backplane Board with Daughter card

Fig 13 Shows the backplane structure to understand the Stackup requirement. Backplane stack-up required higher thickness to hold the daughtercard/components' weight, often having a 6-to-32-layer count with impedance-controlled balanced stacking. High-speed materials with high performance, low dielectric constant, and low loss tangent are used to minimize signal attenuation and ensure high-speed signal propagation.

- *Metal Core PCB (MCPCB) Stackup*

Incorporates a metal core, such as aluminum, copper, or stainless steel instead of FR4 to provide effective heat dissipation for high-power applications. In high-power applications or environments with substantial heat generation, the thermal management of the PCB becomes crucial. To effectively dissipate heat and ensure reliable and stable operations, metal core PCBs are often used in PCB Stackup design. This metal core acts as a heatsink, efficiently conducting and dissipating heat generated by components on the PCB.

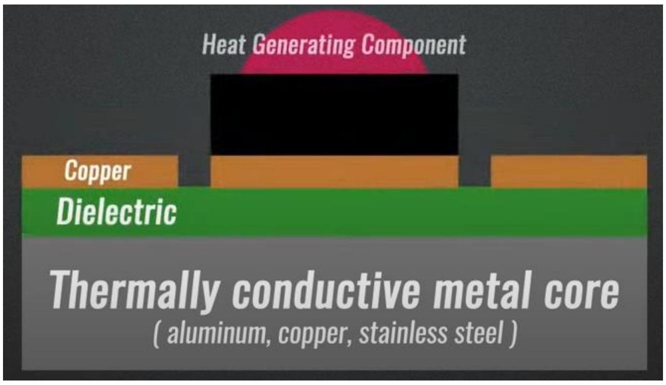


Fig 14 Metal Core Stackup

ISSN No:-2456-2165

Due to higher cost and heavyweight compared to standard PCBs, these materials can be used for specific compact devices such as Mobile phones/accessories, wearable devices, medical, automotive, and augmented reality (AR) devices.

➢ *Microwave PCB Stack-up*

Specifically designed for microwave and millimeter wave applications, known as a high-frequency PCB stackup, is designed specifically for applications that involve microwave frequencies (typically 1 GHz and above) or radiofrequency (RF) signals. These stack-ups are carefully engineered to maintain signal integrity, minimize signal losses, and control electromagnetic interference (EMI) at high frequencies.

Utilizes specialized high-frequency materials to handle extremely high frequencies with low dielectric constant (Dk) and low dissipation factor (Df). The wavelength of a signal in the air is less when running on a PCB due to the dielectric property of the material, so running a transmission line on a PCB requires careful consideration when choosing stackup materials.

➢ *HDI PCB Stackup*

HDI (High-density interconnect) printed circuit boards with a higher wiring density per unit area compared to standard PCB stack-ups. Standard PCB stackup, that relies on through-hole vias to interconnect layers. HDI stack-ups utilize micro-vias, Blind Vias, and buried vias to achieve higher routing density and better electrical, signal integrity performance.

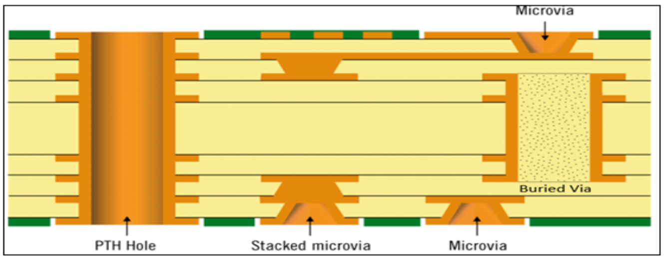


Fig 15 HDI Stackup

Fig-15 shows the X-N-X structure, this is a common way to describe the HDi stack-up configuration. X represents the number of HDI layers with micro vias, and N represents the number of core layers sandwiched between these HDi layers. With current technology, HDI PCB building cost is similar to standard PCB when they go for beyond 8-layer configuration. When going for an HDI stackup the size of the board reduces and it will help to support miniaturization products.

➢ *Sequential Lamination Stackup*

Sequential lamination is the most feasible solution to build multiple-layer stack-ups with advanced via structures. Lamination materials use two or more subsets created individually and bond together for specific impedance requirements. It enables complex inner layer routing with blind and buried vias with two or more than four lamination cycles depending on the combination of the PCB substrate material.

It also offers an excellent solution to achieve a consistent aspect ratio on all drills and provide precise impedance control for critical signals. Fig-16 is a four-lamination cycle process with 20Ghz halogen-free EM-526 Core and EM-89BK high-speed laminate materials. Try to keep the number of lamination cycles between two to three, increasing the number of Lamination cycles means the cost and fabrication time also will increase.

	mil	um	Dk@20GHz	Df@20GHz	Dielectric	Material Destription	Trace Width	Trace space	Via / Pad	Via Type	
SMT	0.98	25	3.0@20GHz	0.016@20GHz	SM	SR-1					
Layer1	1.18	30					100	100	125/225		4th lamination
D12	4.65	118	2.97	0.0026	Prepreg	EM-89BK				Micro Via 1-2 Copper Fill	
Layer2	1.18	30					100	100	125/225		3rd lamination
D23	4.65	118	2.97	0.0026	Prepreg	EM-89BK				Micro Via 2-3 Copper Fill	
Layer3	1.18	30					100	100	125/225		2nd lamination
D34	4.65	118	2.97	0.0026	Prepreg	EM-89BK				Micro Via 3-4 Copper Fill	
Layer 4	1.18	30					100	100	250/400		1st lamination
D45	4.65	118	2.97	0.0026	Prepreg	EM-89BK					
Layer 5	1.30	33					100	100			
Core	11.81	300	3.79	0.007	Core	EM-526				Through hole 4-7 Oganic Fill	
Layer 6	1.30	33					100	100			
D76	4.65	118	2.97	0.0026	Prepreg	EM-89BK					
Layer 7	1.18	30					100	100	250/400		1st lamination
D87	4.65	118	2.97	0.0026	Prepreg	EM-89BK				Micro Via 8-7 Copper Fill	
Layer 8	1.18	30					100	100	125/225		2nd lamination
D98	4.65	118	2.97	0.0026	Prepreg	EM-89BK				Micro Via 9-8 Copper Fill	
Layer 9	1.18	30					100	100	125/225		3rd lamination
D109	4.65	118	2.97	0.0026	Prepreg	EM-89BK				Micro Via 10-9 Copper Fill	
Layer 10	1.18	30					100	100	125/225		4th lamination
SMB	0.98	25	3.0@20GHz	0.016@20GHz	SM	SR-1					
SUM	62.99	1600.00									

Fig 16 Four Sequential Lamination Cycle

This process is packed with CTE (Coefficient of thermal expansion) which creates lamination void risk and copper extensions on the Z-axis with higher pressure and temperature during bonding materials. The increasing temperature of dielectric material will expand faster than the copper in some cases. The CTE of glass reinforcement is around 6ppm/^{O}C and the CTE of copper is around 17ppm/^{O}C and the CTE of resin is around 100ppm/^{O}C.

➢ *Hybrid PCB Stackup*

A hybrid PCB stackup is a combination of multiple Substrate materials to improve performance, multi-functionality, and design flexibility. It can be a combination of low-speed and high-speed lamination material or different application materials such as FR4+Aluminum, FR4+Metal core, and FR4+ceramic materials. Hybrid PCB stackup is used for handling better thermal management, power distribution miniaturization, and reliability. Hybrid PCB stackup provides higher efficiency and performance requiring a high degree of flexibility in stackup design such as a combination of metal layer for EMC shielding, and ceramic material for high frequency in a single board.

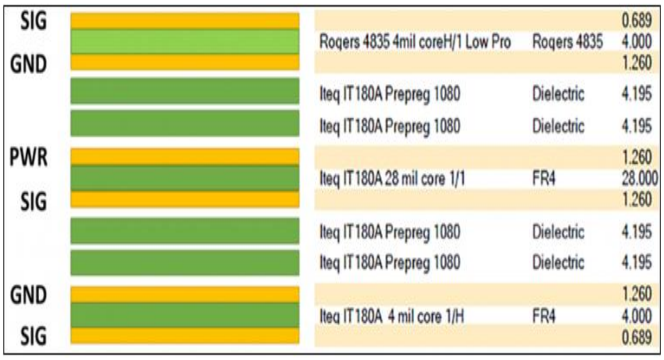


Fig 17 Hybrid Stackup

Fig-17 represents a simple hybrid lamination, Hybrid laminations are mostly expensive based on the combination, used in industrial applications such as communication Networks, Medical, Aerospace, and defense. Lamination Material selection for hybrid PCB stackup required special attention such as dielectric constant, surface roughness, and thickness based on impedance matching, cross talk, and signal integrity. Hybrid Stackup can be used in a PCB with multiple functionalities like Power supply and high-speed circuits to reduce board size.

➢ *Embedded Passive PCB Stackup*

The general PCB passive components assembly process is an SMD or through the hole. An embedded passive PCB stackup refers to integrating passive electronic components like resistors, capacitors, and inductors directly within the inner layers of a printed circuit board (PCB). These passive components are embedded into the PCB during the manufacturing process to save space, reduce interconnect lengths, enhance signal integrity, and improve overall PCB performance.

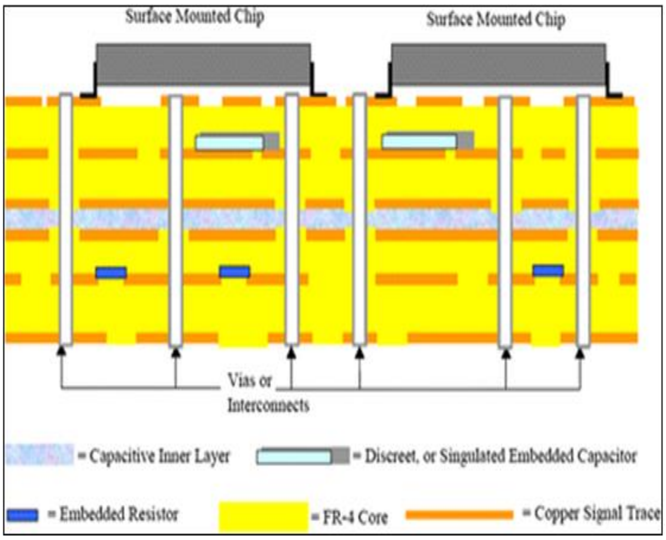


Fig 18 Embedded Stackup

These embedded components are patterned within the dielectric layers (Fig-18), and the planner resistive elements are made into a thin film that becomes part of the etched and printed circuitry on the PCB layers. Embedded component fabrication technology has a huge advantage over Surface-mounted assembly, it reduces board size, increases routing area, and improves electrical performance, and functionality within smaller spaces. The direct integration of passive components into the substrate reduces the parasitic capacitance and inductance, and the closer proximity of the passive components to the active components on the PCB. With advanced technologies active components also can embedded into the PCB's inner layer.

IV. STACKUP IMPEDANCE CALCULATION

There are several online calculators available in the market for calculating the Stackup dielectric thickness and conductive layer copper weight based on signal speed and power requirements. Even if we calculate the Stackup ourselves manufacturing approval is required based on the availability of materials and properties by the manufacturer. A few of the popular PCB toolkits are "Saturn and Polar Instruments" which have been widely used in the PCB Design industry for a long time. Identify the PCB manufacturer and consult with them about their capabilities and material availability to avoid a long period of material procurement time.

➢ *IPC 2141*

There are several methods to calculate the impedance and characterization of the PCB layer stackup. IPC-2141 standard calculation is one of the proven standards to calculate this. Some people use Excel spreadsheets with these formulas to calculate the impedance. Similar details can be found in the IPC-D-317A as well.

ISSN No:-2456-2165

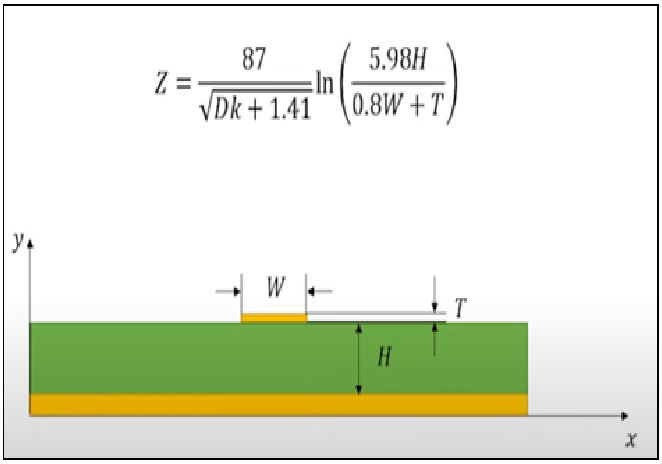


Fig 19 IPC 2141 Formula

➢ *Standard Impedance Calculation*

Calculating the impedance involves considering the properties of the dielectric material and trace width spacing of the transmission lines and the adjacent reference Power/GND plane layers.

$$Z = \frac{60}{\sqrt{2Dk+2}} \ln\left(1 + \frac{4H}{W'}\left[\left(\frac{14Dk+8}{11Dk}\right)\left(\frac{4H}{W'}\right) + \sqrt{\left(\frac{14Dk+8}{11Dk}\right)^2\left(\frac{4H}{W'}\right)^2 + \pi^2\left(\frac{Dk+1}{2Dk}\right)}\right]\right)$$

$$W' = W + \left(\frac{Dk+1}{2Dk}\right)\left(\frac{T}{\pi}\right)\ln\left(\frac{4e}{\sqrt{\left(\frac{T}{H}\right)^2 + \left(\frac{T}{W\pi + T1.1\pi}\right)^2}}\right)$$

$$Dk_{eff} = \begin{cases} \frac{Dk+1}{2} + \frac{Dk-1}{2}\left(\left(1+\frac{12H}{W}\right)^{-0.5} + 0.04\left(1-\frac{W}{H}\right)^2\right) & \text{If } W < H \\ \frac{Dk+1}{2} + \frac{Dk-1}{2}\left(1+\frac{12H}{W}\right)^{-0.5} & \text{If } W > H \end{cases}$$

Fig 20 Standard Impedance Calculation

Z is the characteristic impedance (target impedance, e.g., 50 ohms). **εeff** is the effective dielectric constant of the PCB material. **h** is the height of the dielectric substrate (distance from the trace to the ground plane).

w is the width of the trace.

V. IMPEDANCE CONTROL

Impedance is the resistance to the flow of current represented by an electrical network, and it may be resistive or reactive, or both. Impedance control in a PCB stackup is a critical aspect of ensuring reliable signal integrity and efficient power distribution in high-frequency and high-speed digital applications. The impedance of a transmission line on a PCB refers to the resistance encountered by an AC signal as it travels through the trace and is usually applied to a transmission line in a PCB carrying high-speed signals.

Choose appropriate PCB materials, width, and spacing of the conductive traces, and reference plane layers and arrange them in the stack to achieve the desired impedance. Wider traces decrease impedance, while narrower traces increase it and the higher dielectric constants lead to higher impedance, and vice versa. There are several tools available to calculate the trace impedance for high-speed signals and a popular one is “Polar Instruments”. There were two types of impedance used in PCB one is single-ended impedance and another is differential pair which Parallel routed signals exhibiting a mutual impedance between both lines, typically 50 to 120 ohms.

➢ *Single Line Impedance*

In a single-ended transmission, a signal is referenced to a common ground. The characteristic impedance is calculated based on the signal trace width, trace-to-ground plane separation, and dielectric properties of the PCB material. Devices with 8 to 32 ohms are considered as low impedance. 50 ohms is a good value with great power and the least loss, coaxial signal is a good example for 50 ohms.

- *The Formula for Calculating the Single-Ended Impedance (Zsingle) Transmission Line Equation is.*

$$Z_{\text{single}} = \frac{87\,\Omega}{\sqrt{\varepsilon_{\text{eff}}}\cdot\log\left(\frac{5.98h}{0.8w}+1.4\right)}$$

εeff: Effective dielectric constant of the PCB material.

h: Distance between the signal trace and the reference plane (e.g., ground plane).

w: Trace width

- *50-ohm Impedance with Micro-Stripline*

Micro-Stripline is an electrical transmission line in the PCB external layer coated with a solder mask, the transmission line with only one side reference plane layer separated by a dielectric layer, or adjacent GND/power shapes.

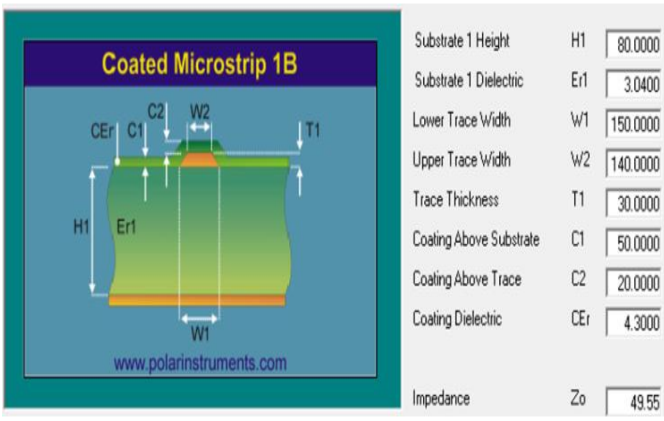


Fig 21 50-ohm Impedance with Micro-Stripline

Fig-21 shows the parameters and sample calculations for the Micro-Stripline with 50 ohms (values are in microns).

- *50-ohm Impedance with Stripline*

A Stripline is an electrical transmission line in the PCB internal layer where the conductor is placed between two identical dielectric materials with both side reference plane layers.

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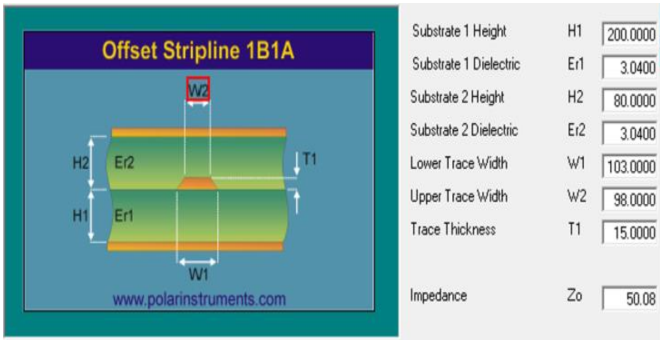

Fig 22 50-ohm Impedance with Stripline

Fig-22 shows the parameters and sample calculations for the Stripline with 50 ohms (values are in microns).

➢ *Impedance (Differential)*

The impedance calculations for a differential dual transmission line are determined by the signal parameters such as line width, line spacing from the GND/Power, copper thickness, reference plane, and dielectric thickness on the PCB. differential impedance is the instantaneous impedance of a pair of transmission lines when two complimentary signals are transmitted with opposite polarity. The characteristic impedance in a differential pair (Zdiff) is calculated based on the trace width, spacing between the traces, and the dielectric properties of the PCB material. The formula for calculating differential pair impedance is:

$$Z_{\text{diff}} = \frac{2 \times Z_{\text{single}}}{\sqrt{1-\left(\frac{s}{w}\right)^2}}$$

s: Spacing between the two traces in the differential pair.
w: Trace width

Differential pair impedance is generally higher than single-ended impedance for the same trace width and dielectric properties due to the wider effective trace created by the two traces. Differential pair impedance is crucial for high-speed digital applications, offering better noise immunity and signal integrity usually comes with 90 to 120 ohms.

- *100-ohm Impedance with Micro-Stripline*

100–120 ohms Differential with co-planner waveguide Micro-Stripline is an external layer coated with a solder mask, the transmission line with only one side reference plane layer, and adjacent GND/power shapes.

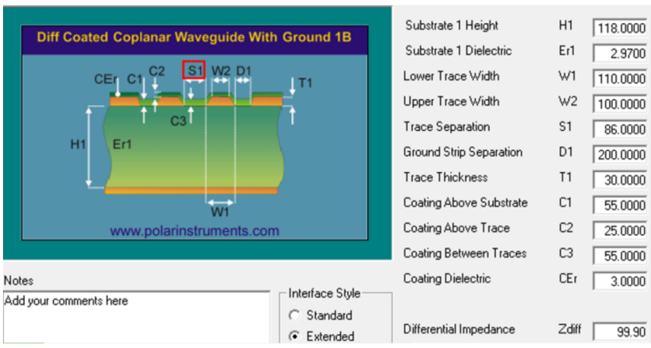

Fig 23 100-ohm Impedance with Micro-Stripline

Fig-23 shows the parameters and sample calculations for the Micro-Stripline with coplanar waveguide (values are in microns).

- *100-ohm Impedance with Stripline*

100-ohm Differential with co-planner waveguide Stripline is where two conductor lines are in parallel with adjacent ground shapes and the traces are placed between two reference plane layers.

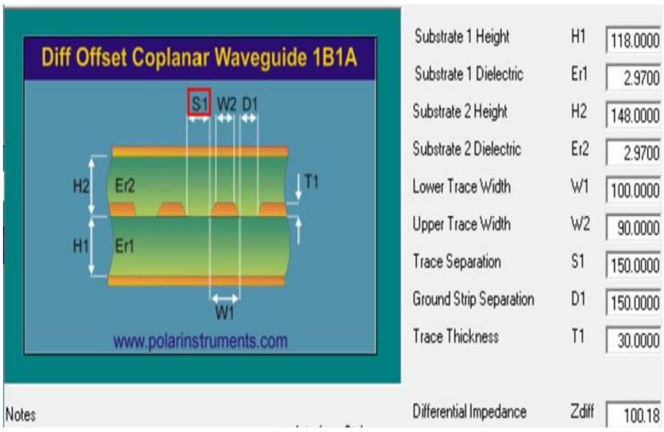

Fig 24 100-ohm Impedance with Stripline

- ✓ Fig-24 shows the parameters and sample calculations for the Stripline (values are in microns).
- ✓ Here are the expansions for the calculations.
- ✓ **H1/H2**: Substrate height **-** As substrate thickness increases, impedance increases.
- ✓ **Er1/Er2**: Dielectric constant with respect to reference layer **-** DK value increases while impedance decreases.
- ✓ **W1-W2**: Lower/upper Trace width – Under trace width increases and impedance increases.
- ✓ **S1**: Trace Spacing – Trace to trace Spacing distance, increases the impedance increases.
- ✓ **D1**: Ground Spacing – Ground Spacing from the traces on the same layer with Stitching vias to the Reference Plane used for microwave/RF application.
- ✓ **T1**: Trace thickness (Copper Weight) – Trace thickness increases, and impedance decreases.
- ✓ **CEr**: Coating Dielectric constant with respect to the coating dielectric material (Soldermask) parameter.
- ✓ **C1/C2**: Solder mask thickness – Coating thickness increases, and impedance decreases.
- ✓ **Zo:** calculated Impedance

➢ *Copper Weight*

Copper weight (Copper Thickness) is known as the thickness of the conductive layer on a PCB. Fig 25 shows the Copper weight chart which is commonly used in PCB manufacturing.

Cooper Weight (Oz)	Thickness (Microns)	Thickness (Mil)
0.5	17.5	0.7
1	35	1.4
2	70	2.8
3	105	4.2

Fig 25 Standard Copper Weight chart

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➤ *Reference Plane*

A reference plane in a PCB refers to a conductive layer (usually ground or power planes) that serves as a stable and consistent electrical reference for signals on the board. It provides a defined electrical potential against which signal voltages and currents are measured. Properly utilizing reference planes is critical for maintaining impedance control, and signal integrity and reducing electromagnetic interference (EMI) in high-speed digital and high-frequency analog circuits.

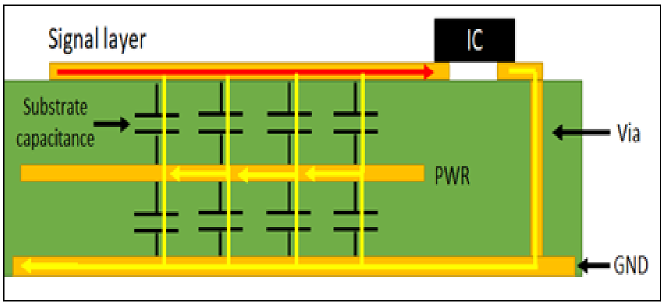

Fig 26 Reference Plane on a Stackup

Fig-26 shows the reference plane configuration, defining reference planes with impedance-controlled structure. Managing return paths is a critical part of Stackup with proper dielectric material and the thickness of the material might force return currents to pass into a PCB power plane before being coupled back to a ground layer. In a Signal traveling on a transmission line, the return path is determined by the capacitance between the line and its reference plane. A higher capacitance, higher frequency, or both means that the return current can easily pass into the ground layer as a displacement current.

➤ *Split Plane (Signal/Power/Ground)*

A split plane in a PCB is used for different power signals in one layer, and in some cases, it may be Mixed Signals like analog and digital circuits in a single layer. If you split the Power, Ground, and Signal in a layer you may end up with signal Integrity issues when routing the signal to the adjacent layer over the split area due to losing the return path. Avoid parallel trace running on split areas and also avoid traces over voids to prevent return plane discontinuity. The Best example is when designing a four-layer stack up, making the external layers as Ground and using the Internal layers for power and the signal which will provide the best return path to the circuits.

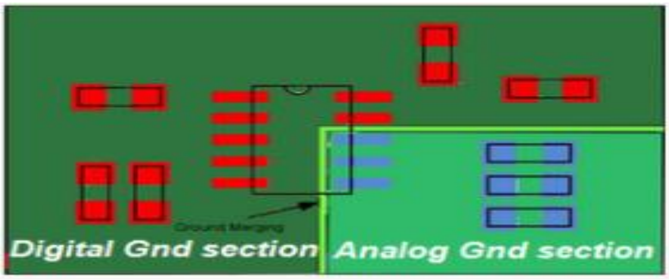

Fig 27 Split Plane

Fig-27 is a simple analog and digital ground split plane in one layer. It is important to align the split plane with the layer Stackup design to maintain consistency and ensure proper layer-to-layer registration on the conductive and dielectric Layers.

➤ *Dielectric Thickness*

The thickness of the lamination material between the conductive layers of the PCB reflects the dielectric thickness. The characteristic impedance of the transmission lines' performance and thermal and mechanical stability is determined by the dielectric layer thickness and the material properties. Choosing the right material based on the operating frequency, mechanical and electrical properties, thermal property (CTE), Dielectric Constant (Dk), and dissipation factor (Df) known as Loss tangent is a key factor. Fig-28 is a typical 6-layer impedance-controlled symmetrical Stackup with the combination of Prepreg and Core lamination material and each layer's dielectric thickness.

Layers	Cu Thick. (mils)	Cu Foil wt (oz)	Stackup Figure	DK	DF	Lam. Thick. (mils)	Material
1	1.90	0.5 oz					
				2.98	0.0014	**5.00**	Core Tachyon 100G 5.00mils
2	0.60	0.5 oz					
				3.04	0.0016	**6.35**	Prepreg Tachyon 100G 1078
3	0.60	0.5 oz					
				3.11	0.0018	**10.00**	Core Tachyon 100G 10.00mils
				2.97	0.0014	**4.10**	Prepreg Tachyon 100G 1078
				3.11	0.0018	**10.00**	Core Tachyon 100G 10.00mils
4	0.60	0.5 oz					
				3.04	0.0016	**6.35**	Prepreg Tachyon 100G 1078
5	0.60	0.5 oz					
				2.98	0.0014	**5.00**	Core Tachyon 100G 5.00mils
6	1.90	0.5 oz					

Fig 28 Symmetrical layer Stackup

➤ *Material Construction (Single vs. multi-ply)*

The material construction on a PCB Stackup using Glass Fabric bonded with resin epoxy material. There are several Glass styles widely used based on the Glass spread like 106, 1080, 1078, 2116, 3313, etc. and there are several options like low DK glass style with less or more gap. The core material with 2-ply construction vs. 1-ply will give you a different Dk and Df based on the retained resin % of the core isolation and separation between conductive Layers. Fig-29 shows the 1-ply vs. 2-ply construction with Stripline

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on a core material. 1-ply is good for the low-cost general minimal complex PCB. Multi-ply provides better isolation which costs more and is good for complex PCBs with high-frequency, high-speed applications with better EMC, crosstalk, and Signal integrity.

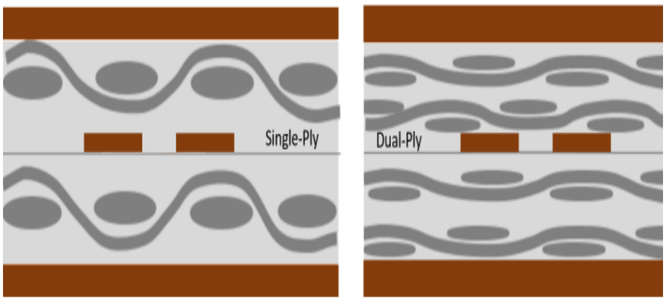

Fig 29 1-Ply vs. 2-Ply Spread Glass

The number of plies whether prepreg or core comes with the same glass weave style and porosity which will have different dielectric constants, and also the different laminate thicknesses will require different glass weave styles. It is important to choose the right glass spread based on the transmission line speed and power requirement while defining a Stackup.

➢ *EMI/EMC Consideration*

Electromagnetic Interference (EMI) and Electromagnetic Compatibility (EMC) considerations are crucial in PCB stackup design to minimize unwanted electromagnetic emissions. The multilayer Stackup with proper Ground plane is an option to reduce the EMI/EMC, especially for high-frequency, high-speed digital and high-power applications. Impedance control Stackup with trace width and spacing, coplanar Ground with stitching vias between critical signals can reduce EMI emissions. The blind and buried, back-drill technologies with sequential lamination can reduce stub length and reduce unwanted radiations. Propper stacking with the arrangement of signal layers can EMI and improve EMC. Plane layers with adjacent Ground, Guard/ shunt traces, and power plane distribution with shielding ensure a low-impedance return path and minimize noise.

#	Name	Layer	Layer Function	Value mil	Material	Dielectric Constant
*	*	*	*	*	*	*
		Surface				1
		Dielectric	Dielectric	0.71	Fr-4	3.9
1	TOP	Conductor	Conductor	1.18	Copper	3.9
		Dielectric	Dielectric	3.7	EM_528BK	3.19
2	L2-GND1	Plane	Plane	0.98	Copper	3.41
		Dielectric	Dielectric	3.7	EM_528BK	3.19
3	L3_SIG1	Conductor	Conductor	0.98	Copper	4.1
		Dielectric	Dielectric	3.7	EM_528BK	3.19
4	L4_GND-PWR1	Conductor	Conductor	1.18	Copper	4.1
		Dielectric	Dielectric	1.5	EM_526B	3.17
5	L5_PWR1	Plane	Plane	0.98	Copper	4.5
		Dielectric	Dielectric	2.36	EM_526	3.29
6	L6_PWR2	Plane	Plane	0.98	Copper	4.5
		Dielectric	Dielectric	1.5	EM_526B	3.17
7	L7_GND-PWR2	Conductor	Conductor	1.18	Copper	4.1
		Dielectric	Dielectric	3.7	EM_528BK	3.19
8	L8_SIG2	Conductor	Conductor	0.98	Copper	4.1
		Dielectric	Dielectric	3.7	EM_528BK	3.19
9	L9_GND2	Plane	Plane	0.98	Copper	3.41
		Dielectric	Dielectric	3.7	EM_528BK	3.19
10	BOTTOM	Conductor	Conductor	1.18	Copper	3.9
		Dielectric	Dielectric	0.71	Fr-4	3.9
		Surface				1

Fig 30 Symmetrical Layer Stackup

Fig-30 is a symmetrical 10-layer Stackup with a tight coupling plane (Top/GND/Signal/Power/GND/Power) that helps to reduce voltage drops, minimize noise, and enhance EMC performance.

ISSN No:-2456-2165

VI. CONCLUSION

The miniaturization of electronic devices has led to the need for a more compact and more efficient PCB stackup design. In the modern era with Artificial intelligence (AI) Augmented reality (AR), and 5G Speed network solutions, all PCB engineers should be up to date with the current technologies and advanced Stackup design for future product designs.

Stackup design is a critical aspect of designing a printed circuit board (PCB) that directly impacts its performance, reliability, and manufacturability. Determine the number of layers, Layer thickness, and impedance requirements based on the complexity of the circuit and functionality. Using materials with a low CTE, thermal conductivity, and controlled dielectric constant, for effective thermal management, helps run devices in extreme temperatures. Using the multi-layered construction with multiple laminations with blind and buried vias, PCB manufacturers can create high-quality, reliable boards that can perform in various environments. Choose appropriate dielectric materials based on the desired electrical properties, such as permittivity, dissipation factor, and thermal conductivity, and follow a logical order and symmetrical layer arrangement to optimize signal integrity and thermal management.

Cost and reliability play a pivot role in stackup design, poor stackup design impacts time to market and cost. The board design is time-consuming work and once start the manufacturing it may take 2-8 weeks to build a multi-layer PCB based on the lamination cycle and material procurement time on the fabrication. There is a quick turn and standard turn for PCB manufacturing quick turn costs more. Small mistakes will take 2-8 weeks to redo the same PCB and it may impact entire product deliveries as time to market. In the competitive world, everyone wants to showcase their product on time in any industries like network, Consumer, Aerospace, Medical, Automobile, etc. Doing a Pre-evaluation and pre-simulation to design the stack up with proper lamination material, via type and number of layers with the number of lamination cycles will save a lot of cost and time. Use simulation tools to validate the stackup design and analyze signal integrity, impedance matching, and thermal behavior before PCB fabrication. Clearly document the Stackup details, including layer order, materials used, and design guidelines, to aid PCB fabrication and assembly.

Choosing the right Stackup for designing the PCB is a crucial aspect of product complexity, size, reliability, and cost. Using modern technologies like Flex PCB, Rigid-Flex, and Embedded Passive PCB, metal core PCB Stackup with required laminations provides a compact and reliable product to the electronics Industry. PCB Designers must work with the PCB manufacturers to finalize the Stackup and consider the performance, reliability, and manufacturability of the printed circuit board.

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