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Verifying Deeds Simulator as a Savvy Tool for Half Adder and Full Adder Circuit Simulation

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Abstract:- Accurate simulation of digital logic circuits is essential for ensuring their functionality before actual hardware implementation. The performance of the Digital Electronic Educational Design System (DEEDS) simulator was evaluated by applying it to half adder and full adder logic circuits. The goal is to assess the precision and dependability of DEEDS by comparing its simulation outcomes with theoretical expectations for these fundamental arithmetic components. This study employs DEEDS to model and simulate these adder circuits, with a focus on comparing the simulation results to theoretical predictions. The verification process involves a thorough examination of the sum and carry outputs for both half adder and full adder circuits across various input scenarios. The analysis identifies any discrepancies between the simulated and theoretical results and explores potential sources of these discrepancies. The results demonstrate that DEEDS offers a reliable and accurate simulation platform for these essential digital circuits, with simulated results closely matching theoretical expectations. This verification highlights DEEDS' effectiveness as a tool for digital circuit design and analysis.

Keywords:- *Digital Electronics Education And Design Suiter Simulator (DEEDS), Half Adder, Full Adder, Karnaugh Maps.*

I. INTRODUCTION

Arithmetic operations form the cornerstone of digital computing systems, with the half adder and full adder circuits being fundamental to this process [1]. The half adder handles the addition of two single-bit binary numbers, producing both a sum and a carry output. The full adder enhances this functionality by integrating a carry-in input, thereby facilitating the addition of multi-bit binary numbers through the accumulation of carry from previous stages [2].

Accurate simulation of these adder circuits is essential for ensuring their proper functionality and performance before physical deployment [3]. The Digital Electronic Educational Design System (DEEDS) provides a sophisticated simulation environment for designing and analyzing digital circuits. DEEDS offers a robust platform for modeling these circuits, enabling thorough analysis and verification of their behavior. The application of DEEDS for simulating both half adder and full adder circuits is explored in order to showcase DEEDS' capabilities in modeling these fundamental components, evaluate how closely the simulation results align with theoretical expectations, and identify any discrepancies or opportunities for refinement [4].

II. LITERATURE REVIEW

Logic gates are crucial in digital electronics, executing core functions that support various computational tasks. A fundamental operation facilitated by these gates is binary addition, achieved through adder circuits. Among the numerous types of adders, the half adder and full adder are particularly notable for their roles in summing binary numbers, which is essential in a broad range of digital systems [5].

Logic gates, including AND, OR, and XOR, are the building blocks of digital circuits, performing essential Boolean functions. Adders utilize these gates to execute binary addition. For instance, the half adder is designed to add two single-bit binary inputs. It uses an XOR gate to compute the sum and an AND gate to generate the carry-out. This simple design is fundamental to digital arithmetic. The full adder, however, extends the half adder's capabilities by adding a carry-in input. This addition enables the full adder to process the sum of three bits (two main bits and a carry bit) using two half adders and an OR gate to produce the final sum and carry-out [5].

The Deeds Simulator is a sophisticated tool that supports the modeling and simulation of digital logic circuits. It offers an interactive platform for designing, testing, and verifying various digital components, including adders. The simulator's user-friendly interface and comprehensive features make it a valuable resource for both educational and research applications in digital electronics. It enables users to build and visualize complex circuits, providing a deeper understanding of their operations [6].

In evaluating the Deeds Simulator for analyzing half adder and full adder circuits, several key points emerge. For the half adder, the simulator accurately models the circuit using its built-in logic gates. Users can construct the half adder by linking an XOR gate and an AND gate, allowing clear visualization of the circuit's functionality [7]. Simulation results closely match theoretical predictions, verifying the simulator's accuracy in representing basic digital circuits. This precision is crucial for validating circuit performance and ensuring alignment with theoretical expectations. Furthermore, the simulator's visual and

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interactive features enhance the educational experience, enabling students to experiment with different configurations and observe real-time changes in outputs [8].

Similarly, the Deeds Simulator excels in modeling the full adder circuit. By combining two half adders and an OR gate, the simulator effectively demonstrates the full adder's capability to handle carry-in inputs and perform multi-bit addition. The simulation results consistently align with theoretical truth tables across various input scenarios, confirming the full adder's functionality. The simulator's detailed analysis tools provide a comprehensive understanding of the full adder's operation and its interaction with carry-in inputs, offering valuable insights into the complexities of multi-bit addition [9].

Deeds Simulator proves to be an invaluable tool for modeling and analyzing essential digital circuits like the half adder and full adder. Its accurate simulation capabilities and educational benefits make it an effective resource for both teaching and research in digital electronics. The simulator's ability to faithfully represent and verify adder circuits underscores its importance in understanding and designing critical digital components. As digital technology continues to evolve, tools like the Deeds Simulator will remain essential for exploring and validating increasingly complex electronic designs [6].

III. METHODOLOGY

Adders are key components in digital electronics, primarily used for performing arithmetic operations like addition. They execute binary addition, which is crucial for a wide range of computing functions, from basic calculations to complex algorithms. Adders come in different forms, categorized by their complexity and the number of bits they process. Adder circuits, ranges from basic half adders to sophisticated carry look-ahead adders as their design and efficiency make them essential components in digital electronics and computing.

Two types of Adder Circuits will be analyzed using the Deeds Simulator. These are half adder and full adder circuits.

A. *Half Adder*

A half adder is a basic adder circuit designed to sum two single-bit binary numbers. A half adder is a basic combinational logic component with two 1-bit inputs, xi and yi, and two outputs, which are related as follows:

- Components: It includes an XOR gate and an AND gate.

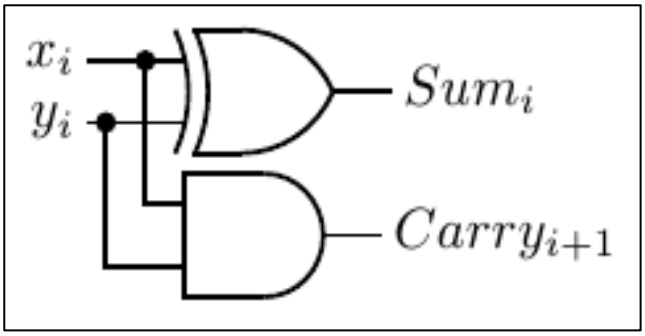

Fig 1: A Half Adder Circuit

➢ *Functionality*

- Sum: The XOR gate calculates the sum of the input bits.
- Carry-out: The AND gate determines the carry bit, necessary when both input bits are 1.

Table 1: Truth Table for the Half Adder

xi	yi	Carryi+1	Sumi
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

- Inputs: xi is the ith bit of one binary number while yi is the ith bit of another binary number
- Outputs: Sumi is the XOR of xi and yi while Carryi+1 is the AND of xi and yi

➢ *To Find the Equations for the Sum and Carry-Out of a Half Adder, we can use Karnaugh Maps or Algebraic Manipulations:*

- Sum Equation:
  $S_i(x_i, y_i) = (x_i \oplus y_i)$
- Carry-out Equation:
  $C_{i+1} = x_i$

B. *Full Adder*

A full adder expands on the half adder by incorporating an extra input for carry-in, allowing it to handle three bits (two main bits and a carry bit).

A full adder extends the concept of the half adder by including a third input, Ci, which enables it to add three bits (two significant bits plus a carry bit). This was achieved using two half adders and an OR gate to construct a full adder.

- Components: It consists of two XOR gates, two AND gates, and one OR gate.

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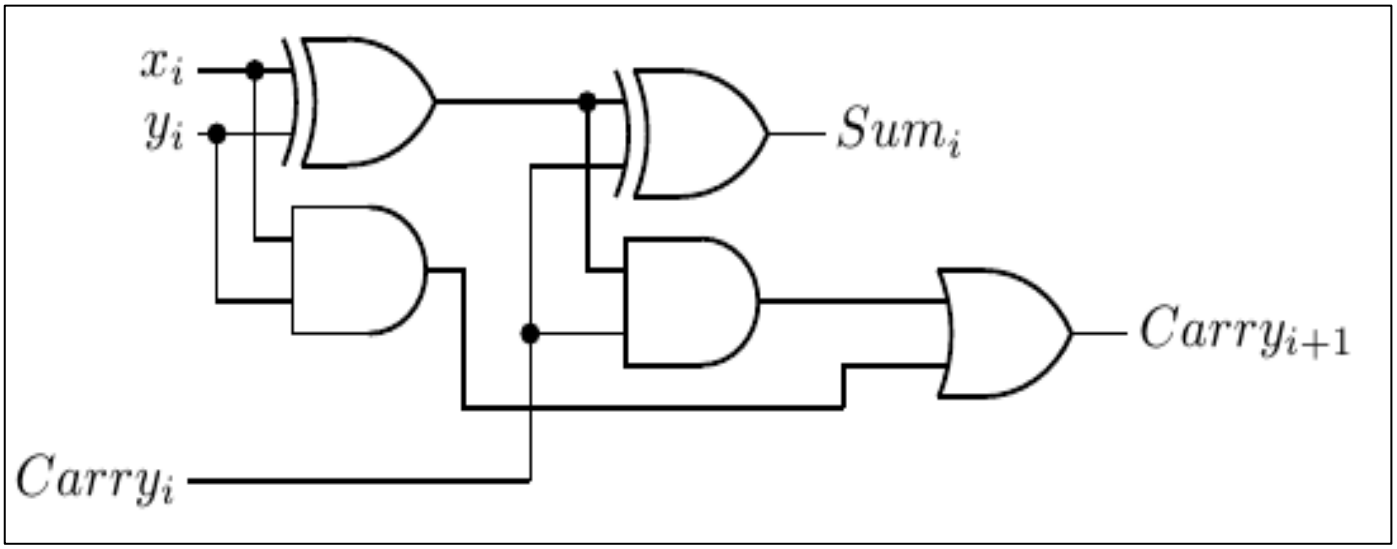

Fig 2: A Full Adder Circuit

➢ *Functionality*

- Sum: Computed by the XOR gates.
- Carry-out: Determined by the OR gate, which combines the carry outputs of the AND gates.

Table 2: Truth Table for Full Adder

Carryi	xi	yi	Carryi+1	Sumi
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Here, xi represents the ith bit of the multi-bit value x, yi denotes the ith bit of the multi-bit value y, Sumi is the ith bit of the multi-bit value Sum, and Carryi+1 is the carry resulting from the addition of the next-lower significant bits xi, yi, and Carryi

To find the equations for the sum and carry-out of a full adder, we can use Karnaugh maps or algebraic manipulations:

- Sum Equation:

✓ $S_i(C_x, x_i, y_i) = \overline{C_i} \cdot \overline{x_i} \cdot y_i + \overline{C_i} \cdot x_i \overline{y_i} \cdot + C_i \cdot x_i \cdot y_i + C_i \cdot \overline{x_i} \cdot \overline{y_i}$
✓ or
✓ $S_i(C_x, x_i, y_i) = C_i \oplus (x_i \oplus y_i)$

- Carry-out Equation:

✓ $C_{i+1} = x_i \cdot y_i + C_i \cdot (x_i \oplus y_i)$

IV. RESULTS AND DISCUSSION

A. Half Adder

Following a series of simulations conducted using the DEEDS application for the half adder, the circuit output aligned with the expected test event. The input comprised two binary numbers, labeled xi and yi, which ranged from 00 to 11, corresponding to decimal values from 0 to 7. This output, displayed in binary format in Carryi+1 and Sumi+1. Detailed results of the experiment are illustrated in the figures below.

➢ *Event 1*

- Input xi and yi= 00
- Output Carryi+1 and Sumi+1 = 00

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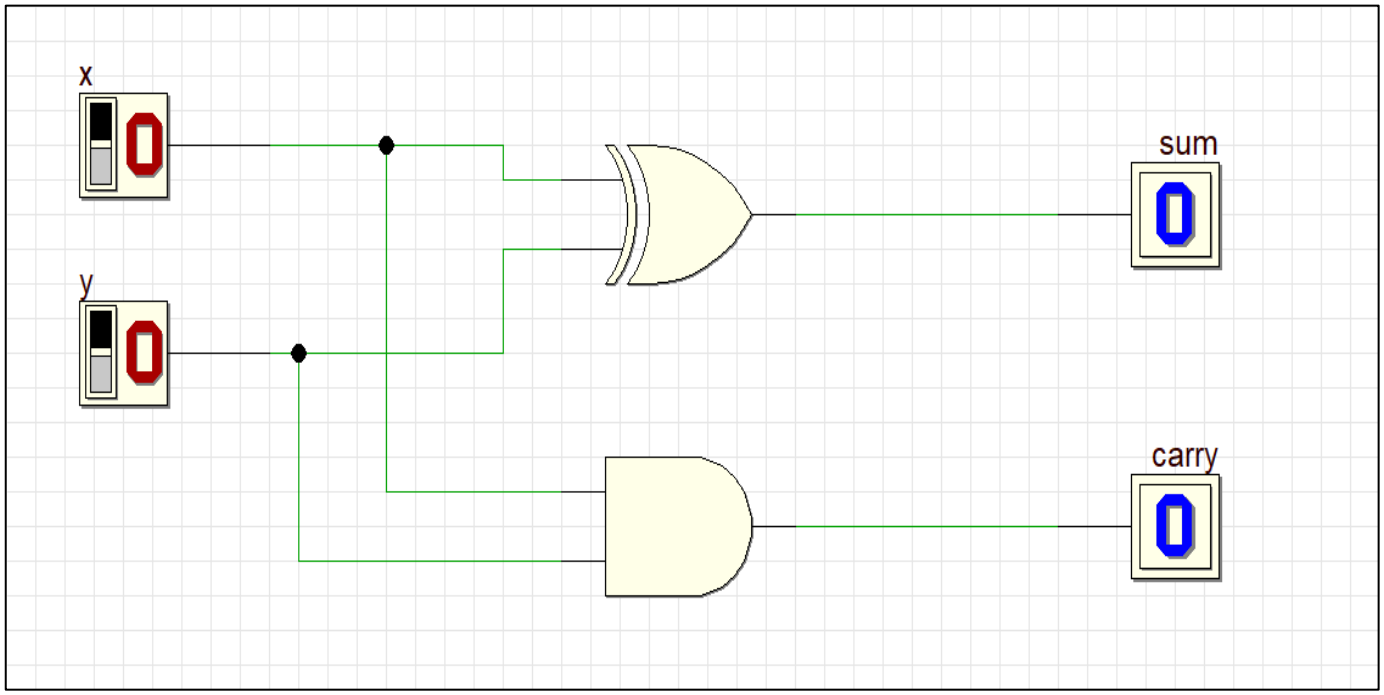

Fig 3: Half Adder Event Testing 1

➢ *Event 2*

- Input xi and yi= 01
- Output Carryi+1 and Sumi+1 = 01

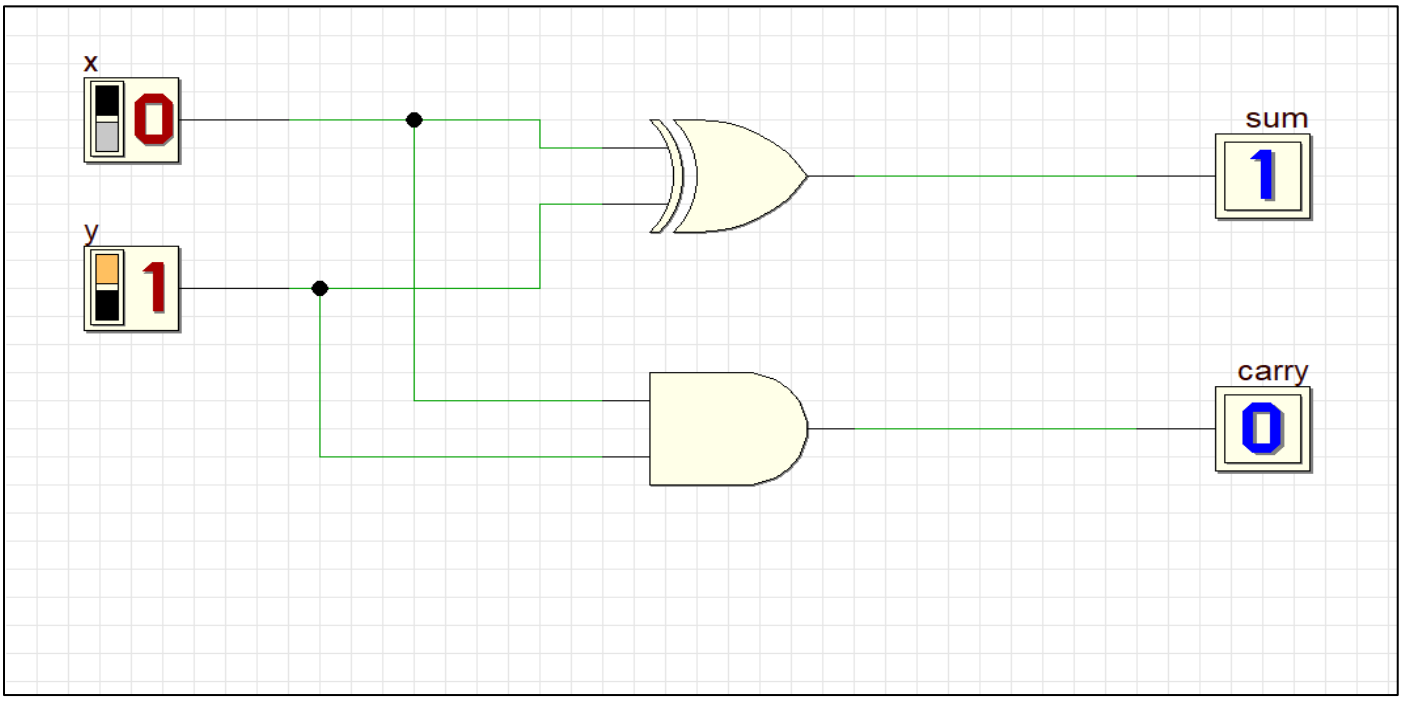

Fig 4: Half Adder Event Testing 2

➢ *Event 3*

- Input xi and yi= 10
- Output Carryi+1 and Sumi+1 = 01

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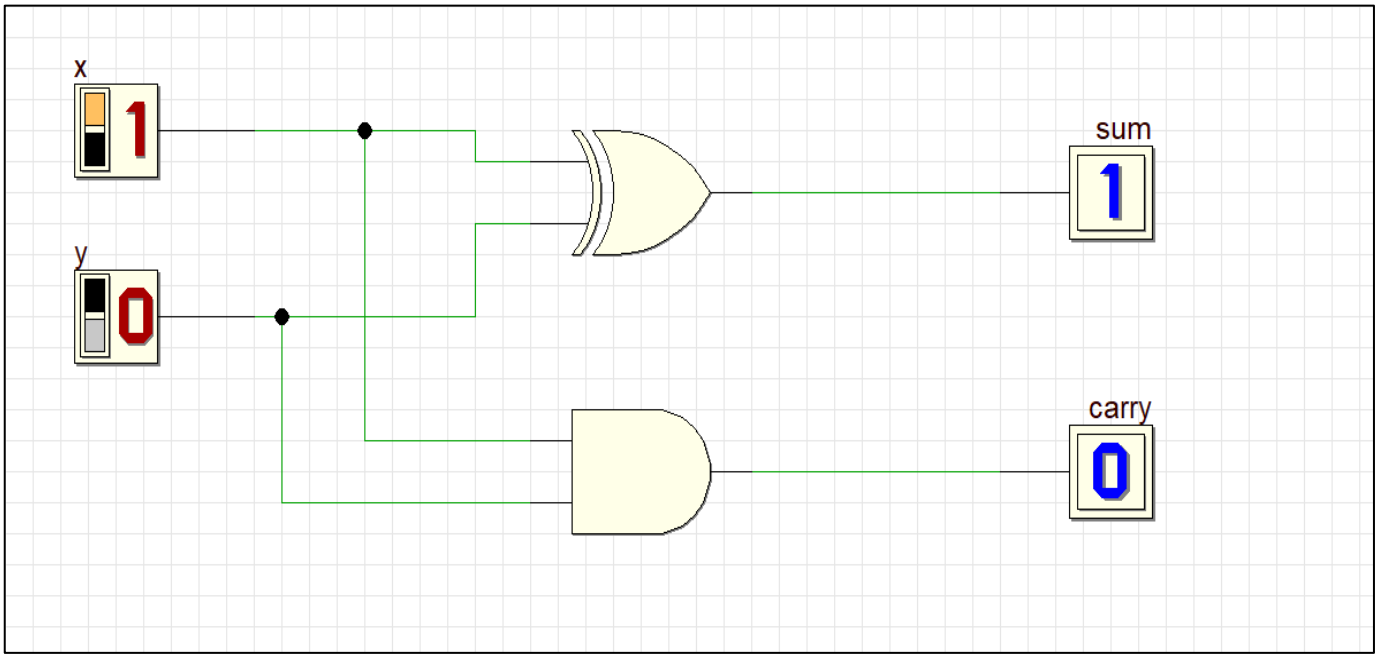

Fig 5: Half Adder Event Testing 3

➢ *Event 4*

- Input xi and yi= 11
- Output Carryi+1 and Sumi+1 = 10

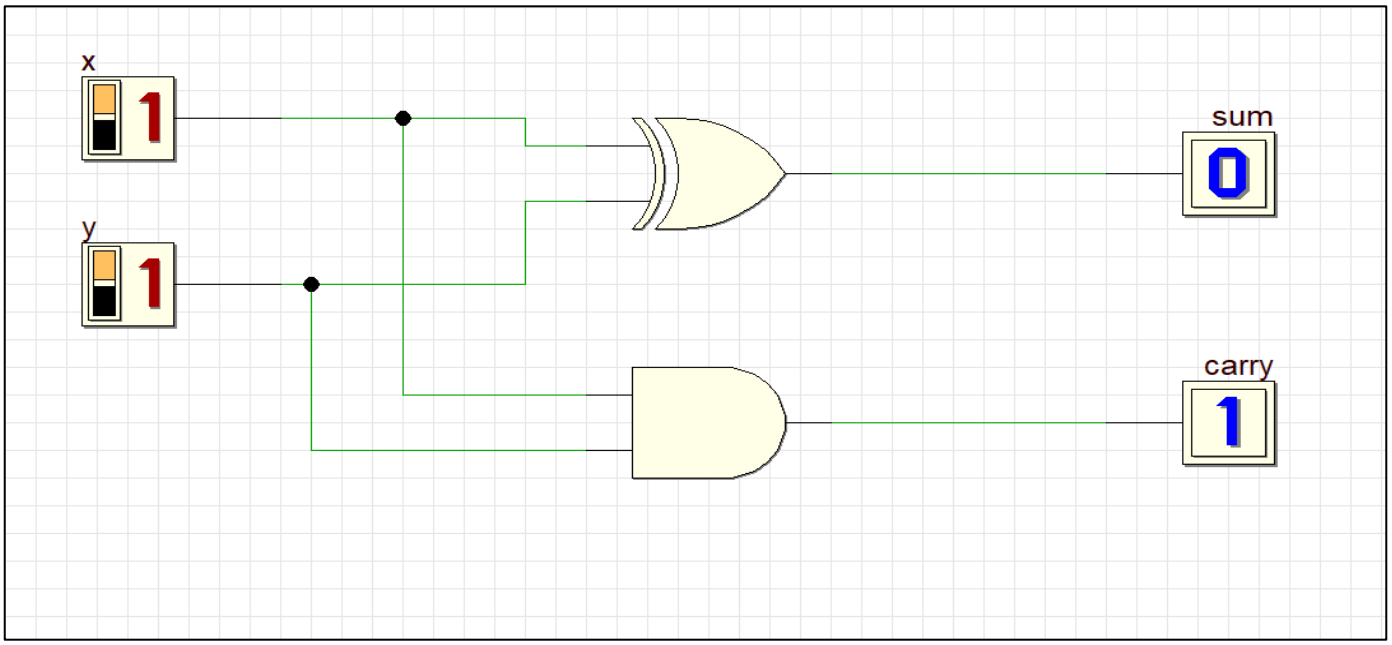

Fig 6: Half Adder Event Testing 4

B. Full Adder

Following a series of simulations conducted using the DEEDS application for the Full adder, the circuit output aligned with the expected test event. The input comprised three binary numbers, labeled Carryi, xi and yi, which ranged from 000 to 111, corresponding to decimal values from 0 to 15. This output, displayed in binary format in Carryi+1 and Sumi+1. Detailed results of the experiment are illustrated in Figure 5-16.

➢ *Event 1*

- Input Carryi, xi and yi = 000
- Output Carryi+1 and Sumi+1 = 00

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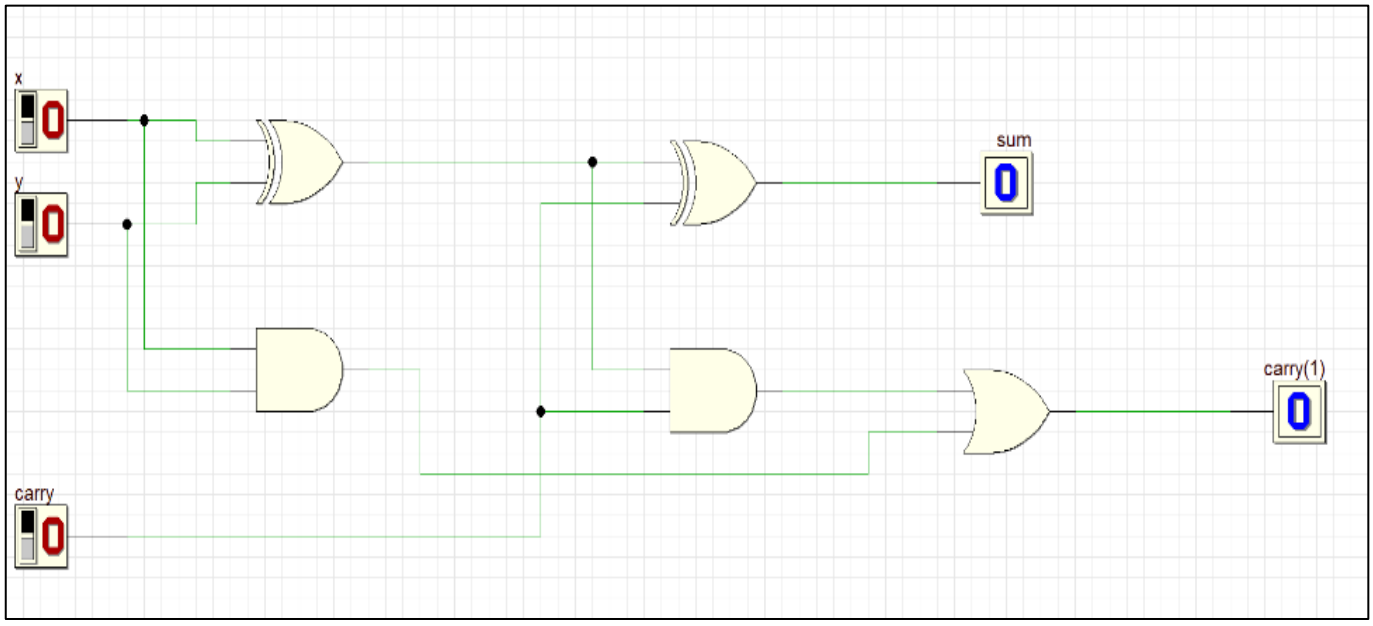

Fig 7: Full Adder Event Testing 1

➢ *Event 2*

- Input Carryi, xi and yi = 001
- Output Carryi+1 and Sumi+1 = 01

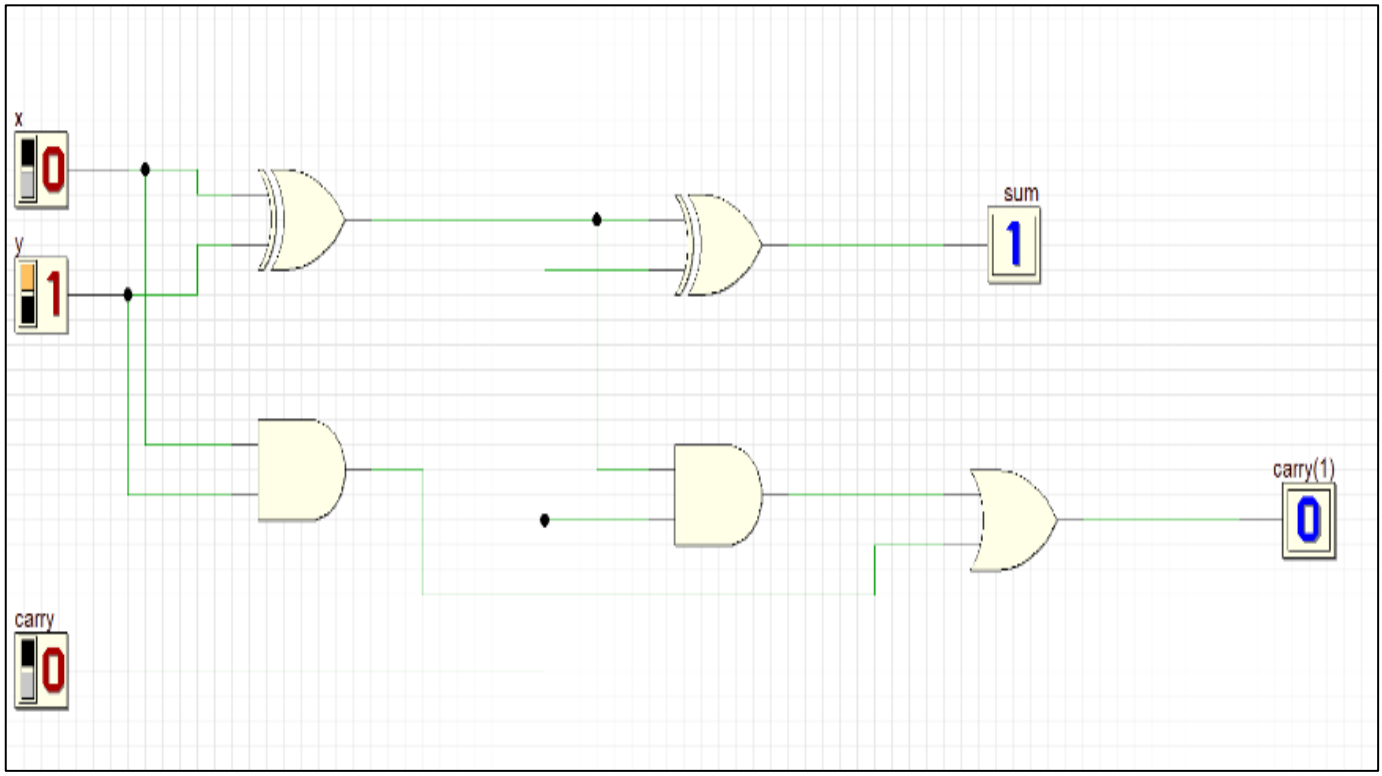

Fig 8: Full Adder Event Testing 2

➢ *Event 3*

- Input Carryi, xi and yi = 010
- Output Carryi+1 and Sumi+1 = 01

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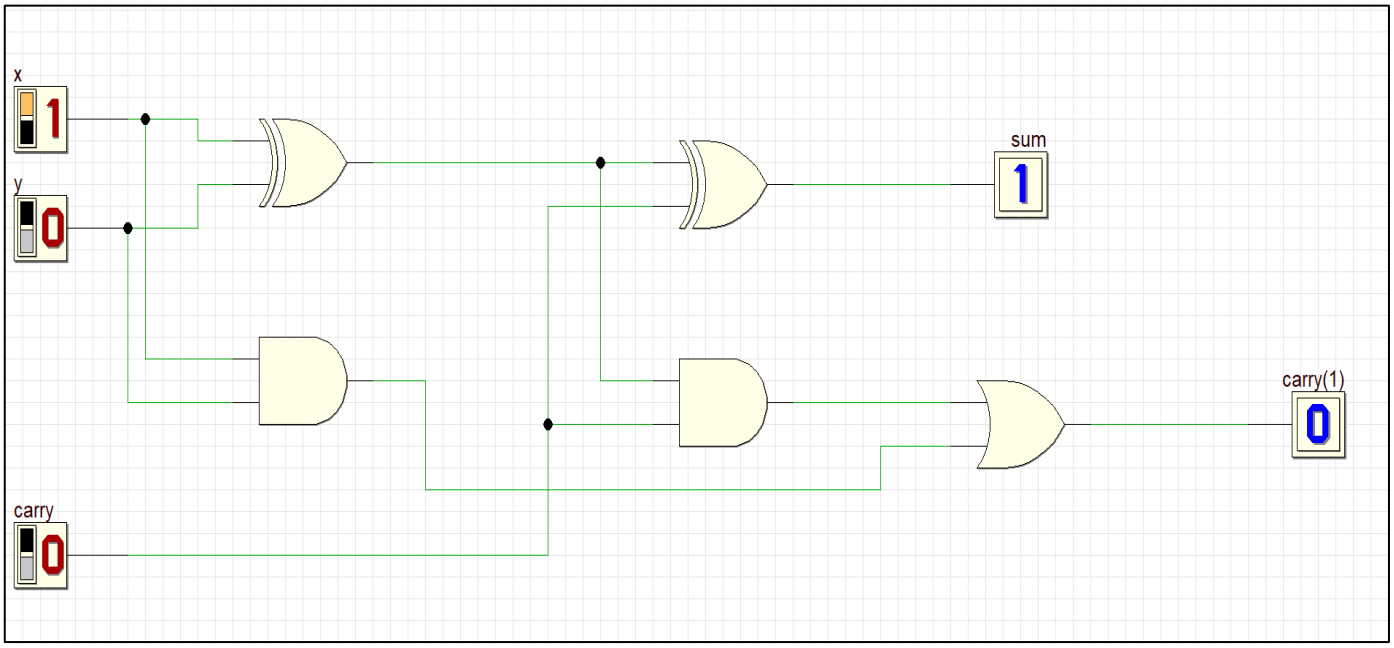

Fig 9: Full Adder Event Testing 3

➢ *Event 4*

- Input Carryi, xi and yi = 011
- Output Carryi+1 and Sumi+1 = 10

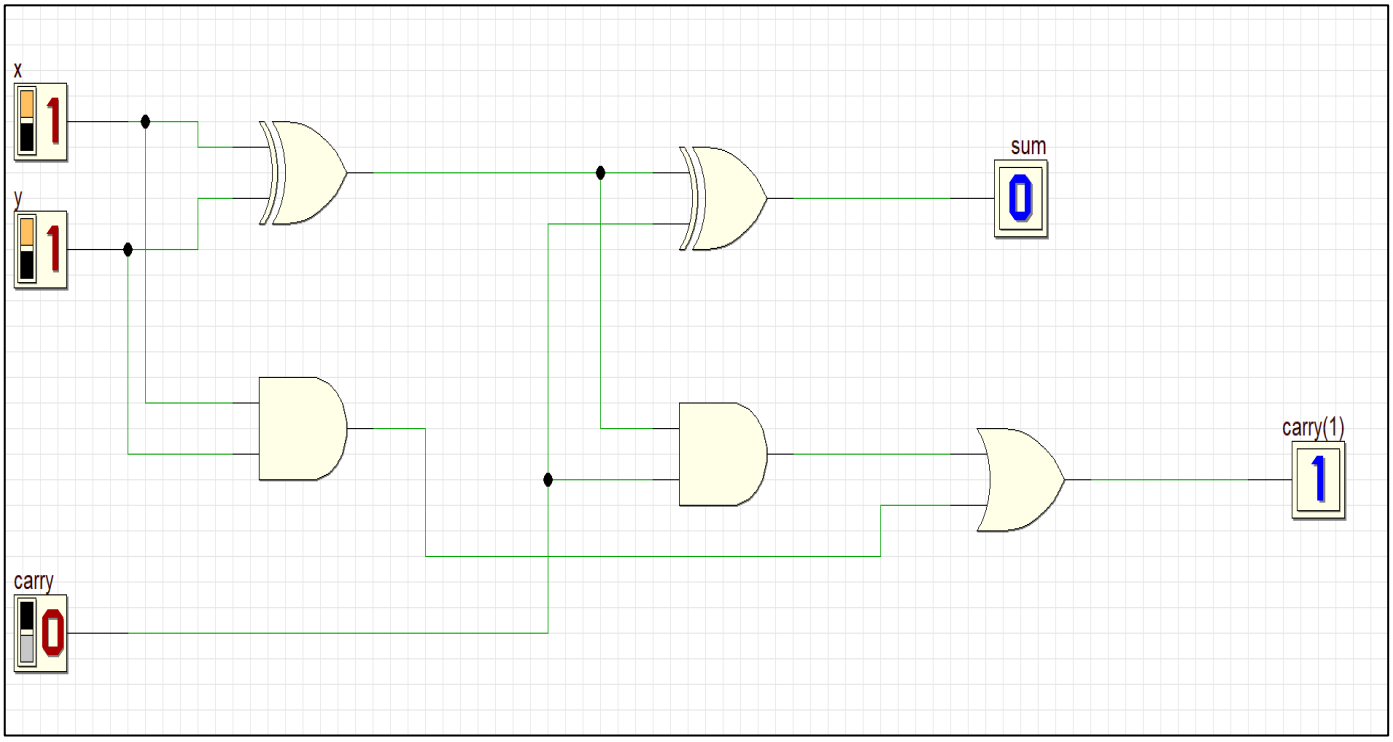

Fig 10: Full Adder Event Testing 4

➢ *Event 5*

- Input Carryi, xi and yi = 100
- Output Carryi+1 and Sumi+1 = 01

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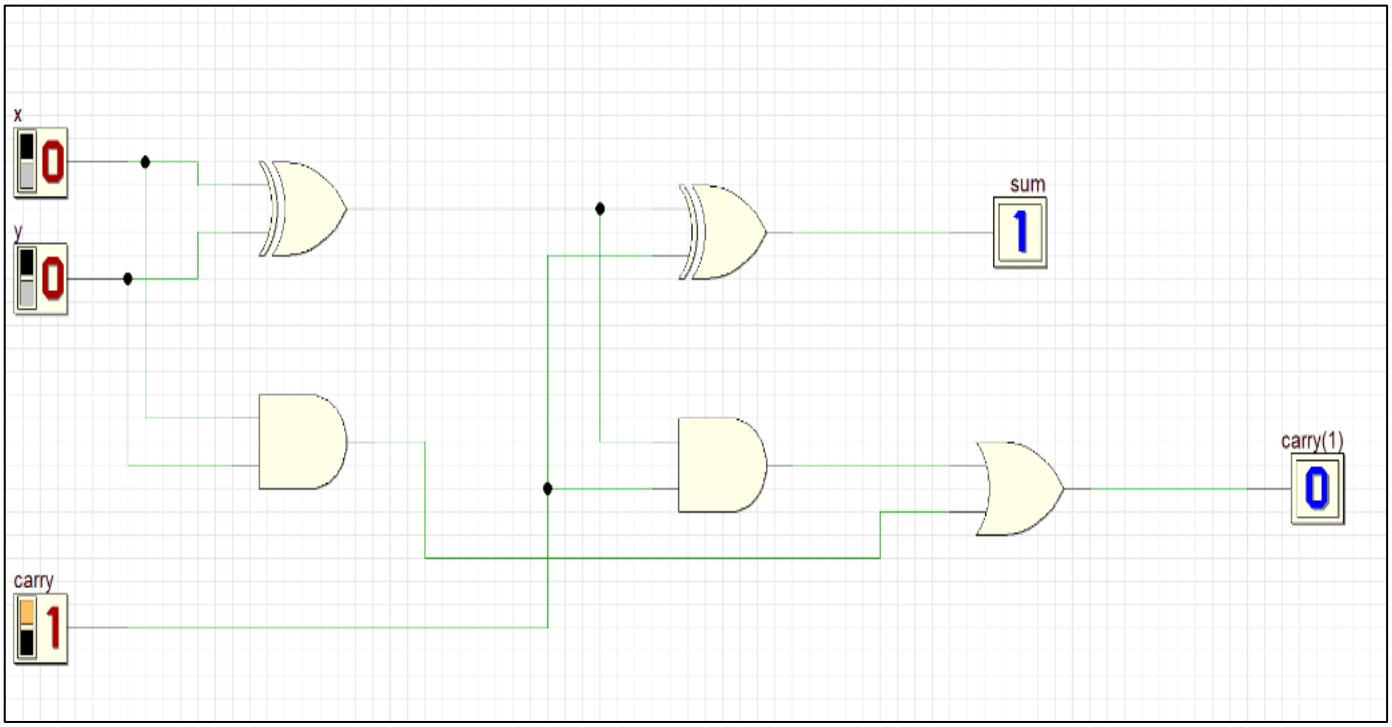

Fig 11: Full Adder Event Testing 5

➢ *Event 6*

- Input Carryi, xi and yi = 101
- Output Carryi+1 and Sumi+1 = 10

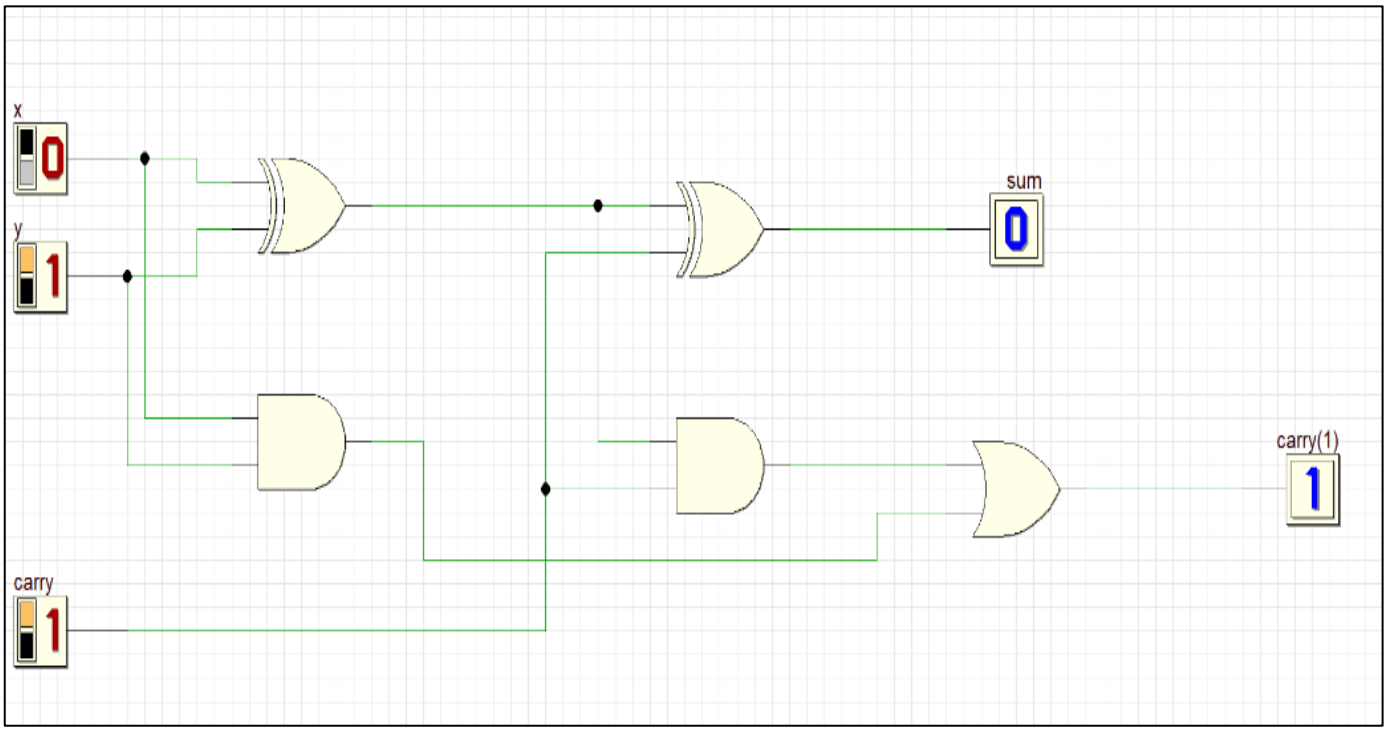

Fig 12: Full Adder Event Testing 6

➢ *Event 7*

- Input Carryi, xi and yi = 110
- Output Carryi+1 and Sumi+1 = 10

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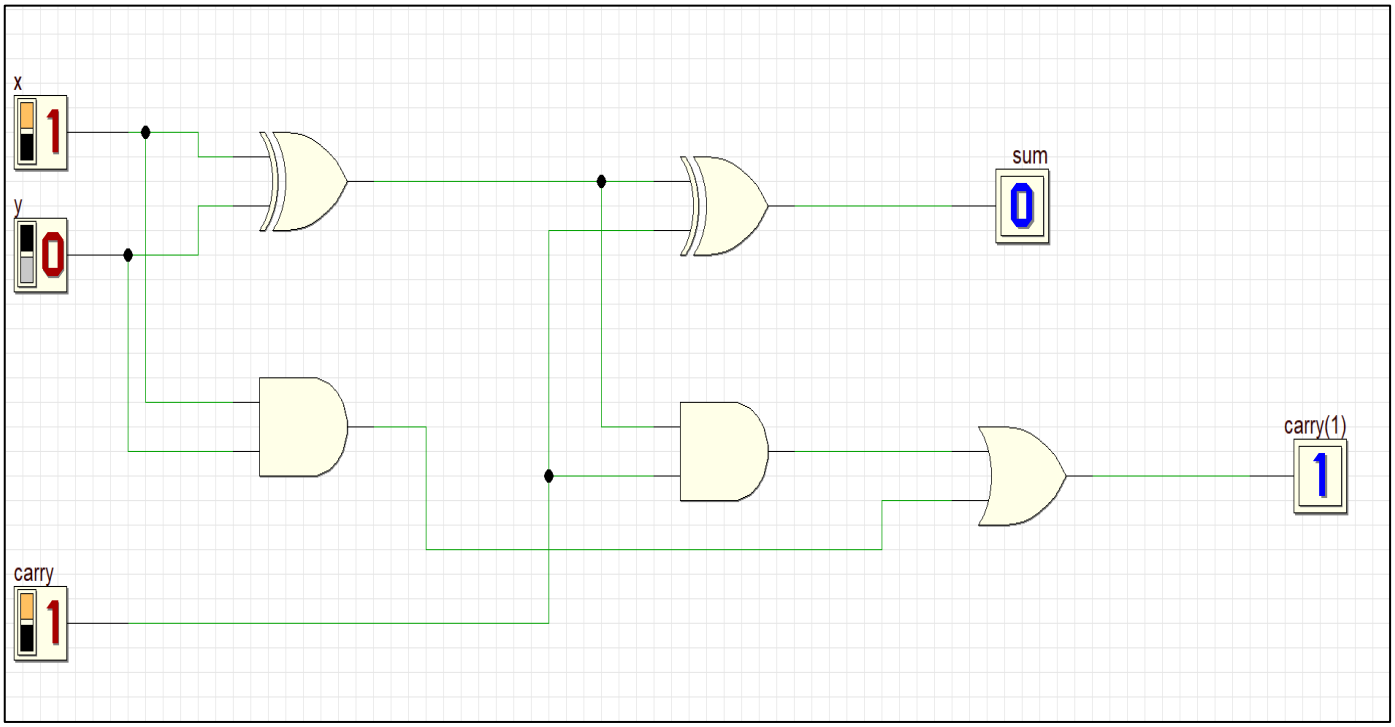

Fig 13: Full Adder Event Testing 7

➢ *Event 8*

- Input Carryi, xi and yi = 111
- Output Carryi+1 and Sumi+1 = 11

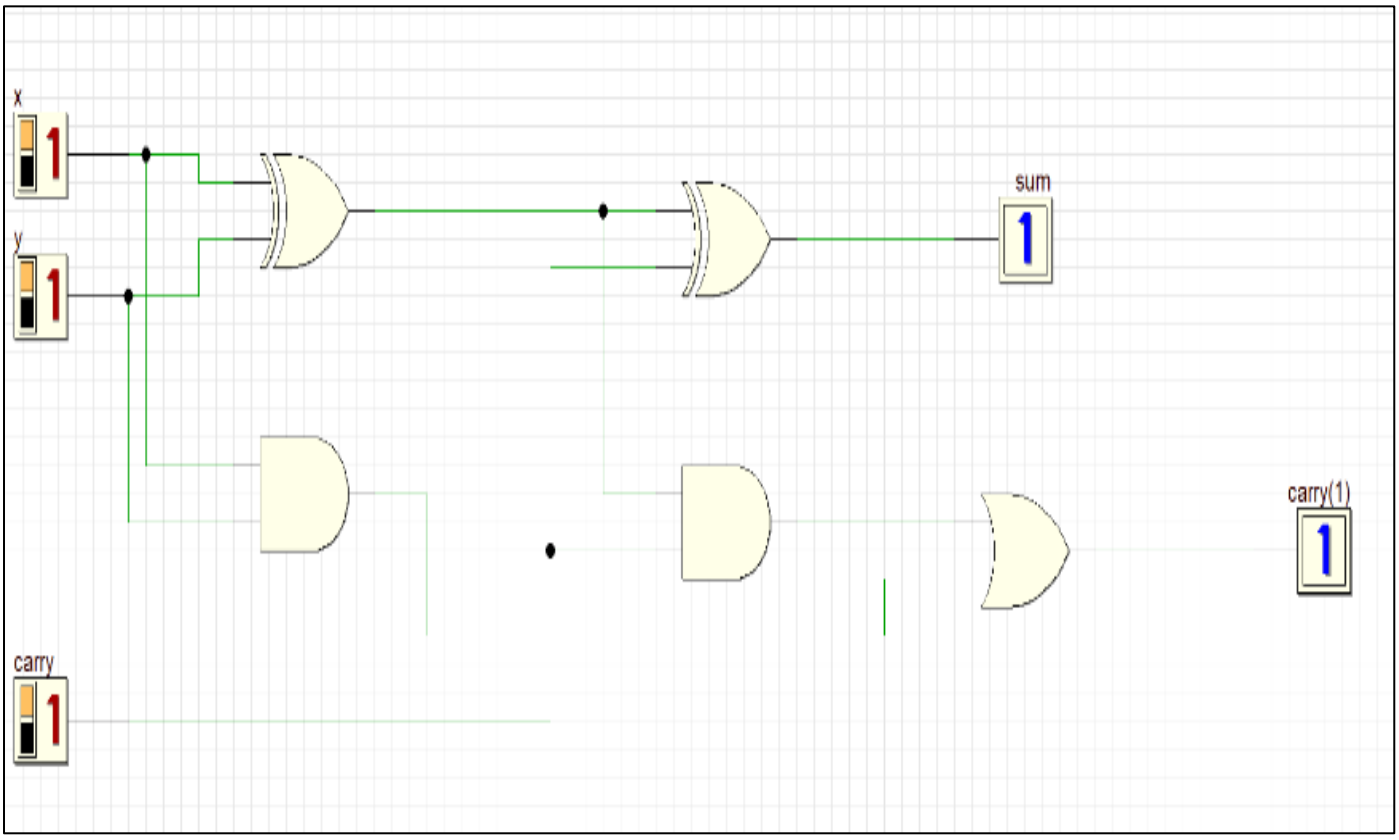

Fig 14: Full Adder Event Testing 8

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The event system in the truth table is identical to the one used in the DEEDS for digital electronics applications.

V. CONCLUSION

Adders are essential components in digital electronics, enabling binary addition which is fundamental to various computing tasks. Through the analysis of half and full adder circuits, their critical role in binary arithmetic becomes evident. The half adder, a basic unit, effectively processes two single-bit inputs to produce both a sum and a carry bit. Simulation results have confirmed that the half adder's outputs align with theoretical predictions, validating its performance in straightforward binary addition scenarios.

Building upon the functionality of the half adder, the full adder introduces an additional carry-in input, enabling it to handle three bits simultaneously. Simulations of full adder circuits showed that the outputs consistently matched the expected results across all test cases. This verification highlights the full adder's ability to perform more complex binary additions involving carry bits, which is crucial for precise arithmetic operations in larger computational systems.

The DEEDS simulator has proven to be an effective tool for modeling and validating these adder circuits. Both half and full adder simulations demonstrated that the practical outputs closely followed the theoretical truth tables. This affirms the significance of these adder components in digital design and underscores their reliability and accuracy in executing binary arithmetic, which is fundamental to digital computing processes.

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