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A Comparative Study on Ripple Carry Adder and Modified Square Root Carry Select Adder in Radix-4 8*8 Booth Multiplier

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Abstract:- In digital circuits multiplication is a fundamental operation, extensively utilized in various computational tasks. The efficiency and performance of the multiplier circuit significantly impact the overall system performances, especially in applications demanding high-speed computation with minimal power consumption. This study presents a comparative analysis between two distinct implementations of Radix-4 8*8 Booth multiplier employing different adder architectures: Ripple carry adder and Modified Square Root Carry select adder. Multiplier with modified square root carry select adder reduced critical path delay (CPD), power delay product (PDP) and area delay product(ADP). Generic process design kit (gpdk) of 45nm technology is used for design and implementation using Cadence software.

Keywords:- *Booth Multiplier; Carry Select Adder; Critical Path Delay; Power Delay Product; Area Delay Product; Cadence.*

I. INTRODUCTION

Multipliers act as a backbone for both Digital Signal Processing (DSP) and Very Large Scale Integration (VLSI) design, for numerous computational operations. It plays as an important key component in designing FIR filters, high performance systems such as Microprocessors, digital signal processors, etc. As sign of numbers are to be considered during multiplication, here comes Booth Algorithm, as it preserves the sign of the results. It is a hardware algorithm that is generally used in various DSP applications where faster multiplications are required. It reduces the number of partial products and additions as compared with other basic multiplication and uses shifting and addition operations to generate faster results.

In VLSI design, an adder act as the fundamental building block and often lies as a major part in critical path[1]. In order to meet the desired requirements researchers had carried out various adder structures designs[2]-[3]. The main goal is to achieve reduced power consumption. So, adders are designed in such away that it reduces the propagation delay. To achieve low power and high speed Ripple carry adder(RCA) authors of [4] adopted two versions featuring Gate diffusion input(GDI) structure which can be used in various applications and Gate diffusion input multiplexer full adder (GDI-MUX) design, which had eliminated the need of XOR/XNOR gates in full adder architecture. Using SPICE , the parameters such as delay, power, area, ADP and PDP are analyzed. In adders, addition of higher bit-width is also a major factor that effect the overall throughput of the circuit. So, by reducing the time required for highest bit-width addition, the throughput of the circuit can be can be improved. This is achieved by placing carry-look ahead adder, carry skip adder, carry select adder, conditional adder and combination of all these adders [5]-[12].

To the end, beyond the Ripple carry adder(RCA) a variety of adder structures have been proposed. In fact, RCA requires very small area and it is very easy to design, but results in more propagation delay which make them unsuitable for various high speed applications because of rippling of carry through the adder structures. So, in order to minimize the propagation delay of adders, Carry select adders and carry look ahead adders were designed. Conventional carry select adders(CSLA) [13] makes use of two RCAs, so area increased but lowered the propagation delay. Author of [14] proposed logic formulation design in order to eliminate the redundant logic operations by optimizing the logical technique in conventional CSLA. Here, the carry select operation is done before the calculation of final sum. As RCA makes use of two carry inputs, C_{in} =0 and C_{in} =1, Ramkumar and Kittur[15] proposed binary to excess one converter based CSLA. The proposed design achieved reduction in area and power [16], but with a small increase in delay. Kim and Kim [17] replaced two RCAs by one RCA and multiplexer based add-one circuit.

A modified carry skip adder was introduced in [18] by merging the idea of concatenation and incrementation block schemes and it was applied to conventional carry skip adder. Area had increased with an improvement in delay and energy efficiency.

Radix-2, Radix-4 and Radix-8 are the three variations of booth multiplier which generally differ by radix that they use for encoding partial products. In Radix -8 booth multiplier, each partial product is a multiple of 0,1,-1,-2,-3,-4,-5 or -6 of multiplicand, requires more hardware resources and have longer critical path and latency. In Radix -2 booth

multiplier, each partial product is a multiple of 0,1 or -1 and is more efficient for smaller operands. Where as in Radix -4 booth multiplier, each partial product is a multiple of 0,1,-1 or -2 of multiplicand. Here, the number of partial product is reduced by half and thereby reduces the number of addition operations in order to get the faster final results. So, for an efficient multiplication of binary numbers in digital signal processing applications Radix -4 booth multiplier is used.

In [19], it is observed that Radix-8 recoding leads to power efficient multiplier when compared with Radix-4 recoding. In[20], implemented 64- bit Radix-16 booth multiplier with partial product array height reduction. Optimized Radix-4 booth multipliers are discussed in [21]. As delay and power efficiency are the main factor that mainly affects the circuit design, modified booth encoder was used in [22]. By removing unnecessary circuit elements from the design had reduced the partial product generation.

As various applications like arithmetic logic units and digital signal processing requires high performance digital multiplications[23], Booth multiplier has become more popular choice as multiplier because of its reduced additions. Thus, achieved the two important characteristics required for designing integrated circuits that is reduced power and area requirements. Without binary additions 2's complement number conversion method is employed in [24]. 2's complement of a number is obtained by taking the complement of the number and then adding 1 to it.

A low power delay product Radix-4 8*8 multiplier is discussed in[26]. Logic optimization and binary to two's complement circuit design was used in order to achieve improvement in delay, power and PDP. It showed a better results as compared to the conventional booth multiplier. Pramod and Shahana[27] had focused mainly on adder structure. Proposed linear and modified square root carry select adder and compared the performance. Reduced delay performance was achieved by modified square root carry select adder.

The paper is systematized as: Radix-4 8*8 booth multiplier in section II, performance comparison in section III and conclusion in section IV.

II. RADIX-4 8*8 BOOTH MULTIPLIER

A. Implementation Using Ripple carry adder

Radix-4 8*8 booth multiplier[26] is used for the performance comparison. Here, the multiplier and multiplicand are of 8-bits and product will be of 16-bits, initialized to zero. Since, we are dealing with radix-4 the 16-bit product result have to be reduced by keeping only the lower 8-bits of the result.

Multiplier architecture will be same as that of conventional booth multiplier[26], but it eliminates the circuits which is not used for computation. Multiplier consists of 4- partial product stages in which partial products are generated parallelly. Stage 1 is implemented using 9-bit 2:1 and 3:1 Multiplexer, 2-input encoder and 9-bit binary to two's complement converter(B2C). Other 3- stages 2,3 and 4 consists of 2 input encoder, 9-bit adder/subtractor and 9 bit 3:1 multiplexer. Each stage gives 2- bit least significant bit (LSB), which is an input to the next stage. Finally, stage -4 gives the final product of remaining 9-bits.

In the booth multiplier, the adder/subtractor is implemented using Ripple carry adder for performing operation. Here, two ripple carry adders are used for two carry inputs, C_{in} =0 and 1 respectively. Two 1-bit full adder is used in stage 1 and 2, 3 and 4 bit ripple carry adders are used in stage 2, 3 and 4.

B. Implementation Using Modified square root carry select adder.

For performance comparison Radix-4 8*8 Booth multiplier [26] is used. Modified square root carry select adder [27] had reduced critical path and thus reduced the delay. Hence, the adder used in the architecture of multiplier is modified square root carry select adder. The design of the adder consists of carry-propagate and generate blocks which is designed using minimum number of logic gates, Nand carry chain block which uses NAND-NAND network in order to achieve reduced delay performances, through logic decomposition, area, delay and power efficient Module-carry generation block is used, carry-select blocks which make use of AND-NOR combination in order to generate inverted carry output and finally sum-generation block which is designed using XNOR gate for the generation of bitwise sum.

III. PERFORMANCE COMPARISON

Adders and Booth multipliers are designed using gpdk 45nm technology, developed using VHDL and analyzed in Cadence software RTL compiler v11.10.

Table I. shows the performance comparison of Ripple carry adder and Modified square root carry select adder. Here, 16-bit Ripple carry adder is compared with 16-bit modified square root carry select adder in terms of CPD, power, area, PDP and ADP.

Table 1 Performance Comparison between Adders

Adder	Bit width	CPD (ns)	Power (nW)	Area (sq.µm)	PDP (fJ)	ADP (sq.µm × ns)
Ripple carry adder	16	0.82	4585	189	3.75	165
Modified square root carry select adder	16	0.31	5520	246	1.71	76

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From above comparison table it is clear that though with a small increase in area and power consumption, modified square root carry select adder had showed better results in terms of delay, PDP and ADP.

Table 2 Performance of Various Multipliers

Radix-4 Booth Multiplier	Bit width	CPD (ns)	Power (nW)	Area (sq.µm)	PDP (fJ)	ADP (sq.µm × ns)
Proposed multiplier 2	8	0.84	25,763	831	21	698
Proposed multiplier 1	8	1.64	17,634	597	28	979
Conv.BM [26]	8	1.08	50,087	1237	54	1336
Conv.WTM [22]	8	1.04	23,542	656	24	682

Table II. shows the performance comparison between proposed multiplier 2 and proposed multiplier 1. The performance of proposed multipliers are also compared with other multipliers shown in the Table II. Proposed multiplier 1 represents the multiplier with ripple carry adder and proposed multiplier 2 represents multiplier with modified square root carry select adder, Conv.BM represents conventional booth multiplier in [26] and Conv.WTM represents conventional Wallace multiplier in [22]. Comparison is made between 8-bit multipliers in terms of CPD, power, area, PDP and ADP.

From the comparison Table II. it is clear that the proposed multiplier with modified square root carry select adder had showed better results in terms of delay, though with a small increase in power and area, but superior in PDP performance.

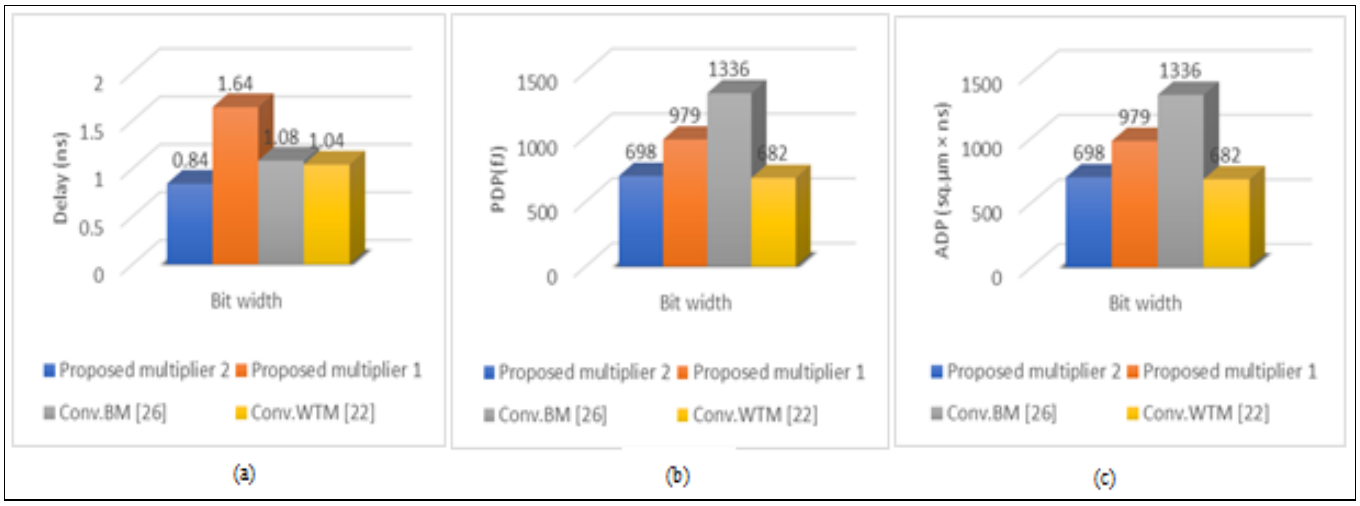

Fig. 1. Performance comparison for various multipliers.

Fig.1. shows performance comparison among various multipliers. Bit width of the Radix-4 booth multiplier chosen is 8. The implementation of proposed multiplier 2 had achieved a better results in terms of CPD, PDP and ADP. The CPD, PDP, and ADP are reduced by 48.9%, 25% and 28.7% respectively when compared to proposed multiplier 1. The CPD of the proposed multiplier 2 is reduced by 22.2% and 19% with respect to Conv.BM[26] and Conv.WTM[22] respectively. Power consumption, PDP and ADP of proposed multiplier 2 is reduced by 48.5%, 61.6% and 47.7% respectively when compared to Conv.BM[26] and PDP is reduced by 14.2% with respect to Conv.WTM[22].

IV. CONCLUSION

Radix-4 8*8 Booth multiplier with reduced critical path delaysss is presented. Two structures of Booth multiplier are implemented using two different adder architectures: Ripple carry adder and Modified square root carry select adder. Proposed Radix-4 8*8 Booth multiplier with Modified square root carry select adder is slightly ahead than the booth multiplier with ripple carry adder in terms of delay, PDP and ADP. The CPD, PDP, and ADP are reduced by 48.9%, 25% and 28.7% respectively.

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