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Design and Implementation of PLL with Dead Zone-Less Low-Power Phase Frequency Detector

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Abstract:- This project introduces a Phase-Frequency Detector (PFD) that includes a dedicated circuit for removing the dead zone. This design utilizes Pass Transistor Logic (PTL) and Delay Cells (DCs) to effectively address this issue. Additionally, a Low-Pass Filter is integrated into the system and connected with charge pump, employing a technique that replaces resistors with transistors, thereby significantly reducing the overall circuit area. Furthermore, a Phase-Locked Loop (PLL) serves to eliminate the dead zone and significantly reduce the circuit's size. This project aims to advance circuit design methodologies by enhancing performance and minimizing area requirements.

Keywords:- *Phase Frequency Detector, Low-Pass Filter, Pass Transistor, Delay Cells, Charge Pump, Phase-Locked Loop*

I. INTRODUCTION

Phase-Locked Loops (PLLs) function as the brain of many modern communication and hardware systems. Recent research [1-3] has extensively focused on PLL circuit design, with ongoing studies aimed at enhancing its application in current technology. Most investigations have concentrated on achieving a higher lock-in range, shorter lock-in time, and acceptable phase noise. PLLs are crucial in various adaptable applications, including clock locking and control recovery in microchips, microcontrollers, microprocessors, and repeater synthesizers. In modern communication systems, PLLs are essential for synchronization, clock synthesis, and the reduction of skew and jitter. A phase-locked loop (PLL) design comprises five main components: Phase-frequency detector, charge pump, low-pass filter, voltage-controlled oscillator, and frequency divider. PLL circuits consist of the components mentioned above. Due to its wide range of applications, PLL design has undergone numerous revisions.

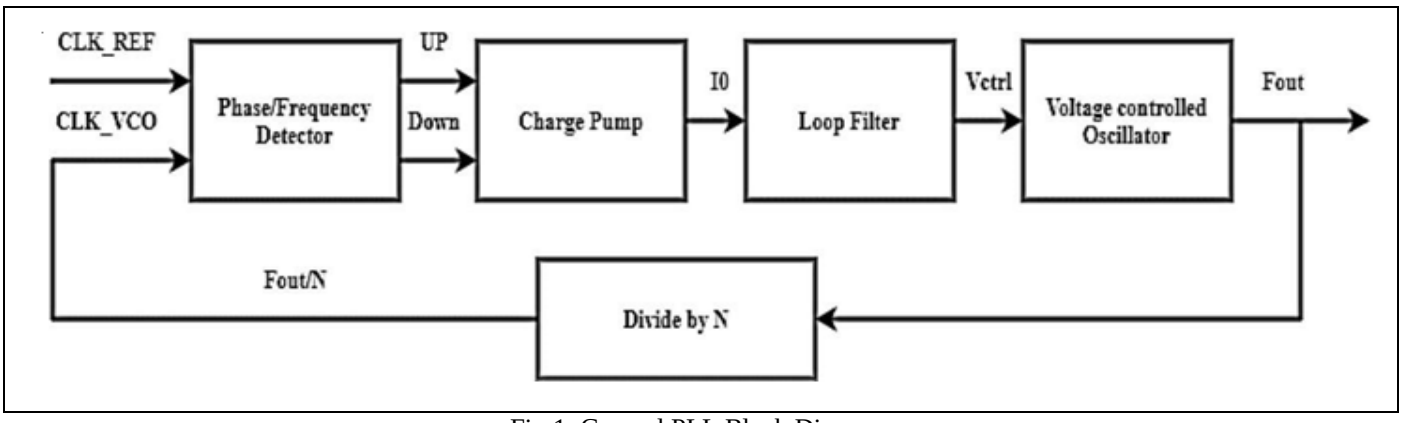

Fig 1: General PLL Block Diagram

This paper holds several sections, each addressing specific aspects: introduction, Phase-Locked Loop (PLL), methodology, implementation, results and discussion, and conclusion.

II. PHASE LOCKED LOOP

A. Phase Frequency Detector

A PFD produces a voltage output signal which is proportion to the phase difference between two input signals. PDs can be based on XOR gates or phase frequency detectors (PFDs). PFDs compare the rising or falling edges of input signals, making its width irrelevant.

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B. Charge Pump and Loop Filter

Charge pump is constructed using transistors which is considered as current source and two latches, correspondent to the UP and DOWN signal, that are considered as results from PFD. Whenever the UP signal goes high, current is entering in the circuit, and when the signal DOWN, goes high, current is exiting the circuit. Loop-filter's role is to convert the PFD's output signal into a control-voltage and to filter out high-frequency noise. In PLL circuit, the loop-filter serves two primary functions: ensuring stability and reducing ripples in the phase detector's output.

C. Voltage Controlled Oscillator

Voltage-controlled oscillators (VCOs) are crucial components in many electronic systems. VCO generates a sine wave or square wave output based on an input control voltage, based on the specific oscillator type used. The current-starved VCO is the most used circuit types.

III. METHODOLOGY

A. Phase Detector

A charge pump PFD is employed in this project. To mitigate this issue, a circuit employing PTL logic and delay cells (DCs) is used to remove the dead zone. In Figure 2, the described PFD architecture makes use of Pass Transistor Logic and Delay Cells (DCs) with an enhanced reset path to improve the linearity of this circuit. Inverters (INV1, INV2, INV3, INV4) are utilized to set the nodes U1 and D1 to definite logic levels, either high (Vdd) or low (0). Furthermore, inverters (INV5, INV6, INV7, INV8) are responsible for producing delayed UP and DN signals. The signals CLKDref, CLKDfb, UPD, and DND are the delayed versions of CLKref, CLKfb, UP, and DN signals, respectively. The transistors (Mu4, Mu5) and (Md4, Md5) form the discharge paths for the UP and DN signals accordingly.

The proposed PFD operates as follows: Initially, nodes X and Y are pre-charged to Vdd, which is the supply voltage. Presence of transistor Mu3 ensures that node U1 reaches Vdd − Vth (where Vth is threshold voltage) because node X is maintained at Vdd by the Mu2 transistor. This causes node U1 to exceed the inverter's switching threshold, resulting in UP going high (Vdd). When CLKfb goes high, DN also goes high. When both UP and DN are high, nodes U1 and D1 are reset to zero, thus resetting UP and DN to zero as well. Similar will be the operation of the proposed PFD circuit when CLKfb leads CLKref.

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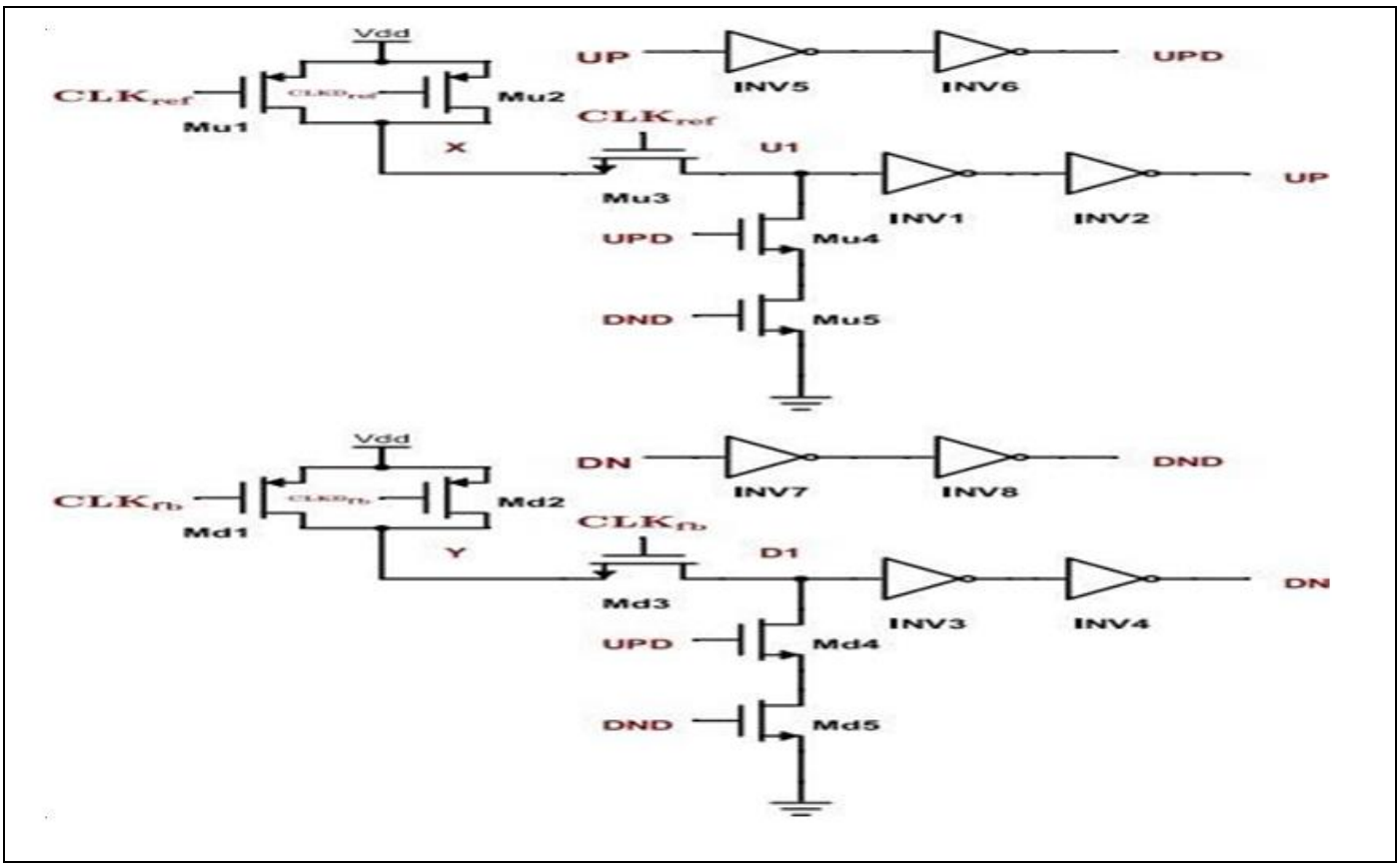

Fig 2: Circuit of Phase Frequency Detector

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B. Charge Pump with Low Pass Filter

The charge pump follows the phase-frequency detector (PFD) in a PLL. The timing/phase of output of VCO and reference are then compared by phase frequency detector, generating current pulses whose width corresponds to the timing or phase error.

Charge pump (CP) is essentially two switched current sources that inject or drain charge from the loop filter (LPF). The topmost PMOS and bottommost NMOS transistors act as the current sources, while the other PMOS and NMOS in the middle are connected to the UP and DOWN outputs of phase detector, respectively, as illustrated in Figure 3.

When the UP signal goes high, the PMOS turns on, connecting the current source to the loop filter. Similarly, when the DOWN signal from the PFD goes high, the same action occurs.

Switched capacitor technique is applied to replace the resistor of low pass filter because it is easier to fabricate reliably with reduced area. A switched capacitor operates by transferring charges in and out of capacitors through the opening and closing of switches. Typically, non-overlapping signals φ1 and φ2 control these switches, as depicted in Figure 4.

➢ *The Relation between Rand C1 is given by,*

- $R = 1 / (C1 * f)$

Thus, the resistance R is reciprocal of frequency (f) when capacitor C1 is constant, and resistance (R) is reciprocal of capacitor when frequency is constant hence for high resistance, we have to decrease frequency.

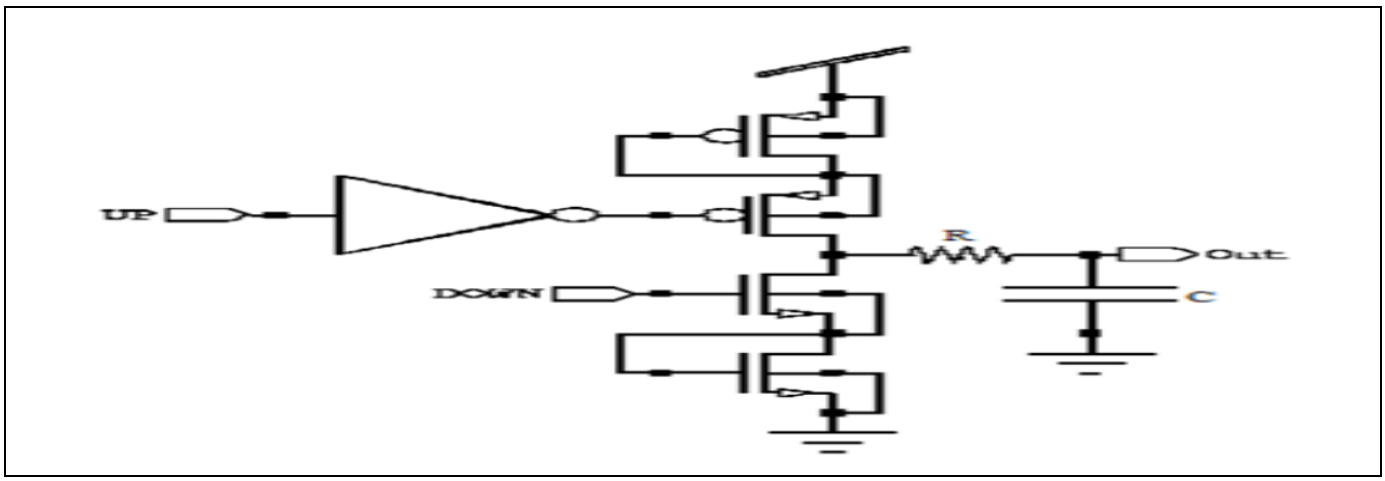

Fig 3: Schematic Diagram of Charge-Pump and Low-Pass Filter

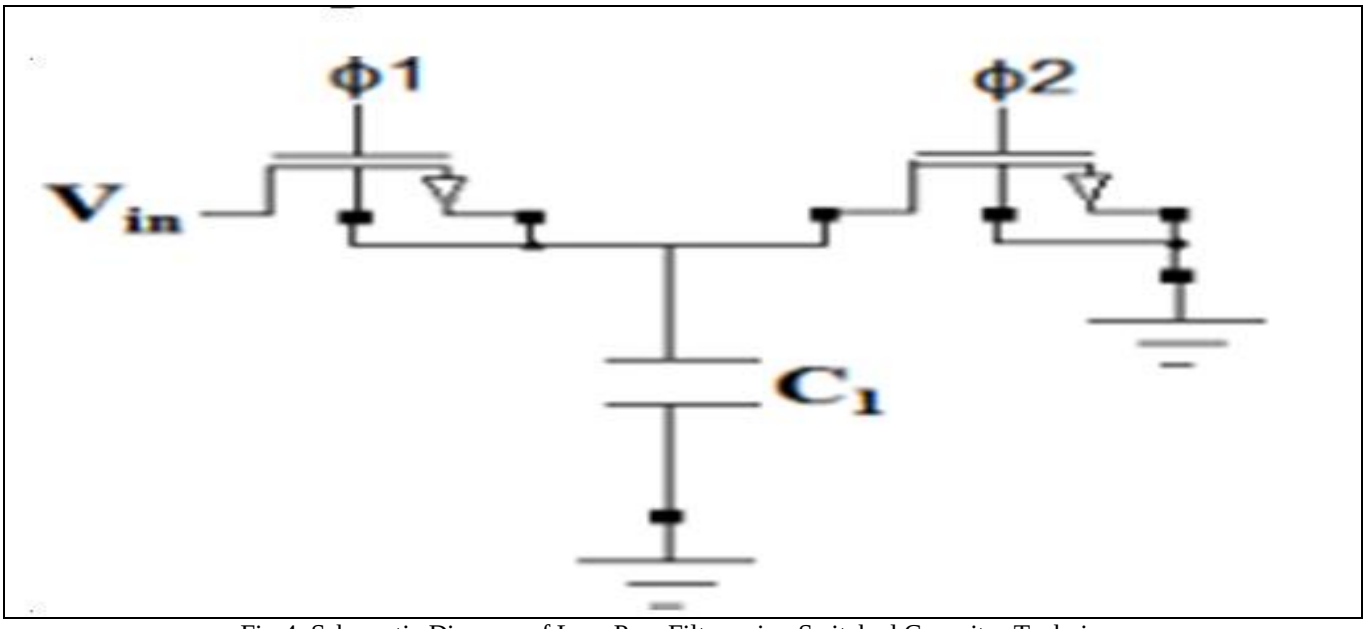

Fig 4: Schematic Diagram of Low-Pass Filter using Switched Capacitor Technique

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C. Current-Starved Voltage-Controlled Oscillator

In every system or device controlling is a key factor. CS-VCO was built using three inverters that were coupled in cascade way including PUN and PDN. In Fig.5 the pull-up network (PUN) consists of PMOS-connected loads, while the pull-down network (PDN) is constructed using NMOS transistors.

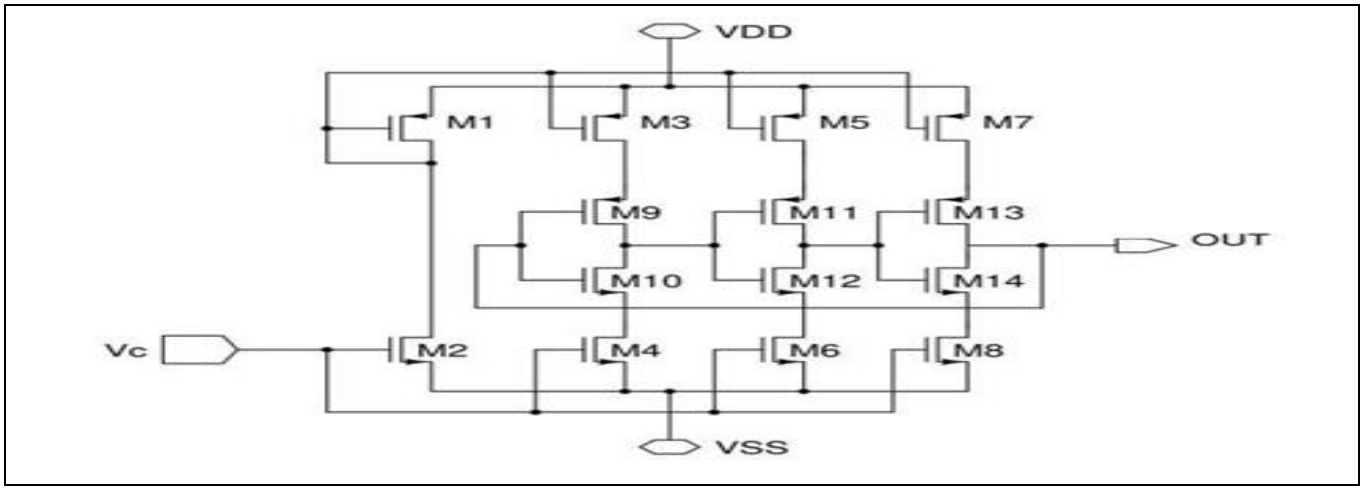

Fig 5: Schematic Diagram of CS-VCO

D. Frequency Divider

The frequency acquired from the VCO is divided using the frequency divider [5]. It is placed in feedback path and PLL creates a closed loop. The Frequency Divider splits a frequency by two using a simple D-Flip flop built using a Pass transistor.

IV. RESULTS AND DISCUSSION

All the designed circuits were implemented using the GPDK45 (45nm) library's CADENCE Virtuoso Analog Design Environment. The implementation is done, where the individual components were designed first and later all the individually designed components were combined together.

A. Phase Frequency Detector

The PFD consumes 28.8 μW and operates at 100 MHz with a supply voltage of 1.2 V. At a frequency of 100 MHz, the charge pump output node (VCTRL) is initially set to 900 mV, with a CP current of 100 μA. Simulation results confirm that the proposed Phase Detector is insensitive to duty cycle variations, maintaining a dead zone free operation even with input clocks having different duty cycles. Figure 6 illustrates the implementation for the Phase Frequency detector architecture. Fig 7, 8, and 9 represents the transient simulation at a clock frequency of 100 MHz. The simulation covers three scenarios: (a) CLKref and CLKfb having the same phase and frequency, (b) CLKref leading CLKfb, and (c) CLKfb leading CLKref.

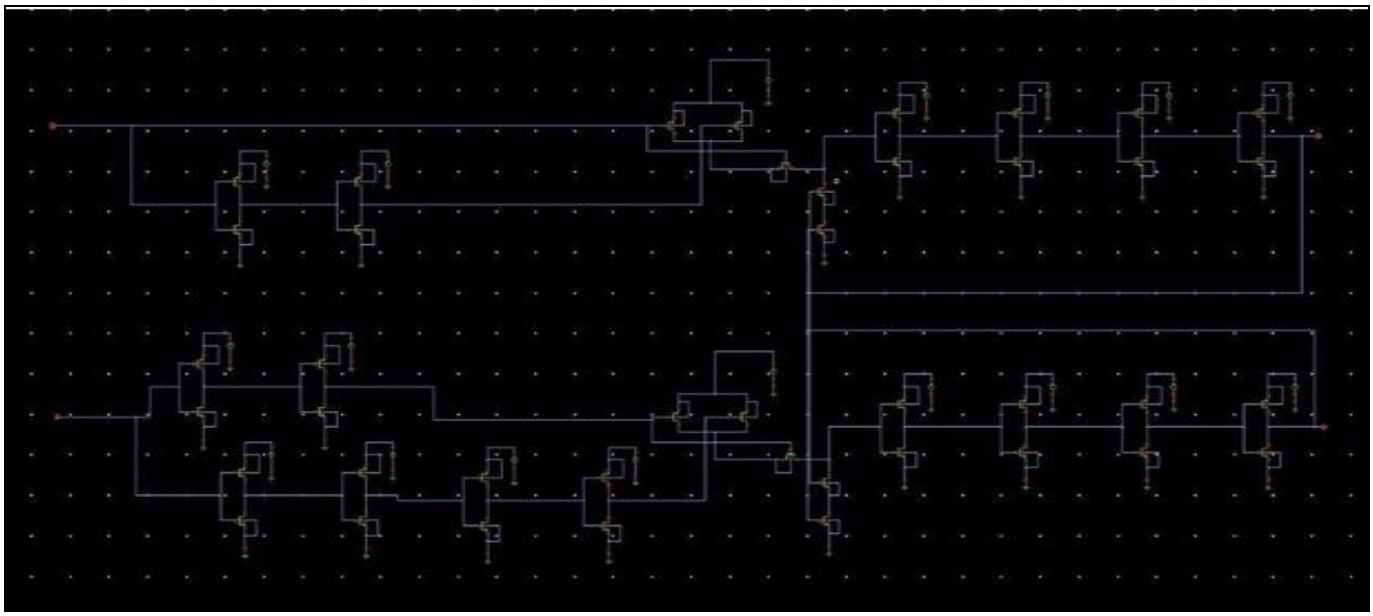

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Fig 6: Implementation of Phase-Frequency Detector

Fig 7: Transient Response of the PFD when CLKref and CLKfb having Same Frequency and Zero Phase Shift

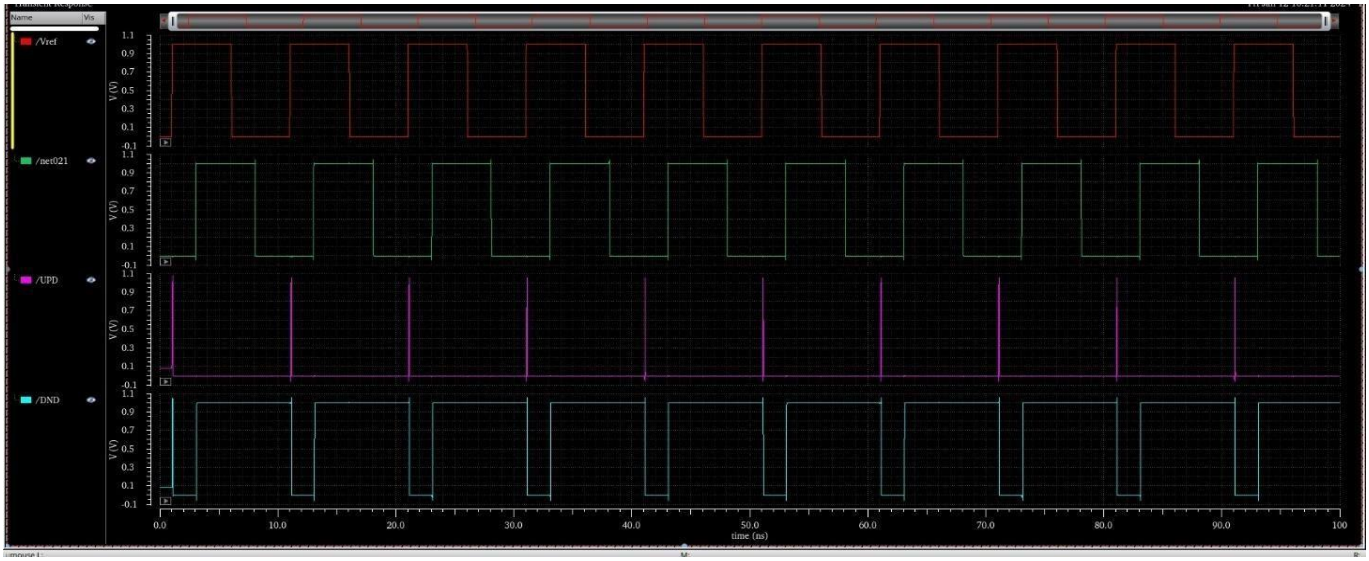

Fig 8: Transient Response of the PFD when CLKref leads CLKfb

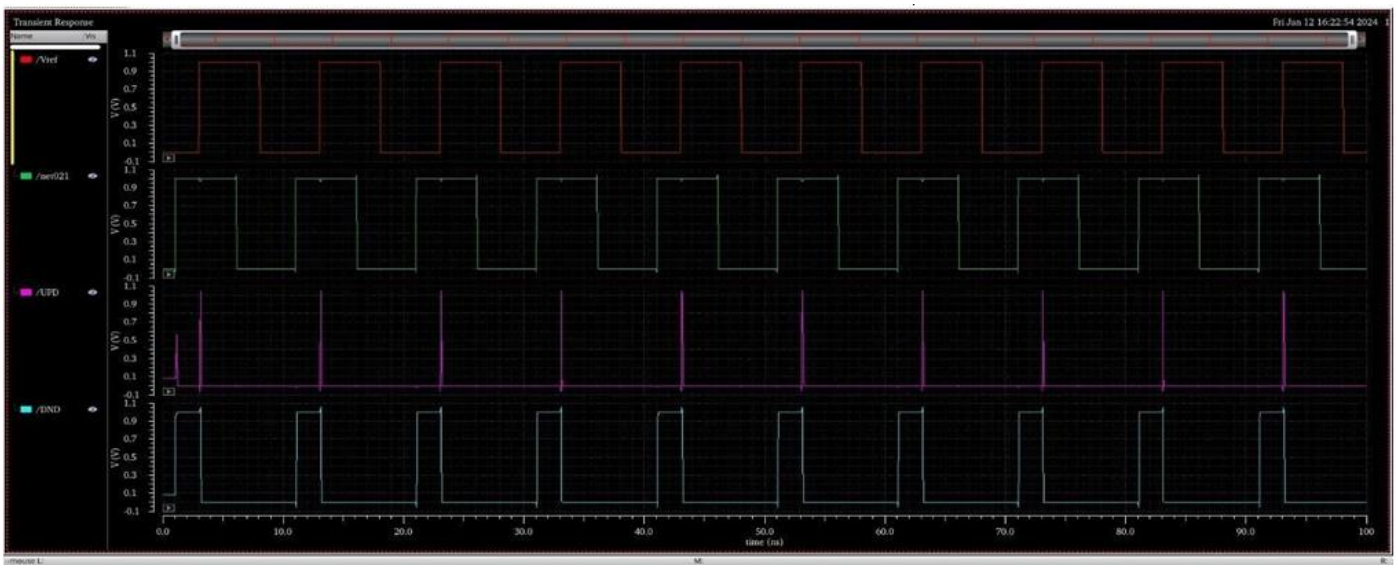

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Fig 9: Transient Response of the PFD when CLKfb Leads CLKref

B. Charge Pump along with Low Pass Filter

The charge pump (CP) will be used to charge or discharge the capacitors of the low-pass filter according the outputs (Up and Down) of PFD. When Up pulse is high, the CP charges the capacitor, thereby raise up the output voltage. The two-input voltage (Up and Down) and the output of charge pump alongside low-pass filter as shown in Fig. 10. The output of it determines the voltage-controlled oscillator frequency.

The CP is designed to have current IP of 100 µA. The dynamic behavior of CP-PLL can be studied by establishing the relationship between control voltage (Vc), charge pump current Iup (Idown) and phase difference Δφ

$$V_c = \frac{I_{Up} T_{in}}{2\pi C_2}, \Delta\phi_e = \frac{I_{Up}\phi_f}{4\pi f_{in} C_2}$$

This means Vc rises in steps proportional to the ratio 2 Iup / C2 in every time period Tin. C1 and C2 are capacitors used in switched capacitor low pass filters. f is the frequency of input clocks φ1 and φ2, used for activation of MOS transistor switches.

$$\omega_o = \sqrt{\frac{I_{Up} K_{VCO}}{2\pi C_2}} \text{ and}$$

$$\eta = \frac{1}{2C_1 f}\sqrt{\frac{I_{Up} C_2 K_{VCO}}{2\pi}}$$

➢ *The Free Running Frequency and Damping Factor are Given by:*

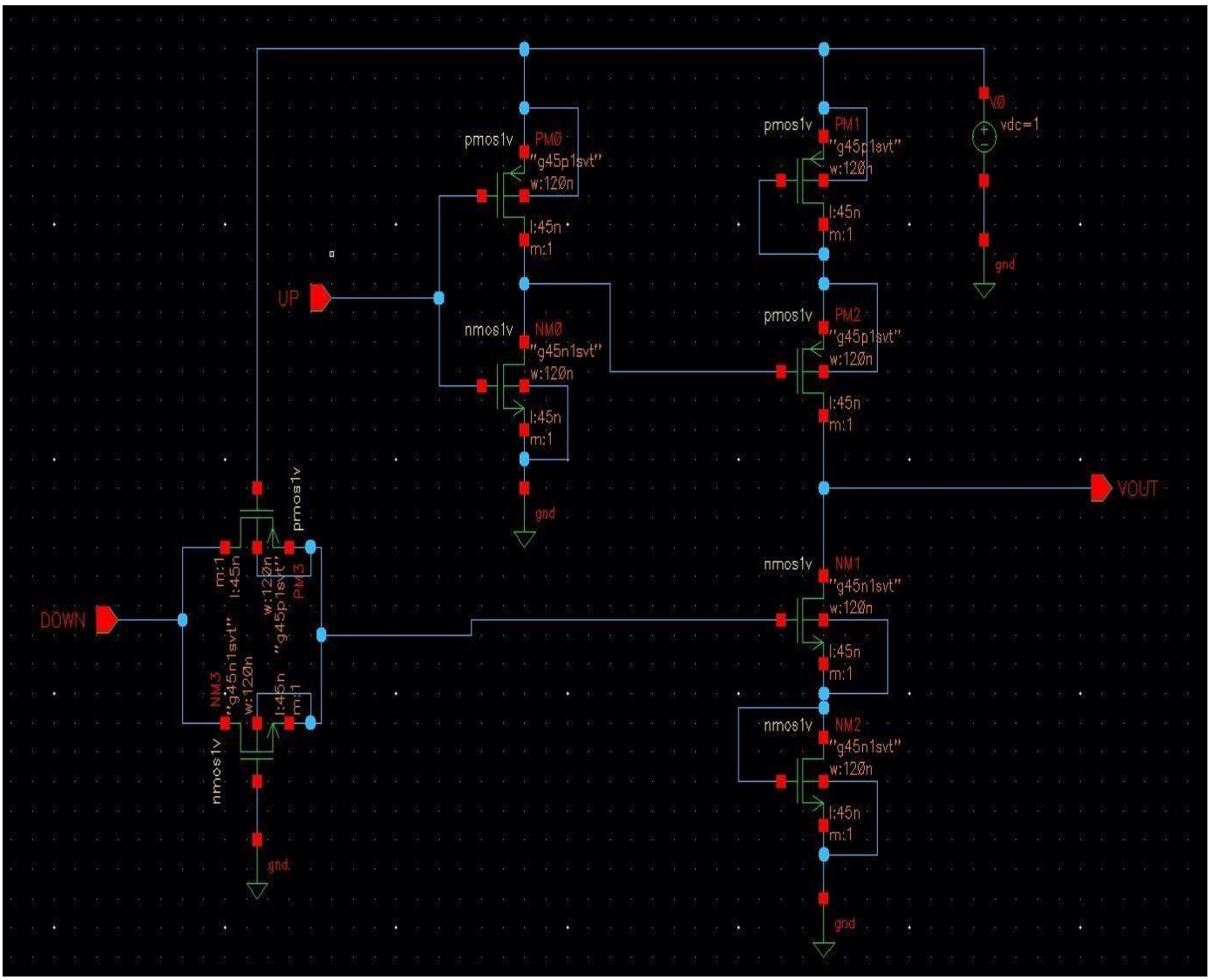

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Fig 10: Circuit Implementation of Charge Pump

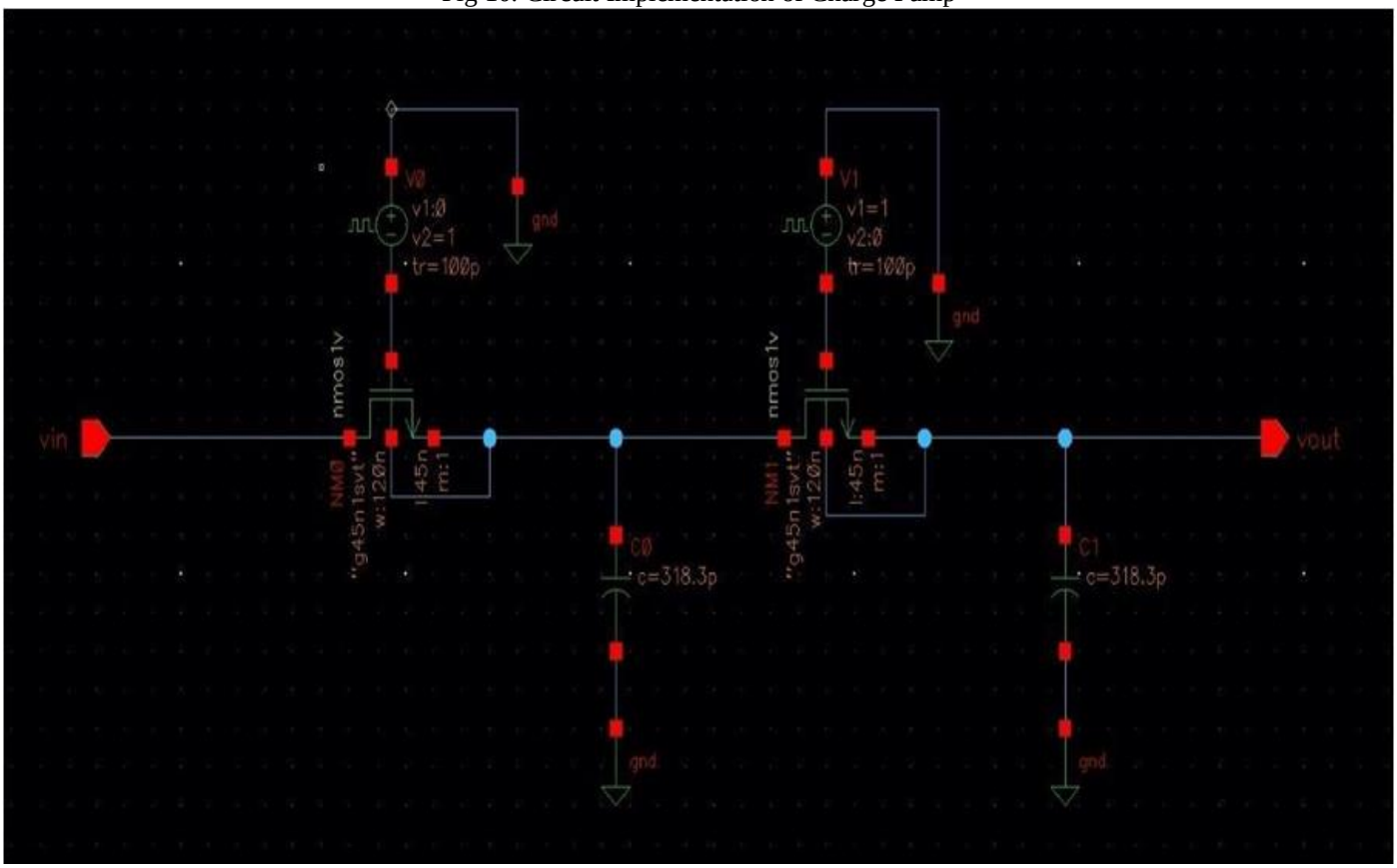

Fig 11: Circuit Implementation of Low-Pass Filter

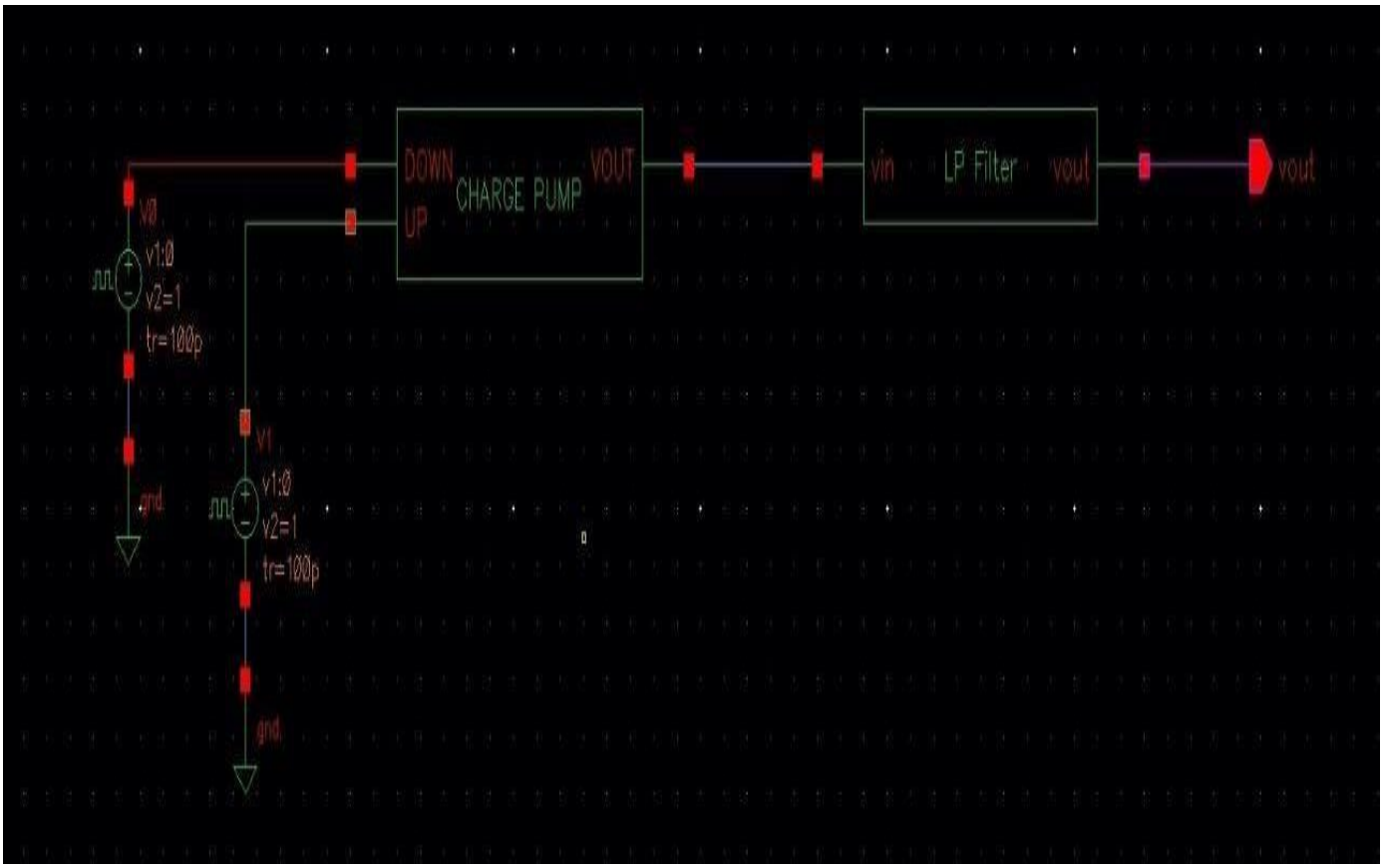

Fig 12: Circuit Implementation of Charge Pump Along with Low Pass Filter

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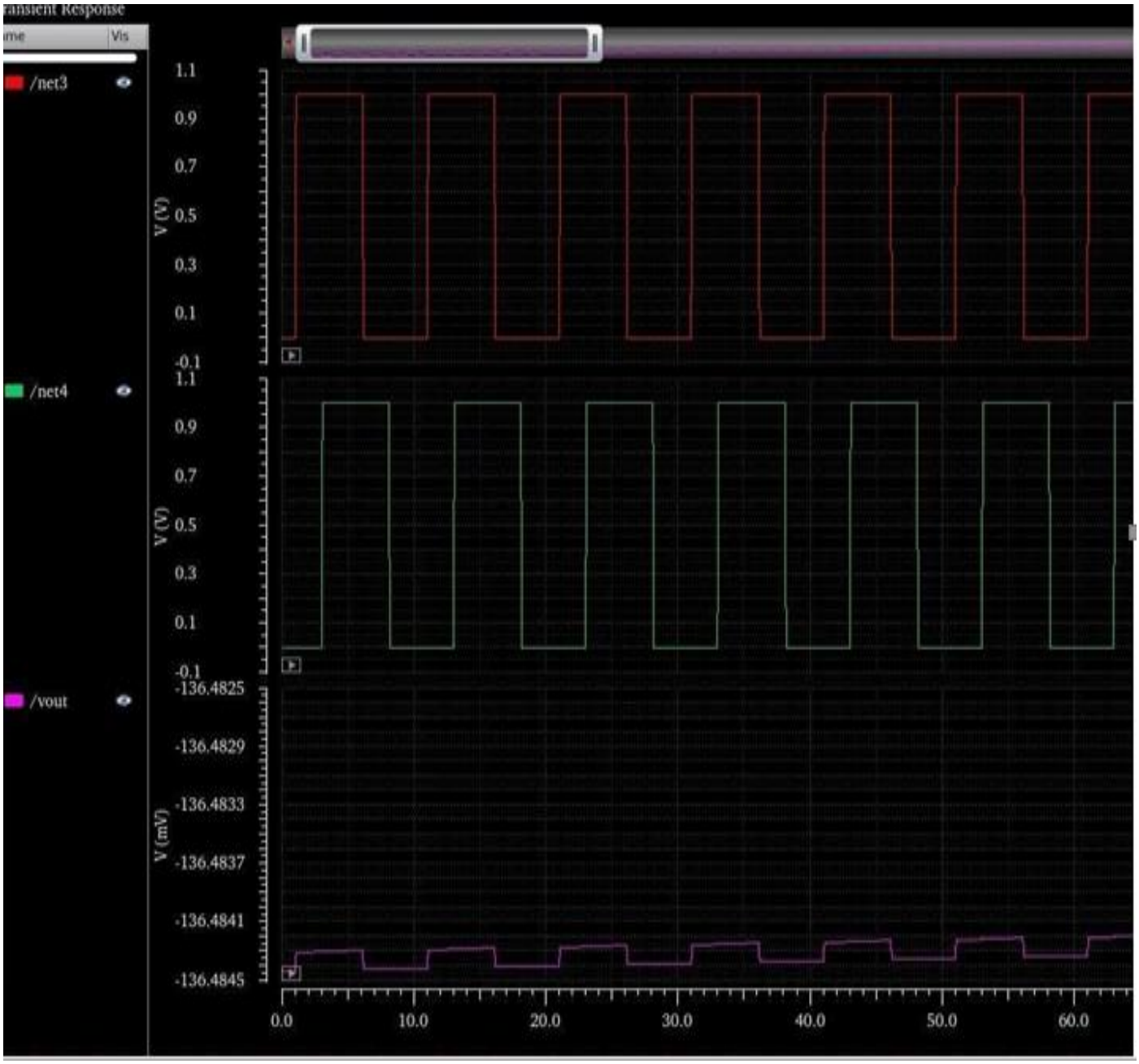

Fig 13: Simulation Waveform of Executed Charge Pump with LPF

C. Current Starved VCO

Implementating three-stage CS-VCO using Cadence tools is depicted in Fig 14, utilizing a 1.2 V supply voltage. The current mirror circuit, positioned on the leftmost side, is constructed from a set of transistors. In the initial stage, the transistors function together to form an inverter, which is then followed by a cascade of inverters created by the subsequent transistors.

The lower current mirror transistor's gate receives control voltage, which serves as the VCO's input. The critical elements of the circuit are the transistors forming the current source, which regulate the amount of current supplied to the inverters. This regulation ensures that the inverters receive only the necessary current, effectively preventing excess current flow. The design incorporates three stages, each containing cascaded inverters, a current mirror circuit, and transistors acting as the current source. The output from the final stage is fed back to the first stage. The control voltage, which ranges from 0.8 to 1.2 V, serves as the VCO input. This value begins at the NMOS transistor's threshold voltage of 0.8 V.

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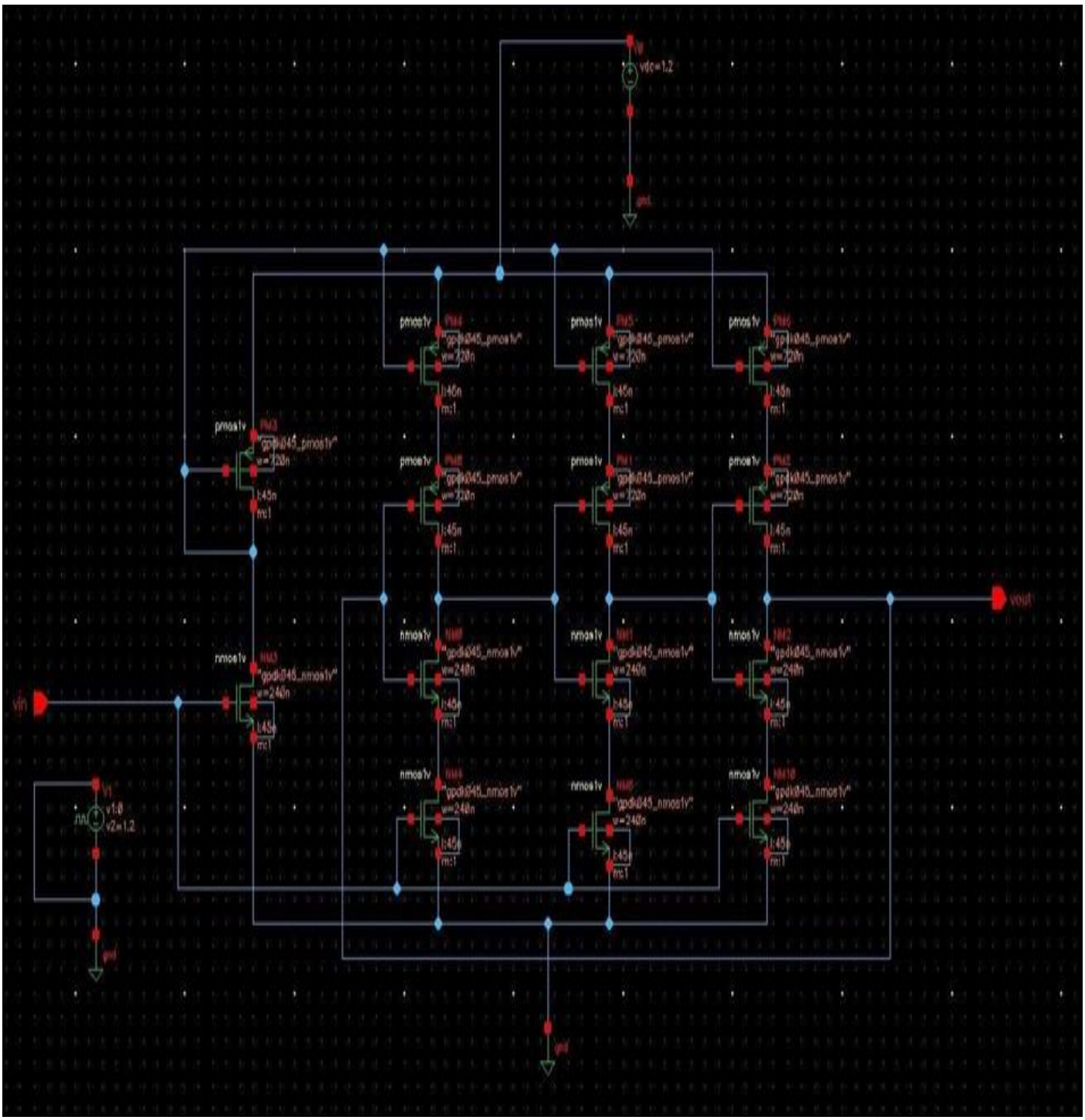

Fig 14: Schematic Diagram of 3-Stage Current Starved VCO

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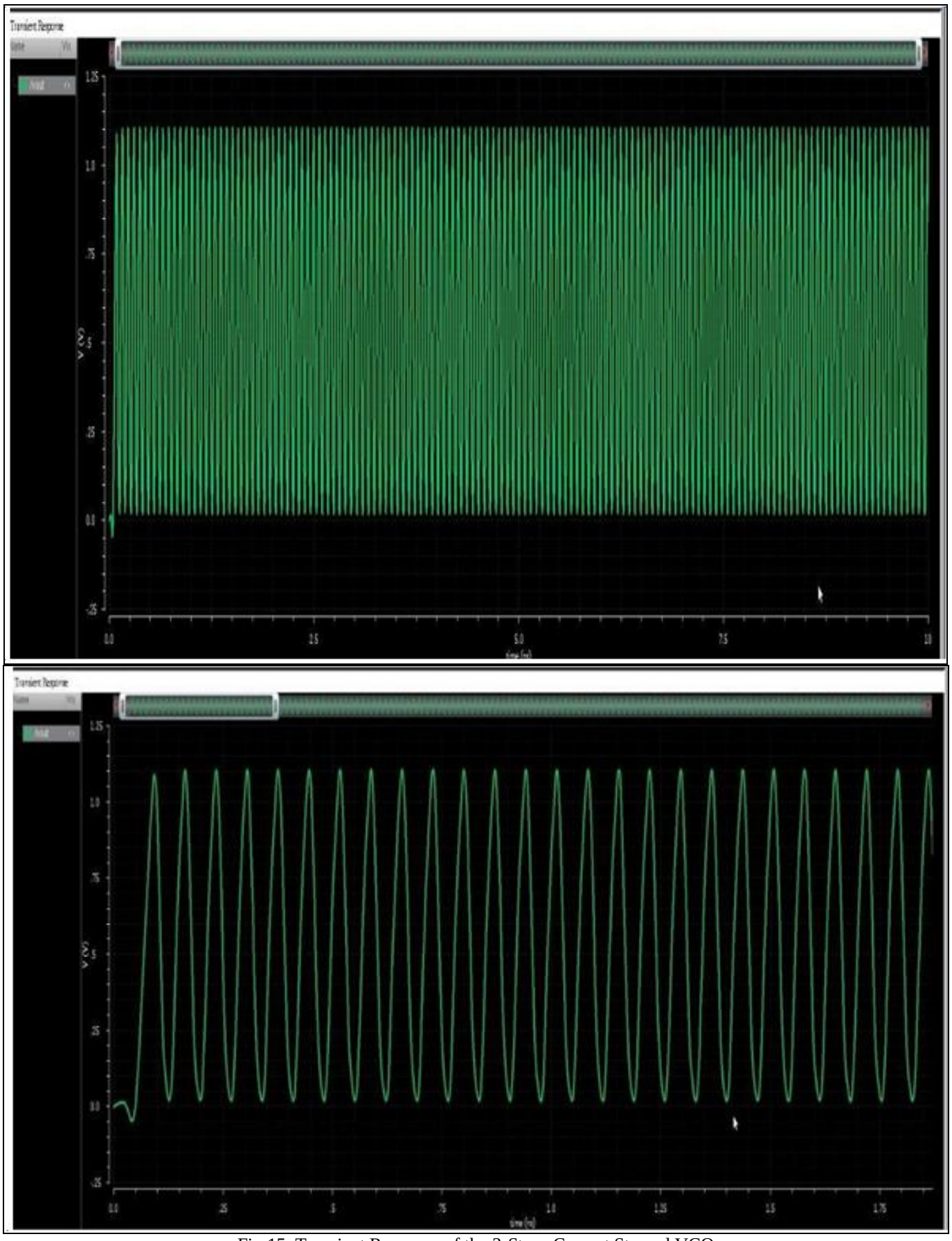

Fig 15: Transient Response of the 3-Stage Current Starved VCO

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D. Phase Locked Loop

After implementing each PLL sub-block, the components are integrated to form a complete PLL system. Fig 16 provides a detailed illustration of the PLL integration process, incorporating all its sub-components. In operation, the charge pump receives the differential phase between the input and feedback signals from the PFD and amplifies the voltage generated by the phase error. This voltage is then filtered by the loop filter to remove noise before being sent to the VCO. The VCO generates a sinusoidal signal at a specific frequency, which is then sent to the frequency divider. Frequency divider divides the signal by a factor of N. VCO frequency adjusts until it matches the input frequency, entering lock mode. The PLL loop continues until both the reference clock (clk_ref) and the VCO clock (clk_vco) achieve a locked state.

The PLL targets an output of 2 GHz frequency, with a reference clock frequency (CLKref) of 125 MHz. The charge pump (CP) is designed to provide a current of 100 µA. VCO is implemented as a 3-stage current-starved ring oscillator, and the frequency divider circuit has a divide ratio (M) of 16.

Simulation results indicate that the PFD achieves 100% linearity and dead zone for a phase difference ranging from $-\pi$ to $+\pi$ is 0. The PFD consumes 28.8 µW of power at an operating frequency of 100 MHz. Additionally, the overall power consumption of the designed circuit measures 288 µW.

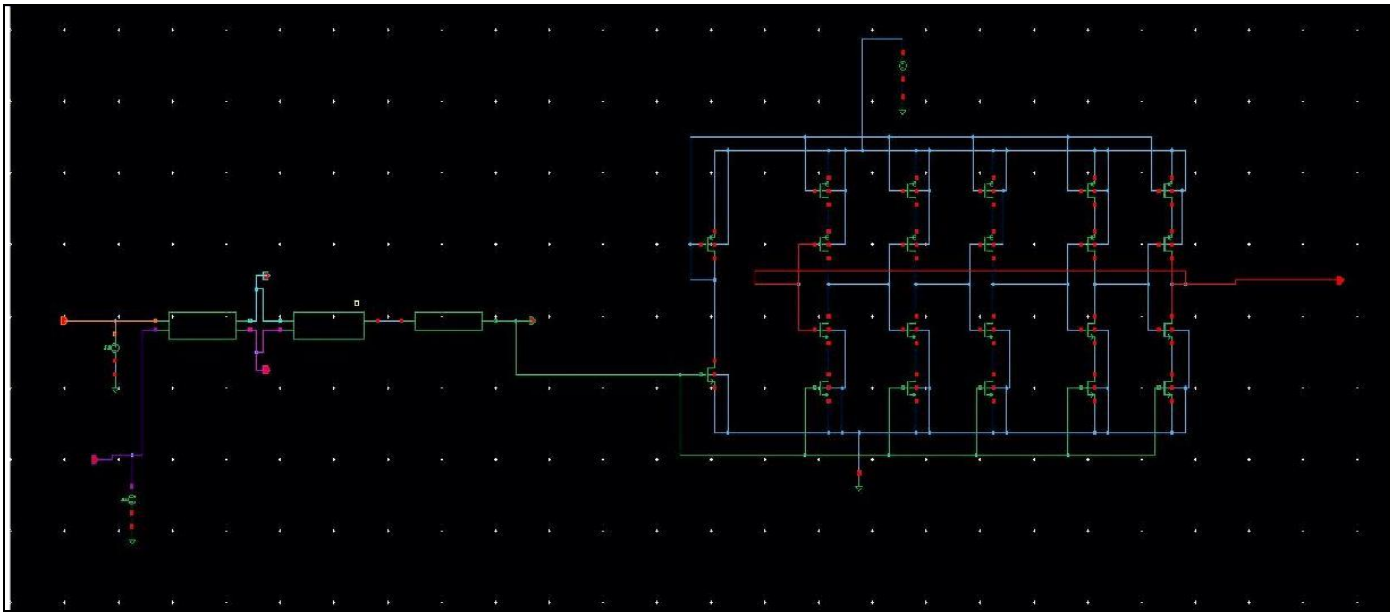

Fig 16: Integration of all Individually Designed Components to form a PLL Circuit

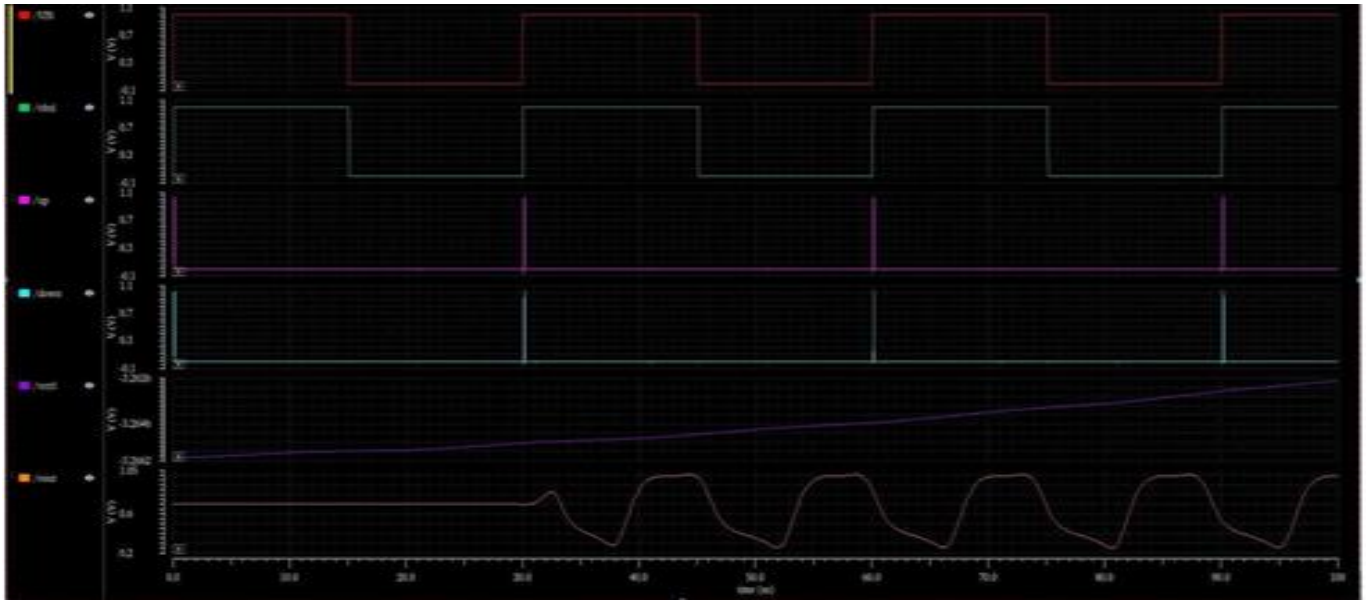

Fig 17: Represents the Simulation Waveform of the PLL Circuit

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V. CONCLUSION

In this study, a Phase Frequency Detector using Pass Transistor Logic and Delay Cells is proposed and designed. The proposed PFD is free from dead zone and exhibits lower power consumption compared to PFDs reported in the literature. The developed PFD functions at a 50 MHz frequency and exhibits a mere 14 µW power consumption, representing a 58.2% reduction from conventional architectures. The charge pump's accompanying low-pass filter utilizes a switched capacitor technique, substituting resistors with transistors and capacitors, effectively lowering the overall power consumption. This methodology ensures reduced power usage while maintaining high efficiency levels.

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