ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24MAR1218

Performance Analysis of Vedic Multiplier in Hardware Implementation of Biomedical Applications

Dr. Meenakshi Agarwal[1]
Skill Assistant Professor, Shri Vishwakarma Skill University, Haryana

Abstract:- As technology advances at a rapid pace, there is an increasing need for real-time digital signal processing (DSP) applications that are efficient and swift. DSPs, or digital signal processors, are crucial components of several engineering disciplines. For processes like convolution and Fourier transforms in DSPs, rapid multiplication is essential. Multiplication is one of the basic mathematical operations used by all applications. Many different multiplier designs have been developed to boost their speed. When compared to array and booth multipliers—the products of decades of hard research—vedic multipliers are among the fastest and lowest power multipliers. The sixteen sutras, or algorithms, that the Vedic Multiplier uses are primarily logical procedures. They are the fastest and most effective because several of them have been proposed using the Urdhava Tiryakbhyam sutra. The purpose of this study is to provide an overview of the numerous biomedical applications of Vedic Multiplier in the wide field of digital signal processing, including denoising of Electrocardiogram (ECG) and Electroencephalogram (EEG) signal. Particular attention is paid to how current Vedic Multiplier designs have been altered to increase speed and performance metrics.

Keywords:- *Vedic Multiplier, Urdva Tiryakabhyam, Nikhilam Sutra, Digital Signal Processing, ECG, EEG Signals.*

I. INTRODUCTION

Rebuilding traditional mathematics with the help of ancient Indian manuscripts known as the Vedas is known as Vedic Mathematics. Sixteen sutras spanning a variety of mathematical topics, such as algebra, geometry, and arithmetic, form the basis of this system [1]. Since both area and delay rise gradually as bit count grows, Urdhva Tiryagbhyam is the most generic sutra for developing Vedic multiplier designs [2]. Recently, in a work, the FIR filter method use a vedic multiplier and carry lookahead adder based architecture to denoise the Elec- troencephalogram (EEG) data. The purpose of the carried lookahead adder and vedic multiplier based FIR filter is to efficiently denoise the EEG signal [3]. The significance of Vedic multipliers is in their ability to solve complex mathematical problems quickly through vocal solutions [4]. This work proposes an 8-bit multiplier for the creation of partial products, based on the UrdhvaTiryagbhyam sutra, a work of Vedic mathematics. In a recent research work, Padmavathy et. al presented the carry skip approach in the Vedic multiplier to achieve partial product addition. This multiplier is intended for the addition of a partial product. The logic levels of the ripple carry adder are changed to add the output of these Vedic multipliers. With the use of this suggested quick FIR filter, ECG noise can be effectively eliminated [5]. As we can see, because the partial products are computed separately and concurrently, the array multiplier requires less processing time. The delay associated with the array multiplier is the amount of time it takes for signals to flow through the gates that comprise the multiplication array [6]. Another way to speed up multiplication is to arrange adders [1]. There are two methods for this: the Wallace tree method and the Carry Save Array (CSA) method. The CSA method processes each bit separately and sends a carry signal to an adder one bit higher in place. The CSA technique has several limitations since the bit count of the multiplier influences the execution time. The carry output signal is sent to the subsequent stage of the full adder after being transferred to the full adder of the same number of bits in the previous stage. Three bit signals are sent to a one bit full adder in the Wallace tree approach, and the sum is then given to the subsequent stage of the full adder of the same bit [7]. This reduces the number of incomplete products using the Booth algorithm. However, large booth arrays are required for high speed multiplication and exponential calculations, which require massive partial sum and partial carry registers. It takes roughly n/(2m) clock cycles to multiply two n-bit operands by a radix-4 booth recording multiplier, where m is the number of booth recoded adder stages. This produces the least significant half of the result. As such, this situation is associated with a large propagation delay [8]. The Wallace tree multiplier utilising a modified booth encoding utilises the wallac tree for quicker additions and the modified booth method to reduce partial products [9-13]. It has recently been asserted in a number of studies that a fast multiplier based on the Urdhva tiryakbhyam sutra, an old Indian Vedic mathematical formula, works faster than other known multipliers. Fixed point FIR filters, convolution, digital filters for ECG and EEG signal denoising, square architecture, etc. have all been implemented using Vedic multipliers [9, 15]. Additionally, they are very useful in situations involving image pro- cessing where space and time are conserved. Image processing is the process of performing certain procedures, such as edge detection, pattern recognition, and sharpening, to photographs in order to enhance a particular feature or

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24MAR1218

extract significant data. Consequently, it is essential in the fields of medical image processing, robotics, holography, x-ray imaging, mapping etc. [2, 14-17]. In this paper, section 2 shows Vedic Matchematics basics. Execution of Vedic Sutras in Biomedical applications is carried out in Section 3. Section 4 shows the Performance Analysis. And Section 5 concludes the paper.

II. VEDIC MATHEMATICS BASICS

Vedic mathematics is a time-tested technique for rapid computation that provides a unique method of mental calculation with the use of simple rules and precepts. Between 1911 and 1918, the holiness Jagad Guru Shree Bharti Krishna Tirtha JiMaharaj (1884-1960) rediscovers the Veda. The 16-Sutra (Algorithm) and 16-up- sutra (Sub-algorithm), according to in-depth research in the Atharva Veda, are the cornerstones of all Vedic mathematics, according to Swami-Ji [18]. It provides a powerful method that quickly and simply computes all mathematical operations, regardless of how basic or complex they are [13]. Compared to modern mathematics, it is more consistent and provides a quick answer. The rapidly advancing technology in signal processing have led to significant progress in accelerating output. It is based on sixteen sutras covering a variety of mathematical subjects, including algebra, geometry, and arithmetic. In most engineering system design courses, modern mathematics is a mandatory subject since it is based on a multitude of mathematical concepts. When utilizing the Vedic mathematics algorithm, quick processing speed is necessary. Moreover, hardware design must be carefully studied in order to use the Vedic mathematics sutras for DSP applications. Multipliers, which are utilized in many different applications like digital filters, are the primary instrument for signal processing [14]. The fundamental component of any processing unit is its inclusion and multiplication scheme, the performance of which determines the efficiency and accuracy of the filter's operation. The size of the filter also slows down the operation overall by causing more multiplication. Thus, optimizing area and pace present a difficult task that contradicts itself when it comes to accelerating. The multiplier measures each resource over a predefined period, just as the traditional paradigm. According to the literature, a number of multiplier algorithms, including those for biomedical applications based on the Yavadunam Sutra, Nikhilam Sutram, and Urdva Tiryakabhyam Sutra, have been constructed utilizing various sutras [4, 16, 17].

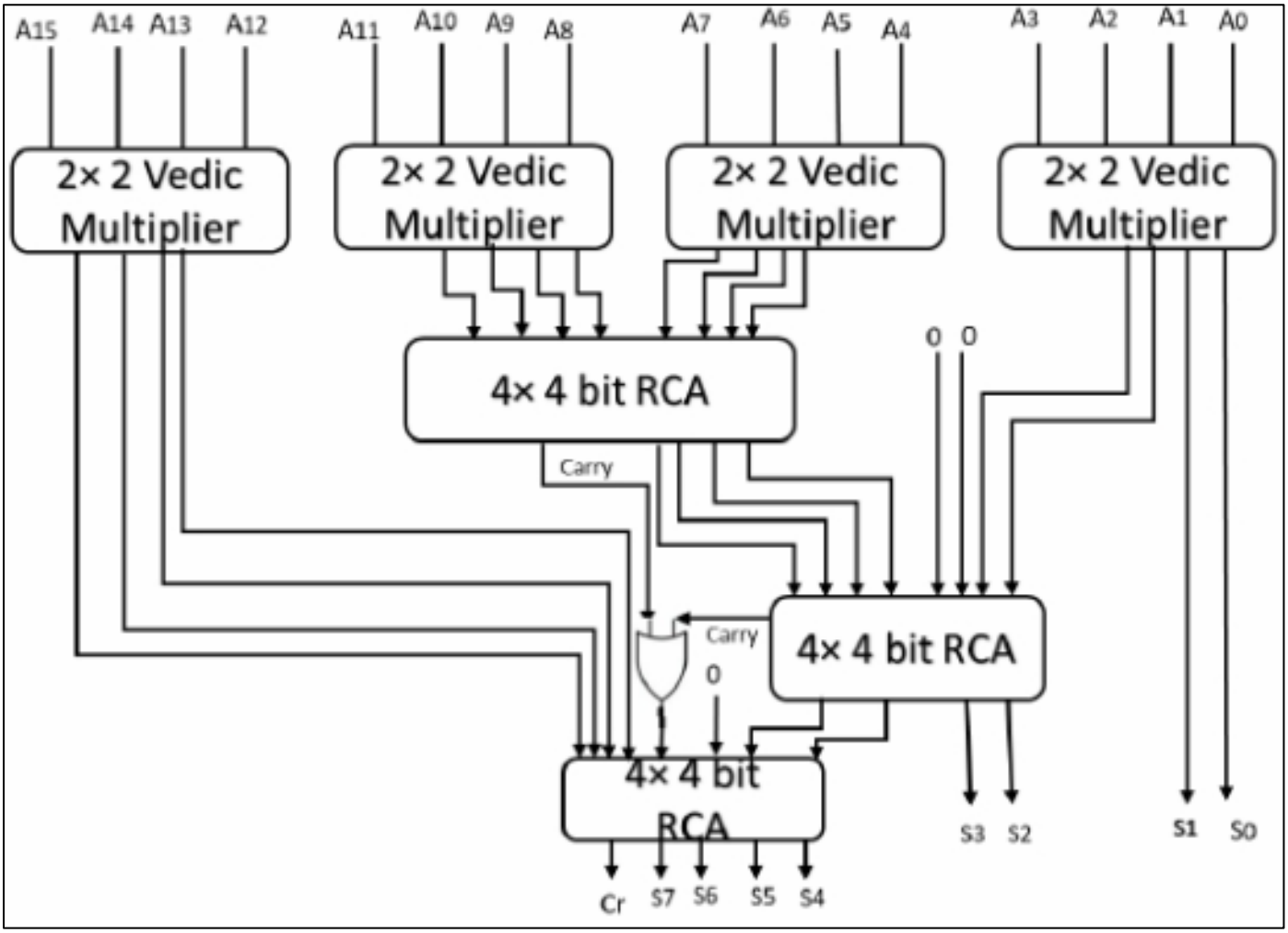

Fig 1 4x4 Binary Multiplication

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24MAR1218

III. EXECUTION OF VEDIC SUTRAS IN BIOMEDICAL SIGNAL PROCESSING APPLICATION

➢ *In this Section, the basic Sutras which are Frequently used to Implement DSP Applications will be Discussed.*

- *Urdhava Tiryakbhyam*

Urdhava Tiryakbhyam's unique concept lies in its ability to generate all partial products simultaneously. Fig. 1 illustrates this method as a 4x4 binary multiplication. Small units of 2x2 Vedic multipliers that compute in parallel have developed this multiplier [2].

Furthermore, the generalised approach can be used to perform any N × N bit multiplication. Since the partial products and their sums are calculated concurrently, the processor's clock frequency has no bearing on this. In general, this is good because it reduces the need for microprocessors to operate at increasingly greater clock speeds. The number of switching instances and the frequency of a processor's operation are positively connected. This raises the device's operating temperature via increasing power consumption and heat dissipation. Another advantage is that it can be expanded. Increasing the input and output data bus widths would not do anything more than boost processing power because of its regular nature. Because of its uniform structure, it can be easily arranged and uses the least amount of space in a silicon chip. The gate delay and area increase very slowly with increasing input bit count, in contrast to other multipliers. The Urdhava Tiryakbhyam multiplier consequently consumes less energy, time, and space.

- *Nikhilam Sutram*

Nikhilam Sutra for multiplication can be applied to complete addition, shift operations, and two-to three- digit multiplication with only one multiplication. For example, 106 * 108 Using an integer base difference for multiplication Factor of 106 multiplied by 100 (100-106) equals 6 and 108 (100-108). It comes out to 11448. (108-(-6)) = 114 (-6)*(-8) = 48 or 11448. Multiplication is required for 4 steps in the Karatsuba algorithm, whereas in the classic technique, it is required for 9 steps. The fundamental concept of the Nikhilam Sutra is as follows: m*n= (x+a)*(x+b)=x(x+a+b) + ab if n=x+b, m=x+a is the multiplicand, and x is the closest base.

- *Yavadunam Sutra*

This means that one can "write the square of the deficiency and determine the deficiency, lessen the deficiency from that number" [4], using the Yavadunam sutra to square a number. Yavadunam Tavadunikrtya Vargancha Yojayet (YTVY) is the up-sutra of the Yavadunam sutra. One distinctive criterion of this formula is that it may only be applied to the square of any integer that is closer to the bases of powers of ten, i.e., 10, 100, 1000, 1000,...These procedures can be used to find the square of an integer using the Yavadunam sutra of Vedic mathematics. Step 1: Use the closest base to identify the deficit. Step 2: Place the shortfall on the right side and square it. Step 3: Increase or decrease the amount by the deficiency. Step 4: The outcome is equal to [|Number - Deficiency|+ carry over] & [Deficiency Square]. The deficit is the difference between the base and the input that has to be squared. "10" is the nearest base of powers of 10 to the number "9." 10-9 = 1 is the current deficit of 1. The number 996's nearest base of powers of ten is 1000. 996's current deficit is 1000 -996 = 4. This sutra, however, is only effective when the number that has to be squared is nearer a power of 10. Moreover, there is not a traditional architecture for the Yavadunam sutra at the moment. It is challenging to develop a specific architecture because there are many different sources of information.

IV. PERFORMANCE ANALYSIS

According to research conducted in the past ten years, Vedic multipliers have enhanced traditional DSP applica- tion designs. It is stated in [19] that vedic multipliers are used in the design and implementation of FIR and IIR filters of different orders. Moreover, the noisy ECG signals are denoised using these filters. In terms of hardware and power consumption, the digital filters with vedic multiplier results perform better than the conventional filters. In a different study, Kerur et al. found that an 8-bit vedic multiplier outperforms an array multiplier by a factor of 24% and outperforms a booth multiplier by about 18.2% in terms of gate latency [20]. According to [1], DSP processors that use Vedic multipliers are also quite efficient in terms of speed. Its homogeneous and parallel nature facilitates its easy silicon realisation as well. According to Deepa et al., the Yavadunam vedic multiplier performs better in terms of the area delay product than the Array multiplier by 56.88%, the Braun multiplier by 39.01%, the Shift and Add multiplier by 91.46%, the Wallace multiplier by 31.17%, the Dadda multiplier by 13.46%, the Urdhava multiplier by 65.33%, and the Nikilam multiplier by 23.57% [4]. As we know that multiple order notch and peak filters play an important role in denoising of ECG and EEG signals. Meenakshi et al. presented vedic notch and peak filters (VNPF) in another study, and they are contrasted with the filters that are currently in use. In comparison to conventional filters, the suggested designs require less power and occupy less hardware [21]. According to the aforementioned research studies, vedic sutra-implemented multipliers out-perform conventional multipliers in terms of performance. Vedic multipliers also enhance the total hardware implementation in terms of speed, size, and power consumption in any DSP application.

V. CONCLUSION

Vedic mathematics contains a notion of symmetric computation. It covers a wide range of mathematical topics, such as calculus, geometry, trigonometry, and basic arithmetic. All of these methods are very efficient when it comes to manual computations. In terms of speed, the Vedic multiplier that is suggested works pretty well. Its homogeneous and parallel nature facilitates its easy silicon realisation as well. The main advantage is that the delay increases progressively as the number of input bits increases. Therefore, the basic unit for multipliers are implemented using Vedic Sutras and included to carry biomedical signals.

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24MAR1218

Additionally, significant improvement was observed in hardware implementation in terms of area, power dissipation and speed.

REFERENCES

[1]. Pushpangadan, R., Sukumaran, V., Innocent, R., Sasikumar, D., & Sundar, V. (2009). High speed vedic multiplier for digital signal processors. IETE journal of research, 55(6), 282-286.

[2]. Kant, A., & Sharma, S. (2015, September). Applications of Vedic multiplier designs-a review. In 2015 4th International Conference on Reliability, Infocom Technologies and Optimization (ICRITO)(Trends and Future Directions) (pp. 1-6). IEEE.

[3]. Pavithara, P., Devi, P. N., Pavithra, M., Dharani, L. R., Akshaya, M., Deepthi, S. (2023, December). VLSI implementation of vedic multiplier and carry look ahead adder based FIR filter for denoising EEG signal. In AIP Conference Proceedings (Vol. 2901, No. 1). AIP Publishing.

[4]. Deepa, A., & Marimuthu, C. N. (2019). Design of a high speed Vedic multiplier and square architecture based on Yavadunam Sutra. S¯adhan¯a 44(9), 197. a,

[5]. Padmavathy, T. V., Saravanan, S., Vimalkumar, M. N. (2020). Partial product addition in Vedic design-ripple carry adder design fir filter architecture for electro cardiogram (ECG) signal de-noising application. Microprocessors and Microsystems, 76, 103113.

[6]. Murugesh, M. B., Nagaraj, S., Jayasree, J., & Reddy, G. V. K. (2020, July). Modified high speed 32-bit Vedic multiplier design and implementation. In 2020 International Conference on Electronics and Sustainable Communication Systems (ICESC) (pp. 929-932). IEEE.

[7]. Shoba, M., & Nakkeeran, R. (2017). Energy and area efficient hierarchy multiplier architecture based on Vedic mathematics and GDI logic. Engineering Science and Technology, an International Journal, 20(1), 321-331.

[8]. Suryawanshi, J., Gawade, D., Tank, N., Worlikar, S., & Sahu, S. (2022, December). Vedic Multiplier Using Carry look ahead adder. In 2022 5th International Conference on Advances in Science and Technology (ICAST) (pp. 626-631). IEEE.

[9]. Dinesh, B., Venkateshwaran, V., Kavinmalar, P., & Kathirvelu, M. (2014, March). Comparison of regular and tree based multiplier architectures with modified booth encoding for 4 bits on layout level using 45nm technology. In 2014 international conference on Green Computing Communication and electrical engineering (ICGCCEE) (pp. 1-6). IEEE.

[10]. Thomas, A., Jacob, A., Shibu, S., & Sudhakaran, S. (2016). Comparison of Vedic Multiplier with Conventional Array and Wallace Tree Multiplier. International Journal of VLSI System Design and Communication Systems, 4(04), 244-248.

[11]. Kalaiselvi, C. M., & Sabeenian, R. S. (2024). Design of area-speed efficient Anurupyena Vedic multiplier for deep learning applications. Analog Integrated Circuits and Signal Processing, 1-13.

[12]. Kiran Kumar, V. G., & Shantharama Rai, C. (2021). Efficient implementation of cryptographic arithmetic primitives using reversible logic and Vedic mathematics. Journal of The Institution of Engineers (India): Series B, 102(1), 59-74.

[13]. Pasuluri, B. S., & Sonti, V. K. (2021, May). Design of Vedic multiplierbased FIR filter for signal processing applications. In Journal of Physics: Conference Series (Vol. 1921, No. 1, p. 012047). IOP Publishing.

[14]. Naik, R. N., Reddy, P. S. N., & Mohan, K. M. (2013). Design of vedic multiplier for digital signal processing applications. International Journal of Engineering Trends and Technology, 4(7).

[15]. Saxena, M. C., Upadhyaya, M. V., Gupta, H. K., & Sharma, A. (2018, October). Denoising of ECG signals using FIR & IIR filter: A performance analysis. In Proceedings on International Conference on Emerg (Vol. 2, pp. 51-58).

[16]. Madan, P., Singh, V., Singh, D. P., Diwakar, M., & Kishor, A. (2022). Denoising of ECG signals using weighted stationary wavelet total variation. Biomedical Signal Processing and Control, 73, 103478.

[17]. Pasuluri, B. S., & Sonti, V. K. (2022). Design of high-performance GDI logic based 8-tap FIR filter at 45nm CMOS technology using Nikhilam Multiplier. International Journal of Intelligent Systems and Applications in Engineering, 10(3), 340-346.

[18]. Khubnani, R., Sharma, T., & Subramanyam, C. (2022, March). Applications of Vedic multiplier-A Review. In Journal of Physics: Conference Series (Vol. 2225, No. 1, p. 012003). IOP Publishing.

[19]. Kumar, M. Design and Implementation of Digital Low Pass FIR and IIR Filters Using VHDL for ECG Denoising. International Journal of Engineering Trends and Technology, Volume 72 Issue 1, 252-265, January 2024.

[20]. Kerur, S. S., Prakash Narchi, J. C., Kittur, H. M., & Girish, V. A. (2011). Implementation of Vedic multiplier for digital signal processing. In International Conference on VLSI, Communication & Instrumentation (ICVCI) (pp. 1-6).

[21]. Agarwal, M., & Garg, M. (2022). Design and FPGA implementation of vedic notch and peak filters. In IOT with Smart Systems: Proceedings of ICTIS 2021, Volume 2 (pp. 255-267). Springer Singapore.