Volume 9, Issue 9, September– 2024 International Journal of Innovative Science and Research Technology
ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24SEP1230

Addressing Power Efficiency and Stability in SRAM: A 4x4 Cell Array Design with Enhanced Power Gating

[1]Santosh Krishnakant Rai; [2]Chandrahas Sahu
[1]M. Tech Student, Department of Electronics and Telecommunication Engineering
Shri Shankaracharya Technical Campus, Bhilai, Durg, Chhattisgarh, India.
[2]Sr. Assistant Professor (H.o.D) (E&I), Department of Electronics and Telecommunication Engineering
Shri Shankaracharya Technical Campus, Bhilai, Durg, Chhattisgarh, India.

Abstract:- In order to lower power consumption and leakage currents during active operation, the suggested SRAM architecture with power gating design trims the source voltage across the SRAM cell, ranging from 50 to 150 mV. Power gating based on sectors is utilized, using a self-biasing approach where the gate terminal and source of a PMOS transistor act as a diode, controlling the virtual ground. However, three challenges arise with this method in nanometer technology: the additional self-biasing transistor (SBT) occupies 5% more space, the source voltage adjustment mechanisms are not effectively implemented, and the increase in virtual ground voltage leads to bias temperature instability. To implement this design, a 4x4 SRAM cell array is constructed, consisting of 4 rows and 4 columns of 10T SRAM cells. A decoder addresses these cells, and each row represents half a byte, with control circuitry managing input and output data. Additionally, the outputs of individual cells in each column are combined using a 4-bit OR, producing a single data output point. This architecture effectively reduces power consumption while maintaining operational efficiency, making it suitable for nanometer-scale SRAM designs.

Keywords:- *Schmitt Trigger Inverter, Stacked Transistor, SRAM and Power Gating.*

I. INTRODUCTION

Bio implants, cell devices, self-powered wireless sensors, and electricity-harvesting structures are cutting-edge examples of system-on-chips (SoCs). As these SoCs depend upon constrained energy from batteries or other sources, minimizing strength intake has become a vital element of SoC design. One of the important thing strategies to lessen the general strength utilization of SoCs is reducing the electricity consumption of large static random-get admission to reminiscence (SRAM) components [1]. Reducing the supply voltage (VDD) is an effective method for cutting strength and power intake since strength reduces quadratically with lower VDD stages [2]. However, decreasing VDD additionally will increase delays and soft errors quotes (SERs).

When VDD falls beneath the sub-threshold voltage (Vth), there's an exponential rise in put off, main to seriously [3] better static strength intake. This shows that even at extraordinarily low energy ranges, a few powers consumption persists. When VDD is barely above Vth, running inside the close to-Vth place improves latency extensively whilst providing terrific power financial savings in comparison to high-quality-Vth operation and better performance than sub-Vth operation. Therefore, optimizing energy and postpone in the near-Vth location can correctly reduce normal electricity intake whilst maintaining efficiency.

[4] Operating close to the edge voltage (Vth) introduces demanding situations due to smooth errors because of α-particles. [5] The decrease crucial fee on this mode of operation increases the tender error rate (SER). In non-bit-interleaved systems, where words are stored consecutively, a unmarried phrase can suffer a couple of bit mistakes considering gentle errors often have an effect on cells which might be bodily adjoining. This can bring about a couple of simultaneous bit mistakes within the same word. Error correction code (ECC) circuits capable of coping with multi-bit errors correction tend to be huge and consume large energy. However, the bit-interleaving agency helps to mitigate these results [6].

Transistor current shows tremendous fluctuation near the threshold voltage (Vth), and to attain excessive density in restricted area, small transistors are designed to be prone to Vth versions. Traditional 6T SRAM cells frequently compromise write capability to enhance examine stability, making it difficult to stability each. In the close to destiny, changed SRAM cells are expected to offer more advantageous write and examine stability, addressing Vth-associated challenges [five, [7]– [11]. However, modern-day SRAM cells face issues together with the need for write-lower back gadgets in bit-interleaving structures, larger cellular sizes, and excessive power consumption. The Schmitt-trigger-based 9T (ST 9T) SRAM cell addresses those limitations, supplying advanced write and read balance near Vth whilst using less electricity and reducing cell length. This design carries 3 key capabilities: unmarried bit-line (BL) structures that limit electricity consumption and decrease area necessities.

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24SEP1230

II. LITERATURE SURVEY

[12] The LP10T SRAM cell is designed for low standby power while offering high static noise margins. It features a single-ended architecture, distinct bit lines for reading and writing, improved read stability, and better write performance with minimized leakage power. Recent research by Springer delves into advancements in memory technologies, focusing on design principles, architectural frameworks, and practical applications. The research provides valuable insights into emerging innovations such as non-volatile memory and resistive RAM, and evaluates their potential future influence on computing technology.

[13] The cited research provides important perspectives on cutting-edge SRAM cell designs and semiconductor advancements. One investigation examines an SRAM [14] design that reduces disturbances through innovations like adjustable read operation timing and a data-sensitive write word-line configuration. Another study presents SRAM cells that employ power-gating strategies to enhance energy efficiency, responding to the demand for more sustainable solutions in contemporary electronic systems.

The BSIM-CMG 107.0.0 Multi-Gate MOSFET Compact Model offers an in-depth framework for simulating multi-gate MOSFETs, essential for precise semiconductor device design and simulation. Recent advancements in CMOS technology, such as fully-depleted tri-gate transistors and high-density MIM capacitors, are discussed, emphasizing their role in enhancing performance and power efficiency [15][16]. These developments underscore the ongoing evolution in semiconductor technology and SRAM design. Notable studies include an analysis of channel doping effects on FinFETs for 22 nm technology and beyond, which affects device performance and scalability [18]. Other research investigates large-scale SRAM variability in 45 nm CMOS technology, identifying key factors impacting SRAM reliability and performance. Additionally, a paper explores both static and dynamic write margins in nanometer SRAMs, detailing factors that influence SRAM write stability [19][20]. Techniques for controlling SRAM cell leakage in ultra-low-power applications are also examined, focusing on methods to minimize leakage for energy-efficient designs. Lastly, research on NC-SRAM introduces a low-leakage memory circuit tailored for ultra-deep submicron processes, aimed at reducing leakage currents and boosting memory efficiency [21]. These studies collectively highlight the significant progress and ongoing challenges in SRAM technology and semiconductor design.

III. METHODOLOGY

Trimming the supply voltage throughout the SRAM cellular, which tiers from 50 to a hundred and fifty mV, may be executed in severa ways the usage of this approach. The decreasing of leakage present day all through SRAM's lively mode is viable way to a technique called area-primarily based energy gating. By becoming a member of the gate terminal and supply of the PMOS transistor, it features as a diode. This mechanism, which governs the virtual floor, is referred to as the self-biasing approach.

Three issues, though, plague the self-biasing method employed in nanometer technology. In the first place, an extra self-biasing transistor (SBT) needs about 5% more space. Secondly, the mechanisms for the adjusted source voltage are not carried out correctly by these techniques. The third foremost impact of raising the virtual floor voltage is tremendous or bad bias temperature instability.

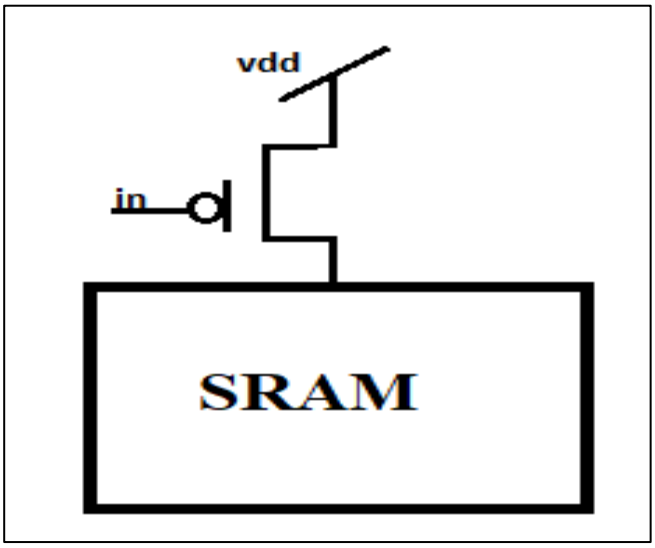

Fig 1 Block Diagram of Power Gating

4 rows and 3 columns of SRAM cell arrays are designed as described in this section. An array's 10T SRAM cells make up each block. A 4x4 SRAM cell array is made up of 4 rows and 4 columns in arrangement. Before arranging the array, the decoder is utilized to address these rows of cells. The row makes up half a byte because it has four cells. The side from which the address lines are generated. Write and ready circuitry allows for the control of input and output data. The output of each column's single SRAM cell can also be combined using a 4-bit OR to create a single output data point.

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24SEP1230

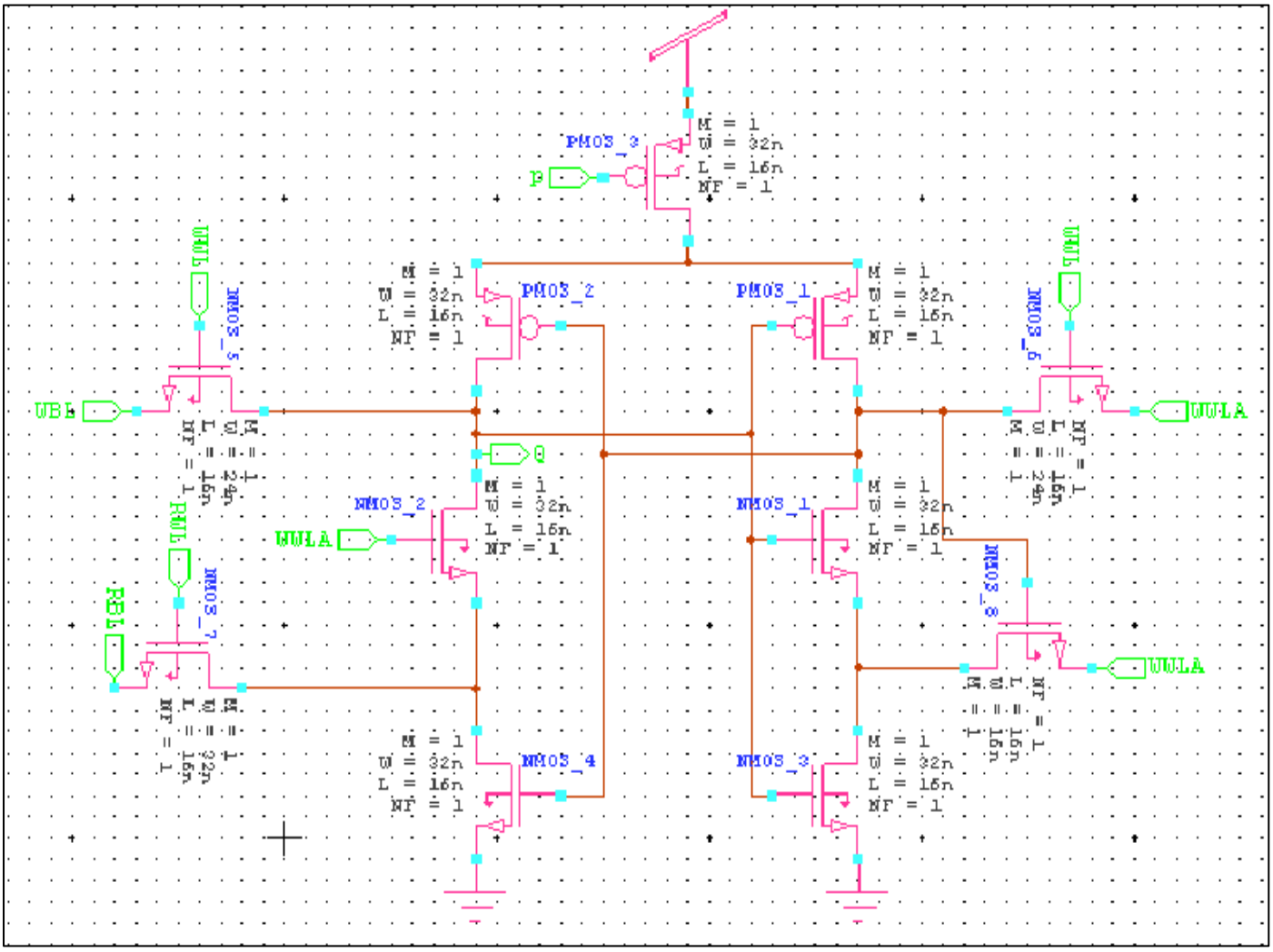

Fig 2 Modified SRAM using Power gating Technique.

The changed 10T SRAM 4x4 array is designed the use of the changed 10T SRAM cells in conjunction with the decoder circuit. Contains sixteen 10T SRAM cells as a traditional array. The sixteen blocks representing the 4x4 matrix is created the usage of the 10T SRAM cells. The 10T SRAM mobile circuit is used to create a symbol and its miles added directly to the array as shown in the parent.

The 2:4 decoder circuit is to call cope with lines i.e., to pick out a positive array row. There are 4-bit strains which can be to cope with the array column smart and 4 outputs from the array. I0 and I1 are the inputs of decoder. I0 and I1 values can be given according to the fact table of the decoder. The output made out of decoder helps to deal with the row sensible cellular and the value from the bit line helps to deal with column wise. With the help of each input, it'll be able to identify an appropriate cell and get the output consistent with it. Y0, Y1, Y2 and Y3 are outputs from the decoder. According to each input an identical row will be chosen. For instance, if enter is 00, the primary row Y0 might be selected. For input 01 the 2nd row Y1, for 10 as enter the 0.33 row Y2 and ultimately for eleven as enter the remaining row Y4 may be chosen. A0, A1, A2 and A3 are the outputs of the array which is chosen in step with the row selected by way of the decoder.

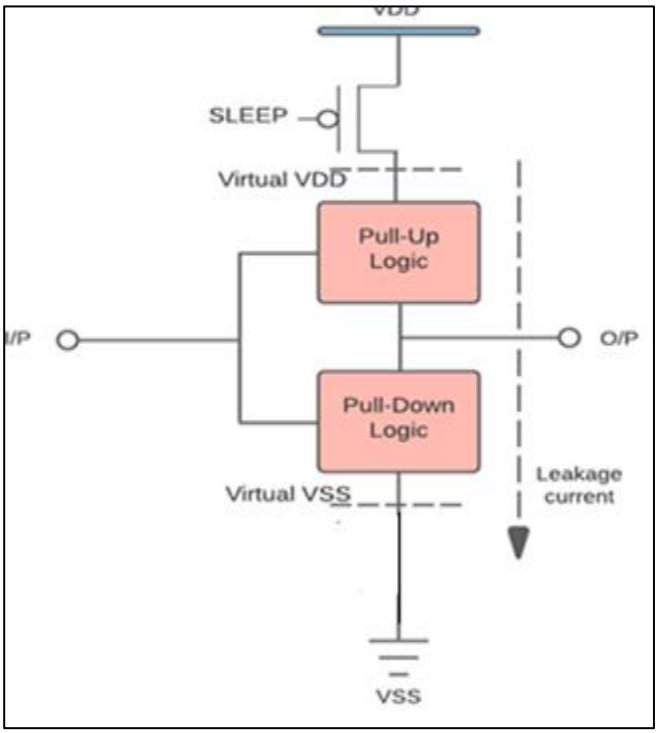

Fig 3 Block Diagram of Power gating Technique

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24SEP1230

Power gating is a method hired in incorporated circuits to lower energy intake by using slicing off the power deliver to certain circuit blocks while they may be now not in use. This approach is especially beneficial in contemporary chips, which typically include numerous functional blocks that may not be active continuously.

Power gating involves integrating switches into the electricity supply traces of unique circuit blocks, managed by means of an energy management unit. These switches can reduce off strength whilst a block is not in use, thereby reducing strength intake. This technique is frequently mixed with different electricity management methods, like dynamic voltage and frequency scaling, to further beautify power financial savings. However, energy gating can gift layout challenges, consisting of improved complexity and capacity timing issues during electricity state transitions. Despite these hurdles, strength gating stays a fantastically effective technique for minimizing strength use in modern electronics, together with smartphones, laptops, and different portable gadgets.

Power gating is a low strength approach used for lowering electricity consumption, particularly specializing in static strength reduction. Here are the key factors approximately energy gating:

➢ *Definition and Purpose*

Power gating is a way used to lessen ASIC and SoC strength intake with the aid of turning off elements of the design that aren't getting used or in inactive mode three. It is especially powerful at decreasing leakage electricity in modern-day technology nodes where subthreshold leakage energy has come to be comparable to dynamic electricity dissipation 3.

➢ *How Power Gating Works*

Power gating works by disconnecting the power supply to inactive blocks of logic 1. This effectively shuts off the power completely for these blocks, resulting in both static and dynamic savings for the time that the block is turned off 1.

The technique uses power switches to control the flow of current between the power domain and ground 1. These switches can be controlled by software, hardware timers, or dedicated power gating controllers 3.

IV. RESULTS

The above diagram is the schematic of the proposed SRAM with power gating the inputs we are going to assign the directly to the 10 t SRAM & output of every SRAM circuit is taking parallelly then connecting into the or gate 4x4 SRAM array technique we used here, so output we are going to take at the parallelly. & the final output will be taking from the or gates as q1, q2q3& q4.

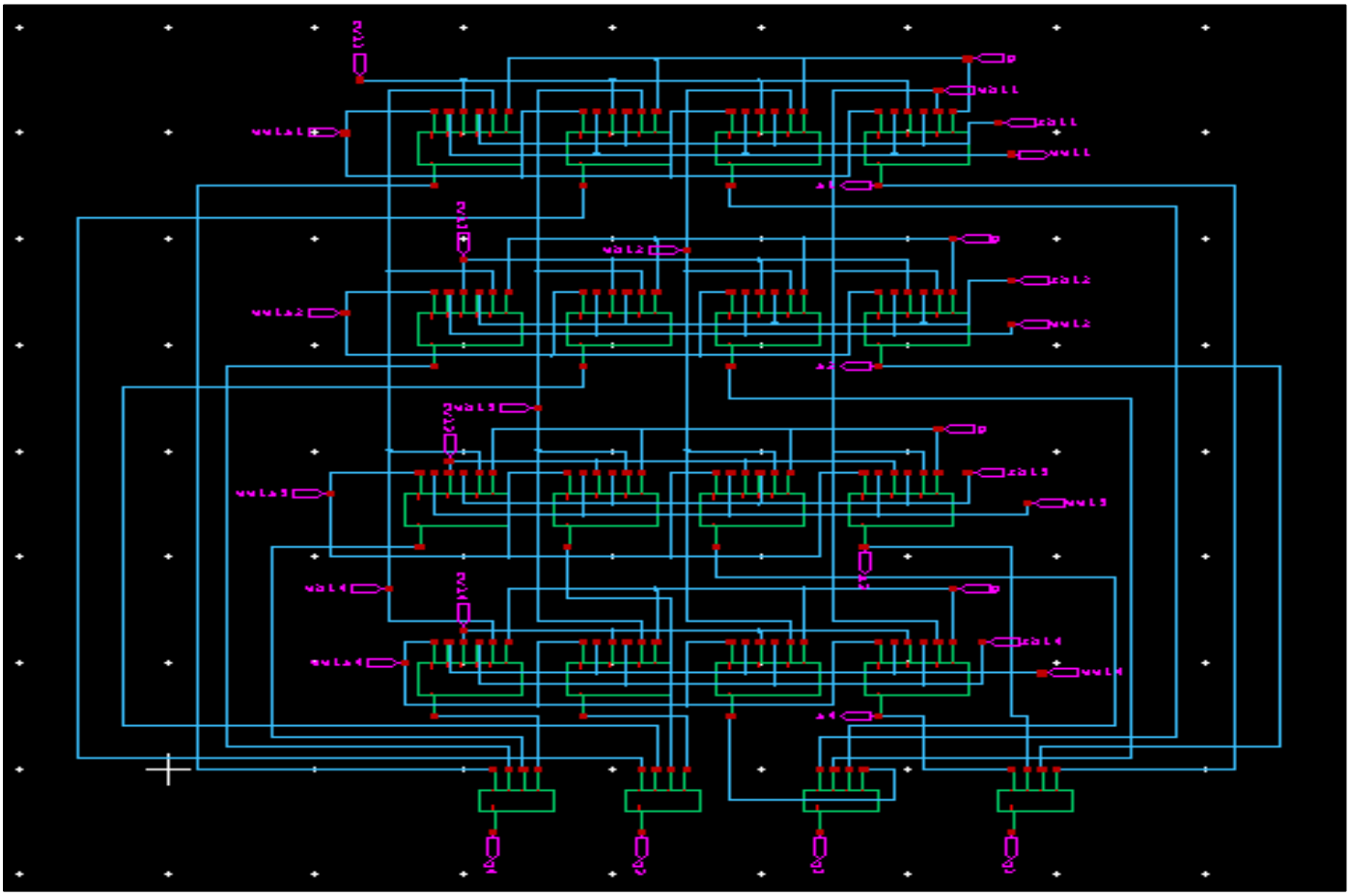

Fig 4 Schematic of Proposed 4x4 Array SRAM with Power gating

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24SEP1230

➢ *Parameters:*

```
Device and node counts:
        MOSFETs - 216
```

Fig 5 Mos Count

```
Average power consumed -> 6.305397e-006 watts
Max power 3.247933e-005 at time 2.09013e-008
Min power 8.380930e-008 at time 2.025e-008
```

Fig 6 Power

```
delay = 1.0078e-008
   Trigger = 1.0500e-008
   Target  = 2.0578e-008
```

Fig 7 Delay

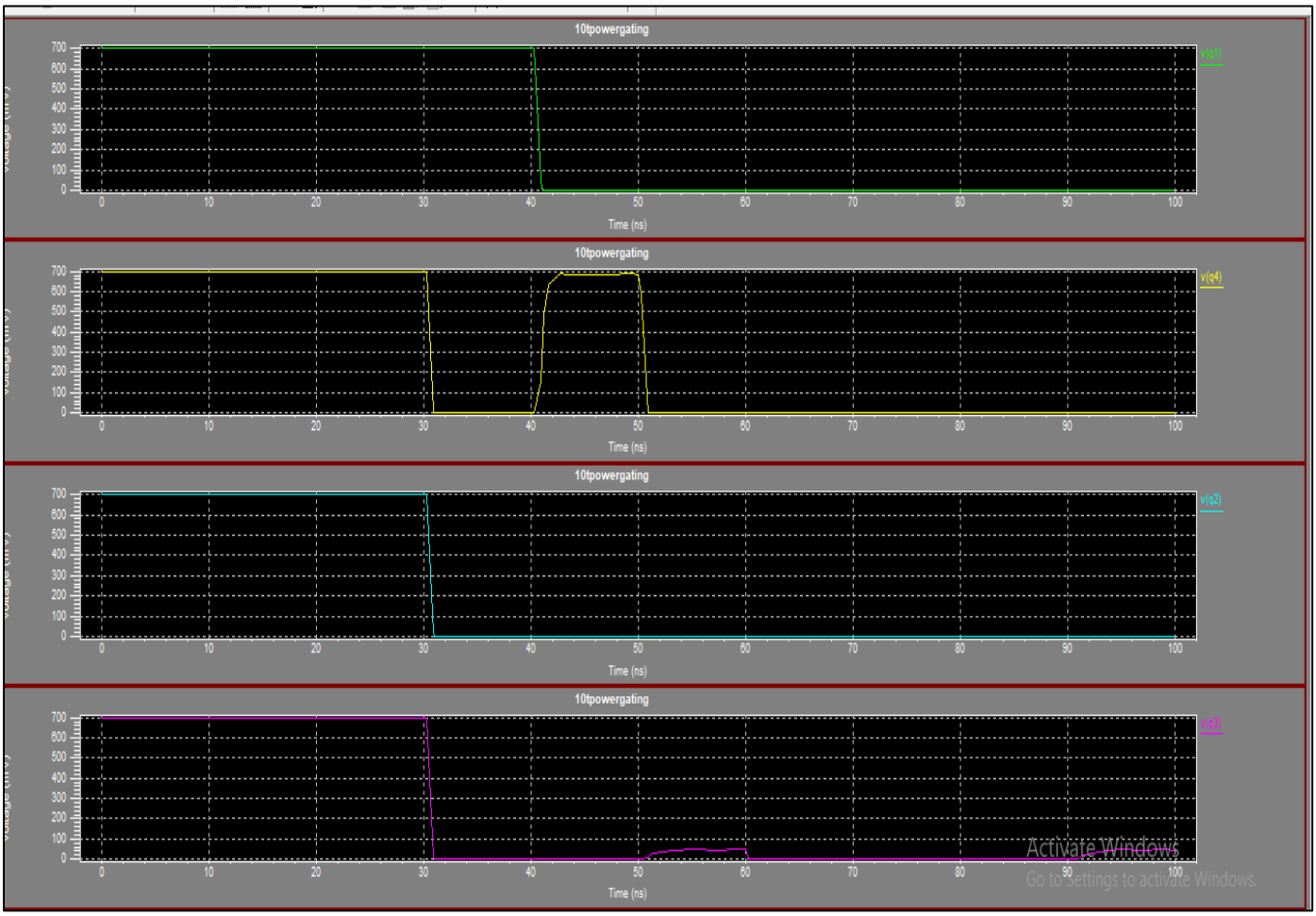

Fig 8 Output waveforms of 4x4 Array SRAM with Power gating

From above, represents the output wave form of 10t SRAM for the power gating, here we are going to take direct q outputs, based on that this is the final output wave from of the power gating technology after using.

Consequently, when we compare all of the strategies we used, we can therefore draw conclusions about the area, power, and delay output characteristics that need to be taken into account, as well as a comparison of those techniques that will yield good performance, the power consumption which is less & the delay how much delay contains each technique. we can compare here Coming to the energy parameter which is going to be fundamental factor of the circuit layout how plenty circuit layout is going to be considering the strength fee the which method goes devour less power we are able to examine here as proven below from this we can finish that which design is going match for extra packages.

Table 1 Power, Delay & Mos count Comparision

	Mos Count	**Power**	**Delay**
10T SRAM(4x4)	200	7.8×10^{-6}	3.08×10^{-8}
POWER GATING	216	6.305 x 10-6	3.01 x 10-8

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24SEP1230

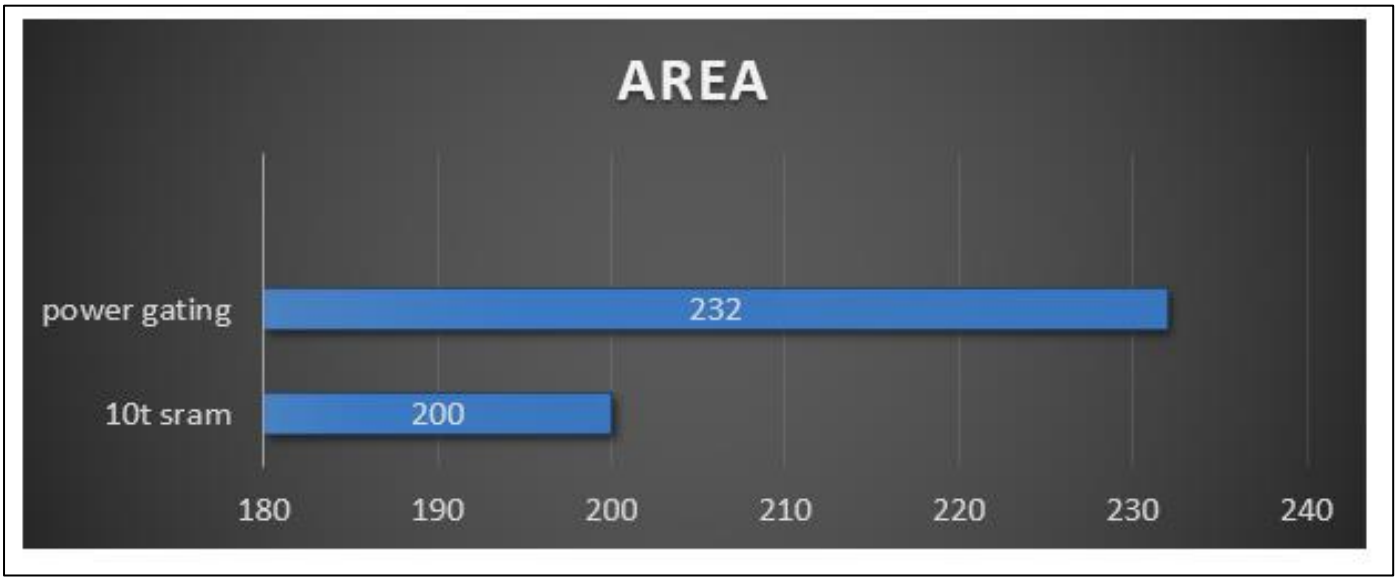

Fig 8 Comparison of Area

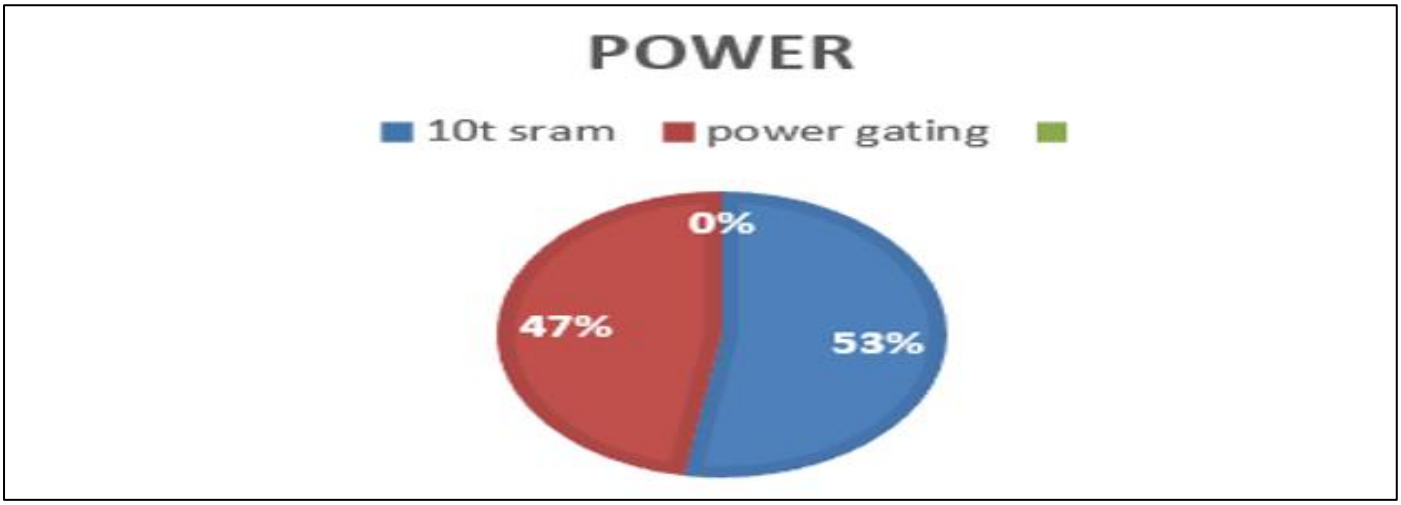

Fig 9 Comparison of Power

So here the last parameter we are going to compare delay so the output and input value should be going compare here base don that the how much delay is going we can measure the below figure shows the delay of each technique.

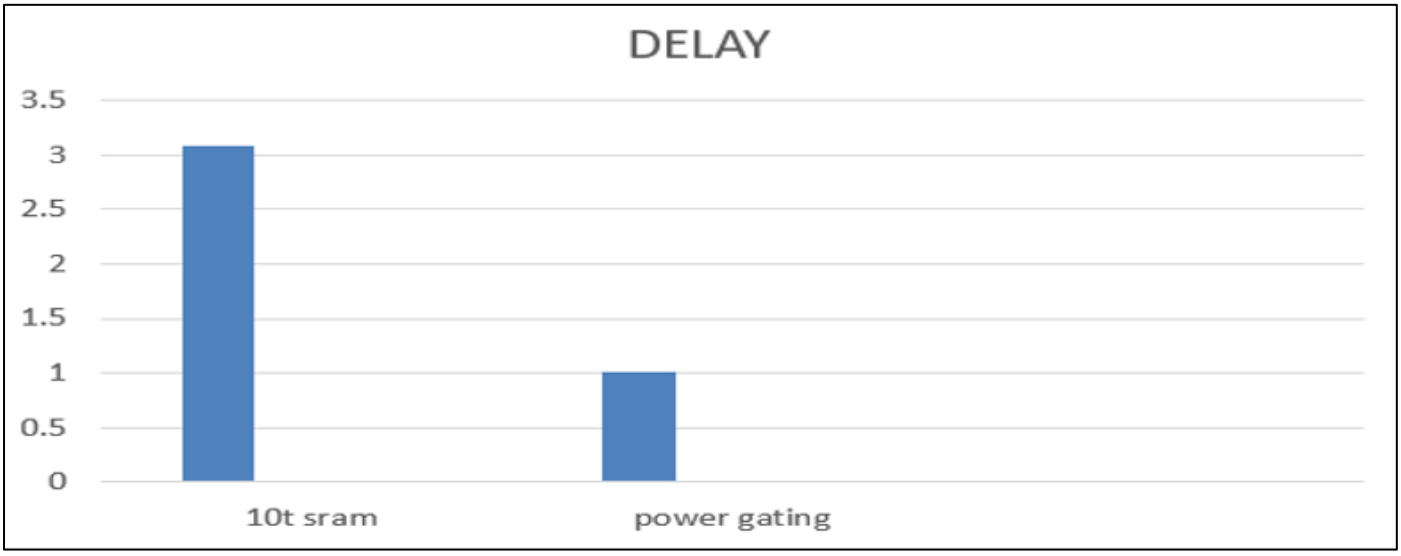

Fig 10 Comparison of Delay

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/IJISRT24SEP1230

V. CONCLUSION

In end, the proposed 4x4 Array SRAM architecture with power gating design offers a giant discount in strength consumption and leakage currents by using trimming the source voltage throughout the cells. The sector-based electricity gating and self-biasing approach, at the same time as effective, presents demanding situations consisting of extended area requirements, incomplete source voltage modifications, and bias temperature instability. Despite those limitations, the 4x4 SRAM cellular array, with its green decoder and output circuitry, keeps operational performance and is nicely-suitable for nanometer-scale applications. This design moves a balance among strength performance and overall performance, addressing critical desires in superior SRAM technologies.

REFERENCES

[1]. C. B. H. and C. A P, "Static noise margin variation for sub-threshold SRAM in 65-nm CMOS," 2006.
[2]. D. R. G, W. M. , B. D. , S. D. and M. T. , "Near-Threshold Computing: Reclaiming Moore's Law Through Energy Efficient Integrated Circuits," roceedings of the IEEE, vol. 98, pp. 253-266, Feb 2010.
[3]. C. B. H, R. J. F, K. S. , P. M. and L. J. , "Flexible Circuits and Architectures for Ultralow Power," roceedings of the IEEE, vol. 98, pp. 267-282, 2010.
[4]. B. R. C, "Radiation-induced soft errors in advanced semiconductor technologies," IEEE Transactions on Device and Materials Reliability, vol. 5, pp. 305-316, Sept 2005.
[5]. C. M. -H. , C. Y. -T. and H. W. , "Design and Iso-Area Vmin Analysis of 9T Subthreshold SRAM With Bit-Interleaving Scheme in 65-nm CMOS," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 59, pp. 429-433, July 2012.
[6]. P. Hazucha, "Neutron soft error rate measurements in a 90-nm CMOS process and scaling trends in SRAM from 0.25-mm to 90-nm generation," IEDM Tech, p. 21.5.1–21.5.4, 2003.
[7]. C. I. J. , . K. J. -J. , P. S. P. and R. K. , "A 32 kb 10T Sub-Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS," IEEE Journal of Solid-State Circuits, vol. 44, pp. 650-658, Feb 2009.
[8]. L. C. e. al, "An 8T-SRAM for Variability Tolerance and Low-Voltage Operation in High-Performance Caches," IEEE Journal of Solid-State Circuits, vol. 43, pp. 956-963, 2008.
[9]. P. G. and F. S. M. , "A 256-kb 9T Near-Threshold SRAM With 1k Cells per Bitline and Enhanced Write and Read Operations," IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, vol. 23, pp. 2438-2446, Nov 2015.
[10]. K. J. P. , K. K. and R. K. , "A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM," in IEEE Journal of Solid-State Circuits, vol. 42, pp. 2303-2313, Oct 2017.
[11]. A. S. , G. M. K. , A. N. and H. M. , "Single-ended Schmitt-trigger-based robust low-power SRAM cell," IEEE Trans. Very Large Scale Integr. (VLSI) Syst, p. 2634–2642, Aug 2016.
[12]. Y. Lie, "Emerging Memory Technologies: Design, Architecture, and Applications," p. 187, Oct 2013.
[13]. M.-H. Tu, "A single-ended disturb-free 9t subthreshold SRAM with cross-point data-aware write word-line structure, negative bit-line, and adaptive read operation timing tracing," IEEE J. Solid-State Circuits, vol. 47, p. 1469–1482, Jun 2012.
[14]. O. T. W. , J. H. , K. K. , P. J. , Y. Y. and J. S.-O. , "Power-gated 9T SRAM cell for low-energy operation," IEEE Trans. Very Large Scale Integr. (VLSI) Syst, vol. 25, p. 1183–1187, Mar 2017.
[15]. B.-C. 107.0.0, "Multi-Gate MOSFET Compact Model," 2013.
[16]. C. Auth , "A 22 nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors," self-aligned contacts and high density MIM capacitors, p. 131–132, 2012.
[17]. C.-H. Lin, "Channel doping impact on FinFETs for 22 nm and beyond," p. 15–16, Jun 2012.
[18]. G. Z. , C. A. , P. L.-T. , D. K. T. , L. T.-J.-K. and N. B. , "Large-scale SRAM variability characterization in 45 nm CMOS," IEEE J. Solid-State Circuits, vol. 44, p. 174–3192, Nov 2009.
[19]. W. J. , N. S. and C. B. H. , "Analyzing static and dynamic write margin for nanometer SRAMs," Low Power Electron. Design (ISLPED), p. 129–134, 2008.
[20]. Bikki and Karuppanan, "SRAM Cell Leakage Control Techniques for Ultra Low Power Application," Circuits and Systems,, 2017.
[21]. Sridhar, Narasimhan and Lakkumanan, "NC-SRAM—A Low-Leakage Memory Circuit for Ultra Deep Submicron Designs," IEEE International SoC Conference, 2003.