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Design of Low-Leakage SRAM Cells for Sub-10nm Technologies

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Abstract: In the era of aggressively scaled CMOS technologies, static random-access memory (SRAM) plays a critical role in determining the overall power and performance of modern integrated circuits. This paper presents a comprehensive design methodology for low-leakage SRAM cells targeted at sub-10nm technology nodes. We propose modifications to conventional 6T SRAM architecture and evaluate alternative topologies such as 8T and 10T cells for leakage reduction. Simulation results using predictive technology models (PTM) for 7nm FinFET demonstrate significant improvements in leakage current, noise margins, and cell stability under process, voltage, and temperature (PVT) variations. Additional analysis includes layout design considerations, temperature-dependent behavior, and scalability insights for advanced technology nodes.

Keywords: *SRAM, Sub-10nm, Low-Leakage, FinFET, PVT Variations, 6T Cell, 8T Cell, Stability, Layout Optimization*.

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I. INTRODUCTION

SRAM is widely used in cache memories, register files, and embedded memory blocks due to its high speed and compatibility with CMOS logic. As the industry transitions below 10nm technology nodes, SRAM design faces challenges including increased leakage current, reduced noise margins, and heightened susceptibility to variability. The growing use of SRAM in low-power mobile and AI applications has intensified the need for optimized designs that balance speed, stability, and power efficiency. This paper addresses these challenges by analyzing leakage mechanisms and proposing optimized SRAM cell designs

II. BACKGROUND AND RELATED WORK

Conventional 6T SRAM cells have been extensively used, but suffer from instability and leakage issues at scaled nodes. Prior research has explored multi-threshold CMOS (MTCMOS), dynamic voltage scaling (DVS), and novel transistor structures. FinFET technology offers enhanced electrostatic control and reduced short-channel effects, making it suitable for low-leakage designs. Several works have reported improved designs using assist circuitry, asymmetric sizing, and differential read/write paths. However, a detailed comparison in the context of FinFET-based nodes is still evolving.

III. DESIGN CHALLENGES AT SUB-10NM

A. Increased Leakage Current

Due to reduced channel lengths and higher subthreshold conduction, leakage becomes a significant portion of standby power.

B. Process Variability

Device mismatch between pull-up and pull-down transistors can cause read/write failures and metastability. Variability increases with device scaling and impacts both functional and parametric yield.

C. Reduced VDD Headroom

Lower supply voltages reduce noise margins and limit drive strengths, especially in low-power modes.

D. Access Device Weakening

Short-channel effects in access transistors degrade performance and reliability, especially under read-disturb conditions.

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IV. PROPOSED SRAM CELL DESIGNS

A. Improved 6T Cell with High-Vth Transistors

This approach utilizes high-threshold voltage transistors in the pull-up path to minimize off-state leakage. Asymmetric sizing improves read stability but introduces slight degradation in write access time. The layout remains compact, preserving high density.

B. 8T SRAM Cell with Buffered Read Path

The 8T cell decouples the read path from the storage node, enhancing read stability. The additional read buffer transistors eliminate the read-disturb effect and allow for better noise margins. Although the area is increased by ~30%, the cell is highly robust under PVT variations.

C. 10T SRAM with Write-Assist

The 10T design incorporates separate read and write ports and uses write-assist techniques such as boosted word-lines or dynamic ground biasing. These features improve write-ability in ultra-low voltage regimes. Write-boost techniques help overcome reduced drive strength, especially important in subthreshold or near-threshold operation.

V. SIMULATION SETUP AND RESULTS

A. Simulation Environment

Simulations were performed using HSPICE and 7nm PTM FinFET models. The SRAM cells were tested under a variety of corner conditions to evaluate leakage power, SNM (Static Noise Margin), RNM (Read Noise Margin), Write Margin, and Delay.

B. Metrics and Evaluation

Table 1 Metrics and Evaluation

Cell Type	Leakage Power (nW)	Read SNM (uV)	Write Margin (uV)
6T	45.2	120	110
Improved 6T	32.1	125	105
8T	18.7	190	100
10T	21.3	170	140

C. Temperature Dependence

Simulations across 25°C to 100°C show a non-linear increase in leakage power, with the 8T cell demonstrating the lowest sensitivity to temperature. This highlights its suitability for mobile and automotive applications.

D. Layout Considerations

Layout parasitics and spacing rules for FinFETs are accounted for using predictive layout estimation. The 10T cell requires more routing space due to assist circuitry, while the improved 6T cell retains high density. Future work includes DRC-clean layout implementation using tools like Cadence Virtuoso.

VI. DISCUSSION

The simulation results and architectural trade-offs reveal that the 8T and 10T designs offer a promising balance between leakage reduction and performance robustness. The 8T design, in particular, achieves superior read stability without significant write degradation. The 10T architecture, while more complex, supports aggressive voltage scaling with strong write margins. These trade-offs must be carefully evaluated for application-specific memory designs, particularly in AI accelerators, mobile SoCs, and wearables.

VII. SCALABILITY AND FUTURE WORK

As nodes shrink beyond 5nm, new challenges such as quantum tunneling and variability due to discrete dopants will require novel cell topologies and 3D integration techniques. Future work includes:

- Development of assist-circuit-aware placement algorithms.
- Integration with near-memory compute blocks.
- Application of machine learning to predict failure under PVT variations.

VIII. CONCLUSION

This work demonstrates that low-leakage SRAM design for sub-10nm nodes requires careful transistor sizing, cell architecture selection, and assist techniques. 8T and 10T designs, though more complex, offer substantial gains in leakage reduction and stability. These findings contribute to the development of energy-efficient memory subsystems in nanoscale CMOS technologies. Emphasis on temperature robustness and layout considerations makes the proposed solutions applicable to real-world silicon implementations.

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