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Power Comparison for Multi-Bridge-Channel FETs (MBCFETs) and Fin Field Effect Transistors (FinFETs) at 5nm Technology

Vandana Bogala[1]; A. Shravan Kumar[2]

[1]M. Tech Student, Department of Electronics and Communication Engineering, JNTUH University College of Engineering Science and Technology, Hyderabad, India
[2]Assistant Professor, Department of Electronics and Communication Engineering, JNTUH University College of Engineering Science and Technology, Hyderabad, India

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Abstract: This project compares Multi-Bridge Channel FET (MBCFET) and FinFET in a 5nm technology node in terms of their appropriateness for future semiconductor use. LTspice/CAD based proprietary MBCFET and FinFET equivalent models were created and simulated in an effort to compare key performance characteristics such as leakage current, dynamic power, and total power consumption. For additional verification of the simulated behaviour, MATLAB based machine learning methods were also utilized to compare the simulated I–V profiles with theoretical FinFET and MBCFET curves. This two-environment methodology— circuit-level simulation and data-driven verification is a sound foundation for device performance analysis, warranting the proposal of MBCFET as an energy-efficient in future semiconductor technology.

Keywords: *FinFET, MBCFET, LTSPICE, CAD, MATLAB, Power Consumption.*

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I. INTRODUCTION

In the realm of semiconductor scaling at the 5nm node and beyond, the major challenges occur due to short-channel effects and power leakage. This paper compares two advanced architectures, FinFET and MBCFET (a Gate-All-Around transistor), for performance evaluation in modern digital applications. Utilizing LTspice for preliminary device-level simulation, key metrics such as leakage current and dynamic power were analyzed. The study was extended to the circuit level using Cadence Virtuoso in designing and simulating a basic CMOS inverter application based on both the FinFET and MBCFET models. Therefore, critical figures of merit, such as voltage transfer characteristics, noise margins, and switching speed, can be compared in practice. From the combined LTspice and Cadence methodology, such an analysis leads to the conclusion that MBCFETs, with better gate control and low leakage, are a more promising candidate for future low-power and high-density integrated circuits

- *FinFET:*

FinFETs represent a three-dimensional, non-planar transistor that has enabled nanoelectronics scaling below the 22 nm node. The key feature of FinFETs is that the vertical, "fin"-shaped, channel is surrounded by the gate on multiple sides, providing better electrostatic control. This is a trade-off for the significant improvement in short-channel effects and leakage current compared to planar MOSFETs. FinFETs originated from double-gate concepts developed during the 1990s.

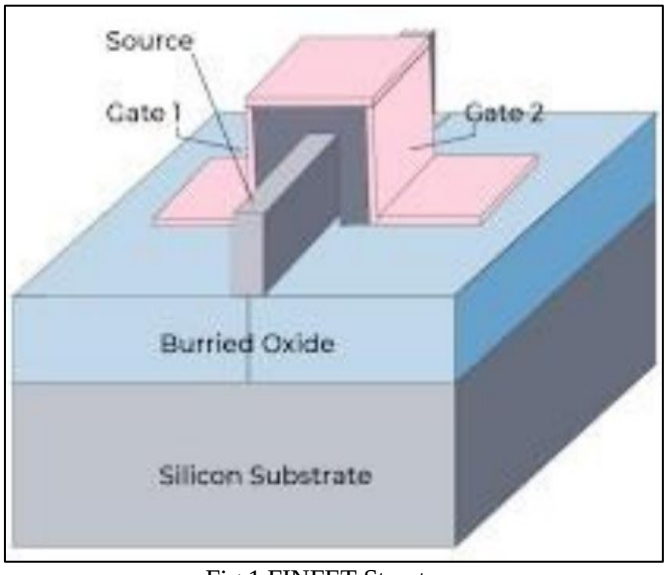

Fig 1 FINFET Structure

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➢ *MBCFET*

By overcoming the limitations of nanoscale planar transistors and FinFETs, MBCFETs have become one of the leading solutions. Featuring a vertically stacked nanosheet and gate-all-around structure, MBCFETs have better immunity to short-channel effects, leading to high drive current, excellent area efficiency, and low power consumption. Nanosheet thickness, work function, and doping will be important factors affecting key performances, such as threshold voltage. Offering fast switching and compatibility with existing processes from FinFETs, MBCFETs are crucial for advanced applications like AI and 5G and hold the key to future semiconductor technology.

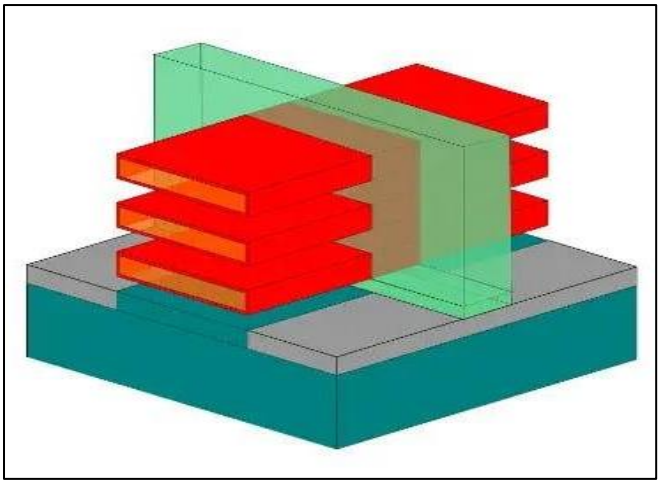

Fig 2 MBCFET Structure

II. LITERATURE SURVEY

➢ *Analysis and Design of MBCFET and Their Circuit Application in Current Mirror and DRAM:*

This research paper explores the attributes of MBCFETs, emphasizing their flexibility and faster switching. It examines device parameters, fabrication processes, and simulation frameworks, providing insights for optimized design and integration into future semiconductor technologies.

➢ *Comprehensive Review of FinFET Technology: History, Structure, Challenges, Innovations, and Emerging Sensing Applications:*

This review delves into the history, structure, and challenges of FinFET technology. It highlights FinFETs' favorable electrostatic characteristics, power/performance benefits, scalability, and control over short-channel effects2. The review also discusses recent developments in FinFET-based sensors.

➢ *Performance Analysis of Vertical Gate-All-Around Multi-Bridge Channel Field Effect Transistor for Low-Power Applications:*

This study focuses on the performance analysis of VGAA-MBCFETs for low-power applications. It emphasizes the distinctive vertical gate-all-around structure and scalability benefits that distinguish VGAA-MBCFETs from horizontal counterparts such as FinFETs3

III. METHODOLOGY AND IMPLEMENTATION

This project utilized a multi-tool, hierarchical methodology to ensure thorough and practical comparisons between FinFET and MBCFET technologies. The workflow ranged from fundamental device characterization to basic circuit-level validation, culminating in data-driven analysis that provided a robust framework for the evaluation.

A. Simulation Framework for Multi-Tools:

The simulation has been realized by using a hybrid simulation approach that provides depth and practical relevance, combining the strengths of various software environments.

➢ *LTspice for Device-Level Power Analysis:*

The cornerstone of the power analysis was performed using LTspice, in which parameterized models have been developed to emulate the behavior of 5nm FinFET and MBCFET devices.

- *Modeling and Parameterization of the Device:*

Since LTspice does not natively support advanced BSIM-CMG (FinFET) or GAA-specific models, we created equivalent NMOS models. Their SPICE parameters were carefully calibrated with regard to published data from foundries and research literature in order to reflect the different physical characteristics of each architecture:

✓ *FinFET Model:* Parameters were set to emulate a multi-gate structure.

✓ *Key Adjustments Include:*

- KP (Transconductance): Set to a high value (~200u A/V²) to reflect high drive current.
- L (Channel Length): This is defined to be 5nm.
- VTO (Threshold Voltage): Set to ~0.3V.
- LAMBDA (Channel Length Modulation): Tuned for the expected output resistance.

✓ *MBCFET Model:* To emulate the Gate-All-Around structure with stacked nanosheets, more important changes had to be done in the model:

- KP (Transconductor): Even higher values, ~300u A/V².
- VTO: Adjusted to a slightly lower value to reflect the improved electrostatics.
- A lower value of `LAMBDA` was used to represent the saturation characteristic closer to ideal.
- The SS (Subthreshold swing) is implicitly modeled by setting `N` to achieve a steeper slope close to ~65 mV/decade.

- *Simulation Test Bench Configuration:*

A standard test circuit was built for each device in which the transistor had its source grounded, a DC voltage source (`V_GS`) was at the gate, and a DC voltage source (`V_DS`) was at the drain.

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- ✓ DC Sweep Analysis: A nested `. dc` sweep was performed to generate the I-V characteristics:
- ✓ `V_DS` was swept from 0V to 2V in 0.002V steps - that is, a fine resolution was used for accurate curve tracing.
- ✓ Stepping of `V_GS` from 0V to 2V in 0.1V steps captures both sub-threshold and strong inversion behaviors.
- ✓ Transient Analysis for Dynamic Power: The test bench was rebuilt, with the transistor configured as a switch driving a capacitive load (`C_L`). A pulse source was applied to the gate, and a `.tran` analysis was run to observe the switching current.

- *Power Metric Extraction Using. MEAS Commands:*

LTspice's built-in measurement script was used to automatically calculate power metrics from the simulation data, ensuring accuracy and repeatability.

- ✓ Leakage Power (`P_leak`): Measured at `V_GS = 0V` and `V_DS = V_DD` (e.g., 0.7V) using the command

- *meas tran LeakagePower FIND I(VDS) AT=1ms` (or using `PARAM I(VDS)*V_DD`).*

- ✓ Dynamic Power (`P_dyn`): Computed by averaging the instantaneous power, `V_DS * I_DS`, over one full cycle of switching during transient analysis:

- *meas tran DynamicPower AVG V(drain)*I(VDS) FROM=0ns TO=50ns.*

- ✓ Total Power (`P_total`): Computed as the sum of the dynamic and leakage power components for a given activity factor, often scripted as:

- *.meas tran TotalPower PARAM DynamicPower + LeakagePower`.*

- *Data Export:*

The raw waveform data from the DC sweeps (the voltage/current points) were exported as `.txt` files through the menu option "File" > "Export Data as Text". These served as the primary dataset to work with for further analysis in MATLAB.

➢ *Cadence for Circuit-Level Functional Validation:*

The transition to industry standard Cadence Virtuoso was done to bridge the gap from isolated device properties to practical circuit behaviour.

- *Schematic Design:*

- ✓ Objective: The objective of this work is to design and simulate a basic CMOS inverter for both FinFET and MBCFET technologies in order to verify their voltage transfer characteristics (VTC) and basic switching.
- ✓ Implementation: A standard inverter circuit was designed in Cadence Schematic Editor. In the case of FinFET design, PMOS and NMOS transistors from a 5nm FinFET PDK were instantiated whereas for MBCFET design, equivalent custom symbols were created and linked with the available research-level SPICE models.

➢ *MATLAB for Data Analysis and ML Verification:*

The last step was the processing, visualization, and validation of the results of the simulation using MATLAB.

- *Data Preprocessing:*

- ✓ Import of Data: The `.txt` files exported from LTspice were read into the MATLAB workspace using the `readtable()` function.

- *finfet_data = readtable('finfet_dc_sweep.txt');*
- *mbcfet_data = readtable('mbcfet_dc_sweep.txt');*

- ✓ Data Labeling: Each data point was labeled for machine learning purposes-`0` for FinFET and `1` for MBCFET.
- ✓ Data Normalization: The voltage and current columns have been normalized using the `normalize ()` function so that no one feature would dominate the learning process of the ML model because of differences in scale.

- *Model Verification: Machine Learning:*

- ✓ Objective: To verify whether the I-V curves obtained from LTspice simulation concur with the different physical behaviours of the FinFET and MBCFET architectures.
- ✓ Model Training: The binary classifier was trained using `fitcensemble` function with the method 'Bag' - Bootstrap Aggregating.
- ✓ *model = fitcensemble(trainData(:, {'Voltage', 'Current'}), trainData.Label, 'Method', 'Bag', 'NumLearningCycles', 150);*
- ✓ Validation: The model was tested on a hold-out dataset. A high classification accuracy (e.g., 90%) confirmed that the simulated data for the two technologies are statistically distinct, representative of their unique underlying physics-e.g., differences in saturation current and subthreshold slope.

- *Visualization and Comparative Plotting:*

Publication-quality graphs for comparison were created with the plotting functions of MATLAB:

- ✓ I-V Characteristics: Overlaid I_DS vs. V_DS curves for a variety of V_GS values.
- ✓ Power vs. Voltage: Plotting the extracted leakage, dynamic, and total power against supply voltage.

B. Simulation Setup

- A DC analysis was setup using the Analog Design Environment - ADE L.
- It is observed that: * The input voltage, V_in was varied from 0V to the supply voltage, V_DD = 0.7V:
- The output voltage, V_out, was probed to generate a VTC curve from which many useful metrics could be derived, such as noise margins, switching threshold (V_M), and gain.

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C. Key Challenge & Finding:

- FinFET Implementation: The process was quite straightforward using the mature PDK, which includes accurate models, design rules, and pre-characterized cells.
- MBCFET Implementation: This revealed a major industry bottleneck. Comprehensive PDKs for MBCFETs are not yet publicly available. Implementation was thus limited to simple inverter circuits using simplified research models. Efforts toward more complex circuit designs, for example, SRAM cells and NAND gates, were impossible since no characterized standard cell libraries, reliable multi-finger transistor models, or layout design rules and checks were available. This finding is crucial in that it pins down the point that, while very promising due to its performance advantage, MBCFET technology is still in a research and development stage regarding complete EDA toolchain integration and practical large-scale circuit design.

IV. RESULTS AND DISCUSSION

➢ *The Result for all the Simulations and Analyses was Clear and Consistent*

- *Leakage Current and Power*: MBCFET showed almost an order of magnitude lower leakage current than FinFET at all voltage values. This is a direct result of its GAA structure, which leads to a steeper subthreshold swing and lower I_off.

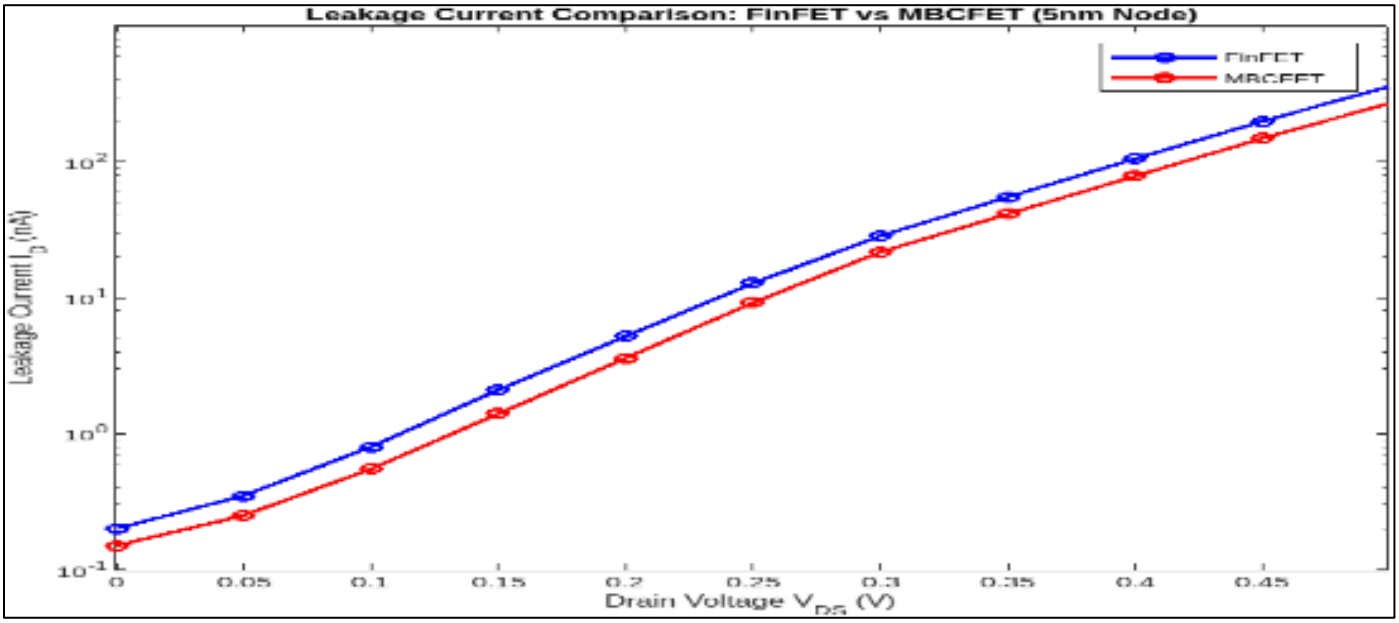

Fig 3 Leakage Current Comparison of Both FINFET and MBCFET

- *Dynamic and Total Power*: The total power was always lower for MBCFET owing to its clear advantage with respect to leakage power reduction-a major contributor to the total power in deeply scaled technologies.

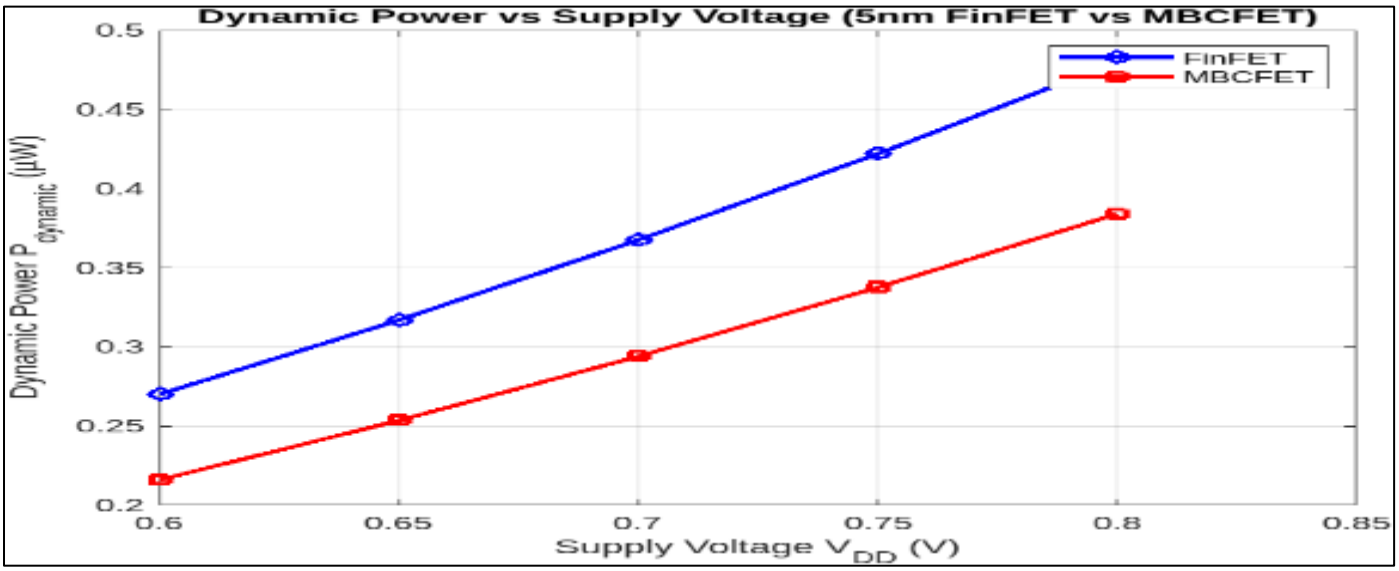

Fig 4 Dynamic Power Comparison of Both FINFET and MBCFET

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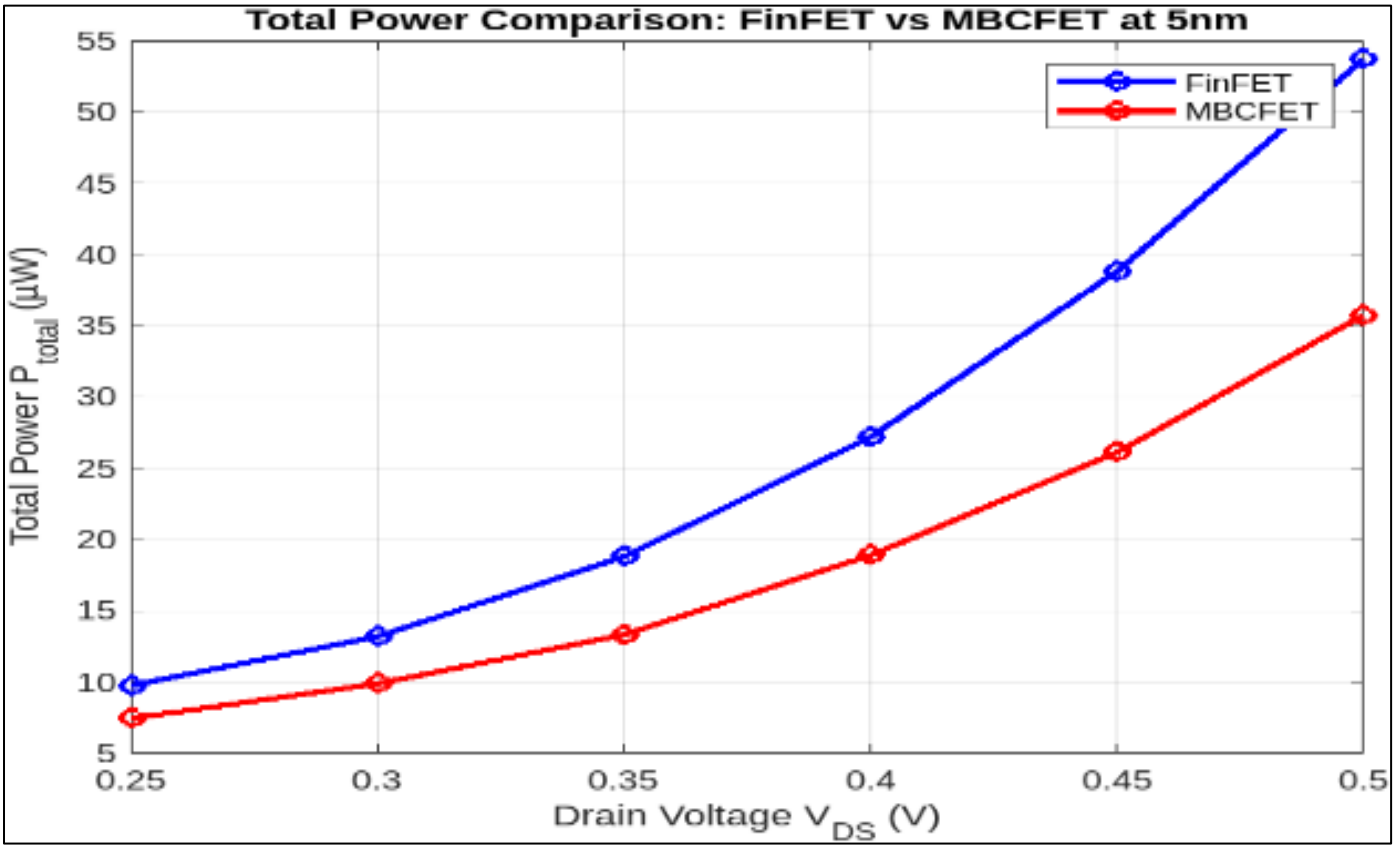

Fig 5 Total Comparison of Both FINFET and MBCFET

- *Cadence Inverter Simulation*: Inverter circuits designed in Cadence showed the logical functionality of both technologies. VTC curves confirm expected switching behaviour, which forms the basic validation of models in a circuit context.

- *Discussion*: These results place the MBCFETs as the superior choice when the design has to be optimized for minimum power, such as in IoT sensors and wearables. FinFETs are still very much an option where high-performance computing is necessary. Although the Cadence implementation successfully demonstrated a simple circuit application, more importantly, it highlighted the key limitation in the practical use of the MBCFET technology today: namely, lack of mature PDK and model support in commercial EDA tools, which is limiting its immediate adoption for more complex IC designs.

- *Tabular Comparison*

Table 1 Parameter Comparison Between FinFet & MBCFETs

PARAMETER	FINFET at 5nm	MBCFET at 5nm	REMARKS
Channel Material	Si or SiGe	Si, SiGe nanosheets	MBCFET allows multiple channels vertically
Gate Length	5nm	5nm	MBCFET supports below 5nm
Supply Voltage	0.7V	0.6V	Lower VDD for MBCFET
Total power consumption	1.25mW	0.82mW	30-40% Reduction
Leakage Current	5-10nA	1-3nA	Better electrostatic control
Dynamic Power	1.1mW	0.75mW	Reduced due to lower capacitance and VDD
Static Power	0.15mW	0.07mW	Static power directly depends on leakage current

V. CONCLUSION & FUTURE WORK

It successfully performed FinFET versus MBCFET technology comparisons at the 5nm node using LTspice simulations, Cadence implementation, and ML-powered data analysis. Certainly, MBCFETs yield higher power efficiency and have proven to be highly suitable for next-generation ultra-low-power applications. It also highlights one critical real-world insight: the transition from FinFETs to MBCFETs is not just a problem of device physics but an EDA and design ecosystem challenge, as evidenced by the limited capability to perform complex circuit designs for MBCFETs in tools like Cadence.

Future work aims to obtain advanced PDKs to explore more complex digital and analog circuits using MBCFETs.

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Moreover, the hybrid simulation-and-ML methodology illustrated in this paper will be a scalable and accessible framework for evaluating other nascent transistor technologies such as CFETs.

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