Volume 11, Issue 4, April – 2026 International Journal of Innovative Science and Research Technology
ISSN No: -2456-2165 https://doi.org/10.38124/ijisrt/26apr633

Stand-Alone PR Controlled Three-Phase Four-Leg Voltage Source Inverter with Linear and Non-Linear Loads

Kiran Reddy Masarla[1]

[1]Engineer – R&D, Medha Servo Drives Pvt. Ltd., Hyderabad, Telangana, India

Publication Date: 2026/05/01

Abstract: This paper presents a comprehensive simulation study of a stand-alone three-phase four-leg voltage source inverter (VSI) operating under both linear and non-linear load conditions. The conventional split-capacitor three-phase three-leg inverter topology suffers from inherent voltage imbalance issues and requires bulky capacitor banks, whereas the four-leg topology eliminates these drawbacks by providing an independent neutral current path. Two control strategies are investigated: the proportional-resonant (PR) controller and the proportional (P) controller, both implemented within a dual-loop voltage and current regulation framework. The space vector pulse width modulation (SVPWM) technique, realized via an offset voltage injection approach, is adopted as the switching modulation scheme. Simulation results are presented and analyzed for balanced resistive (R) loads, unbalanced R loads, balanced and unbalanced resistive-inductive (RL) loads, and non-linear diode-rectifier loads. Performance indices including total harmonic distortion (THD), RMS load current, and neutral current magnitude are evaluated and compared across all loading scenarios.

Keywords: *Three-Phase Four-Leg VSI; Proportional-Resonant (PR) Control; SVPWM; Balanced Loads; Unbalanced Loads; Non-Linear Loads; LC Output Filter; Neutral Current Compensation; THD Analysis.*

How to Cite: Kiran Reddy Masarla (2026) Stand-Alone PR Controlled Three-Phase Four-Leg Voltage Source Inverter with Linear and Non-Linear Loads. *International Journal of Innovative Science and Research Technology*, 11(4), 2723-2734. https://doi.org/10.38124/ijisrt/26apr633

I. INTRODUCTION

Modern power conversion systems increasingly demand reliable, high-quality AC voltage supplies capable of serving both balanced and unbalanced loads, particularly in stand-alone microgrid and uninterruptible power supply (UPS) applications. The three-phase voltage source inverter (VSI) represents the core building block of such systems. Conventional three-phase three-leg VSIs, when configured in four-wire mode, rely on a split DC-link capacitor arrangement to create an artificial neutral point. This approach suffers two fundamental drawbacks: the phase-voltage peak is limited to at most half the total DC-link voltage, degrading DC voltage utilization; and large, expensive capacitors or additional active balancing circuits are needed to maintain neutral-point stability.

The four-leg inverter topology overcomes both limitations by introducing a dedicated fourth inverter leg connected directly to the system neutral point. This additional leg actively regulates the neutral current, eliminating the need for a split DC-link and enabling full DC bus utilization. The DC voltage utilization factor improves to approximately 1.15, while the four-leg topology also demonstrates superior EMC characteristics under unbalanced loading. Only two additional semiconductor switches are required beyond the standard three-leg bridge, making this a cost-effective and performance-superior solution.

The choice of control strategy critically determines the output power quality. PI controllers are widely used but exhibit steady-state error for AC sinusoidal references in the stationary frame, necessitating dq transformation. The proportional-resonant (PR) controller overcomes this by incorporating an ideal resonant element tuned to the fundamental frequency, achieving theoretically infinite open-loop gain and zero steady-state tracking error without coordinate transformation.

A quasi-PR controlled capacitive-coupling grid-connected inverter with a second-order LC filter is presented in [1], demonstrating superior current tracking over PI control. In [2], three-phase four-wire topologies are analyzed for compensation of positive-, negative-, and zero-sequence currents, with a 480 V/50 kVA H-bridge prototype using PR control. Reference [3] proposes an AC-AC converter with a four-leg structure and midpoint DC-link capacitor. A hierarchical control framework for parallel VSI-based microgrids is introduced in [4]. Reference [5] presents a

ISSN No: -2456-2165 https://doi.org/10.38124/ijisrt/26apr633

deadbeat-repetitive controller for V2G four-leg inverters with an LCL filter. Compatible selective harmonic elimination for a NPC four-wire inverter is described in [6], and a carrier-based SVPWM offset voltage method for four-leg VSIs is developed in [7].

Transformer-less PV applications using the four-leg topology with leakage current elimination are explored in [8]. Predictive duty cycle control within a 3D space-vector framework is presented in [9], three-dimensional flux vector modulation in [10], and sphere-decoding MPC in [11]. Reference [12] analyzes three LNPV mitigation strategies with different DC-utilization trade-offs. A minimally switched control algorithm for unbalanced/nonlinear load compensation is reported in [13]. Generalized four-wire cascaded topologies are studied in [14], and quasi-Z-source four-leg inverter predictive control for renewable energy in [15]. The present work builds upon these by implementing and exhaustively evaluating a PR-controlled stand-alone four-leg VSI with SVPWM across seven loading conditions.

II. CIRCUIT TOPOLOGY

The three-phase four-leg VSI topology adopted in this work is shown in Fig. 1. The inverter consists of eight IGBT switches (IGBT1–IGBT8) in four half-bridge legs with antiparallel freewheeling diodes. The first three legs produce the three-phase output voltages for phases R, Y, and B. The fourth leg (IGBT7–IGBT8) connects to the system neutral point N and functions as the active neutral current compensator. A DC bus voltage of 800 V is maintained. Passive LC output filters attenuate switching harmonics and provide smooth sinusoidal load voltages.

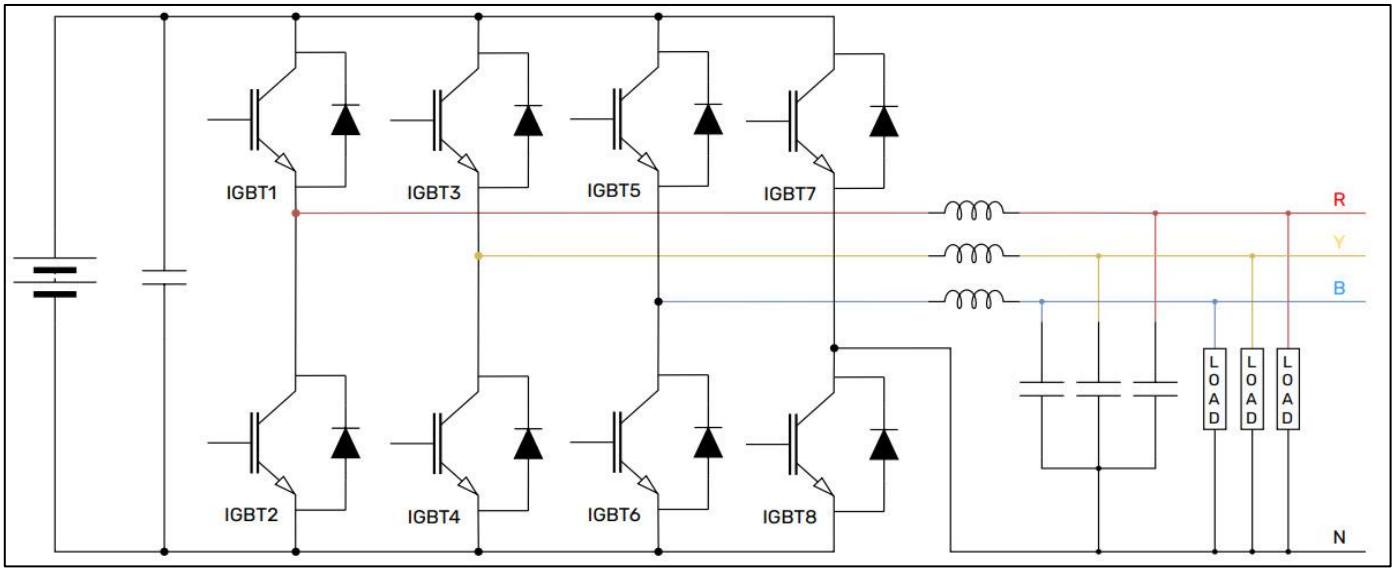

Fig 1 Three-Phase Four-Leg VSI Circuit Topology with IGBT Switches and LC Filters.

The mathematical relationships between the pole voltages and controller reference signals are:

$$E_{ro} = E_rf + E^f_0 \; ; \; E_{\gamma o} = E_\gamma f + E^f_0 \; ; \; E^b_0 = E^b f + E^f_0$$

Where E_{ro}, $E_{\gamma o}$, E^b_0, and E^f_0 are the pole voltages for phases R, Y, B, and the neutral leg; E_rf, $E_\gamma f$, and $E^b f$ are the controller-generated phase voltage references; and E^f_0 is the zero-sequence offset voltage injected to realize SVPWM. The four-leg topology eliminates DC-link midpoint capacitor requirements and prevents neutral currents from destabilizing the DC bus, carrying them instead through the active fourth leg.

III. CONTROL TECHNIQUE

➢ *Proportional-Resonant (PR) Controller*

The PR controller is a frequency-selective regulator that extends PI control to sinusoidal references. It incorporates an ideal second-order resonant element in the forward path, providing theoretically infinite open-loop gain at the resonant frequency ω_n, driving the steady-state tracking error to zero for sinusoidal inputs without requiring synchronous reference frame transformation. The transfer function is:

$$G_{pr}(s) = k_p + k_i s / (s^2 + \omega_n^2)$$

Where $k_p = 0.3$ is the proportional gain, $k_i = 150$ is the resonant integral gain, and $\omega_n = 2\pi \times 50 = 314.16$ rad/s. The resonant branch provides infinite gain at 50 Hz, ensuring zero steady-state error for fundamental-frequency voltage references. The proportional gain $k_p = 0.3$ is intentionally low to limit harmonic amplification. The dual-loop (outer voltage, inner current) control block diagram for all three phases is shown in Fig. 2.

ISSN No: -2456-2165 https://doi.org/10.38124/ijisrt/26apr633

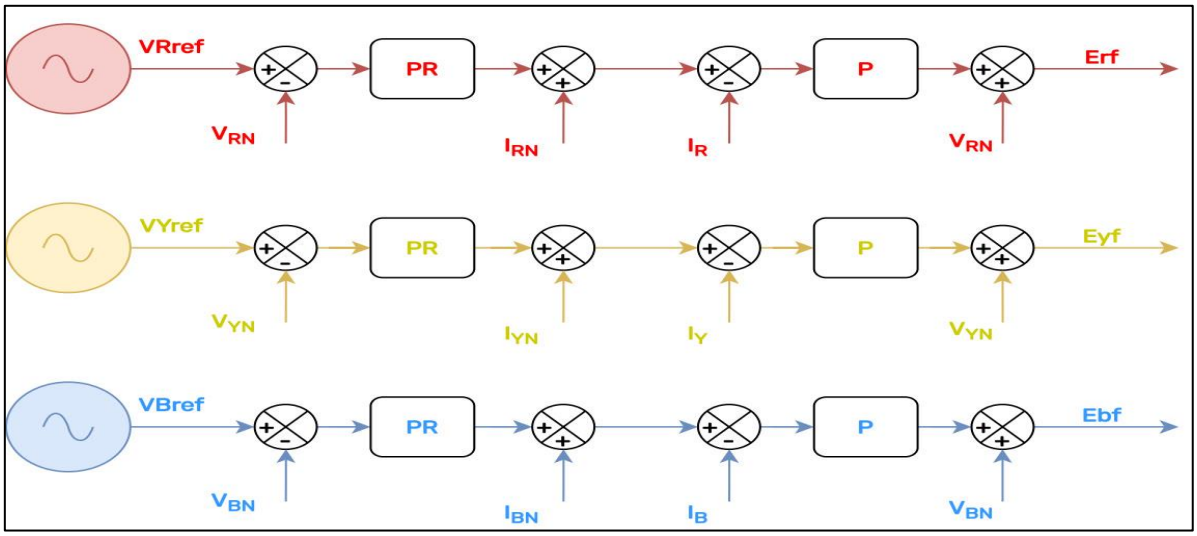

Fig 2 Block Diagram of Dual-Loop PR Control for the Three-Phase Four-Leg VSI.

Each phase employs an identical control loop: the outer PR loop regulates the output voltage (V^RN, V^yN, V^AN) by generating a reference inductor current, while the inner proportional loop tracks the inductor current (I^R, I^y, I^A) to produce the pole voltage reference signal fed to the SVPWM modulator. This cascaded structure provides fast dynamic response and effective rejection of load disturbances.

➢ *Frequency-Domain Analysis*

The frequency response of the PR controller was analyzed through the Bode plot (Fig. 3) computed directly from the transfer function with the design parameters. The magnitude plot exhibits a sharp resonant peak exceeding 70 dB at ω_n = 314.16 rad/s, confirming the theoretically infinite gain behavior. Away from resonance, the magnitude settles to 20 $\log_{10}(k_p) \approx -10.5$ dB. The phase transitions through ±90° at the resonant frequency, characteristic of the ideal resonant element. This frequency selectivity ensures the controller rejects DC offsets and high-frequency disturbances while maximizing gain at 50 Hz.

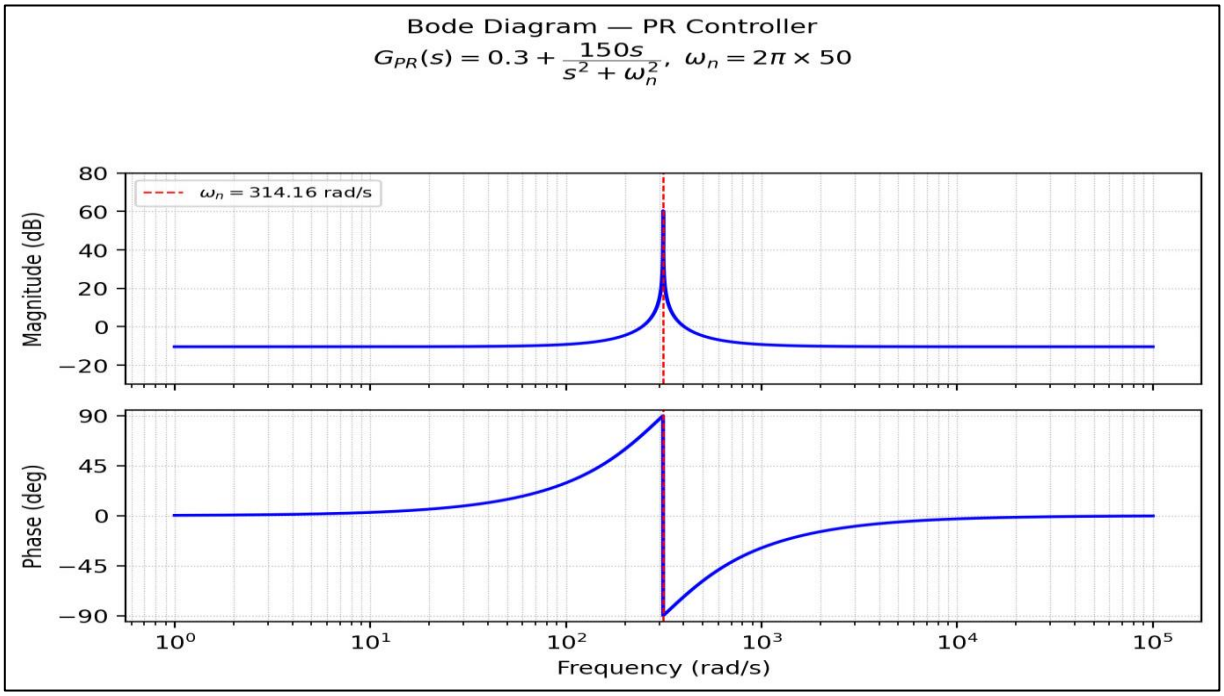

Fig 3 Bode Plot of the PR Controller (k_p=0.3, k_i=150, f=50 Hz). Sharp Resonant Peak Visible at ω_n=314.16 rad/s.

The root locus (Fig. 4) illustrates closed-loop pole trajectories as loop gain K varies from zero to infinity. At K = 0, closed-loop poles coincide with the open-loop poles at $\pm j\omega_n$ on the imaginary axis. As K increases, branches migrate toward the left-half-plane open-loop zeros, confirming closed-loop stability throughout the operating gain range. Both locus branches remain in the left-half plane, ensuring stable operation for all practical gain settings.

ISSN No: -2456-2165 https://doi.org/10.38124/ijisrt/26apr633

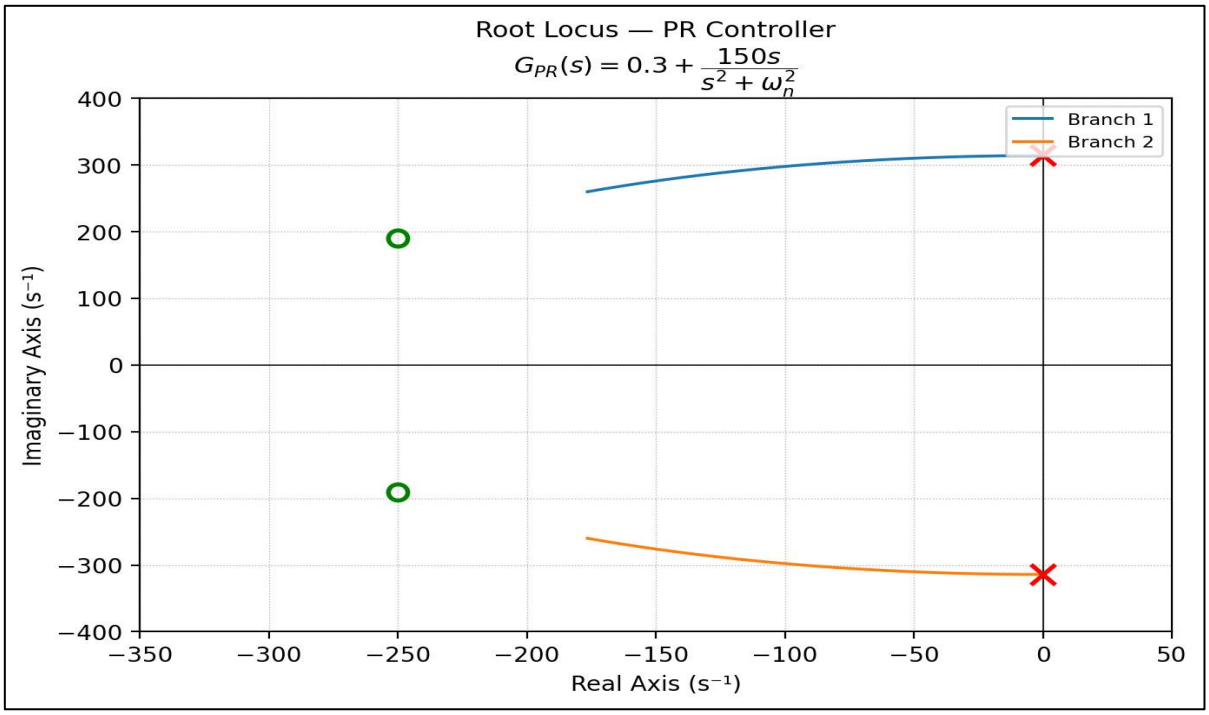

Fig 4 Root Locus of the PR Controller. Both Branches Remain in the Left-Half Plane, Confirming Stability.

➢ *SVPWM via Offset Voltage Injection*

The SVPWM technique is implemented through zero-sequence offset voltage injection, mathematically equivalent to 3D space-vector modulation without its computational complexity. The zero-sequence voltage for the fourth leg is:

$$E_{f0} = \begin{cases} -V_{max}/2, & \text{when } V_{min} > 0 \\ -V_{min}/2, & \text{when } V_{max} < 0 \\ -(V_{max}+V_{min})/2, & \text{otherwise} \end{cases}$$

Where V_{max} = max(E_rf, $E_\gamma f$, E^bf) and V_{min} = min(E_rf, $E_\gamma f$, E^bf). This offset, added to each phase reference, is also used as the fourth-leg reference to eliminate split-capacitor neutral current. Fig. 5 shows the offset voltage generation and PWM pulse assignment: PWM1–2 to leg 1 (R), PWM3–4 to leg 2 (Y), PWM5–6 to leg 3 (B), and PWM7–8 to the neutral leg.

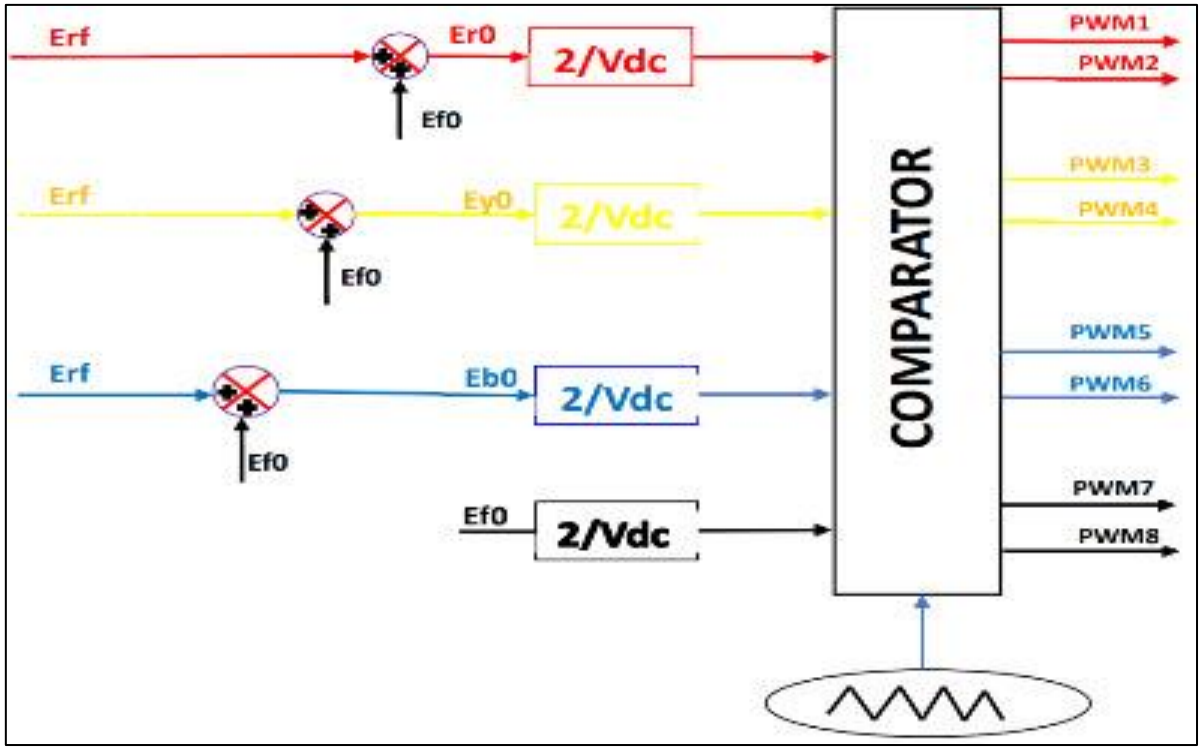

Fig 5 Offset Voltage Generation Block and Triangular-Carrier PWM Pulse Assignment.

ISSN No: -2456-2165 https://doi.org/10.38124/ijisrt/26apr633

IV. SIMULATION RESULTS AND DISCUSSION

The stand-alone PR-controlled three-phase four-leg VSI was simulated in MATLAB/Simulink under seven loading conditions. Table I details the load parameters for balanced and unbalanced cases. The DC bus is 800 V, LC filter values are L = 2.5 mH and C = 100 μF, and the switching frequency is 10 kHz.

Table 1 Load Parameters

Phase	Bal. R	Bal. RL	Unbal. R	Unbal. RL
R	15 Ω	15Ω, 50mH	15 Ω	15Ω, 50mH
Y	15 Ω	15Ω, 50mH	10 Ω	10Ω,100mH
B	15 Ω	15Ω, 50mH	20 Ω	20Ω, 10mH

➢ *Balanced and Unbalanced Resistive Loads*

Three-phase output voltages and load currents for balanced and unbalanced R-loading are shown in Fig. 6. Under balanced loading (15 Ω per phase), the PR controller maintains symmetric sinusoidal voltages with equal amplitude across all phases. RMS current is 15.32 A per phase. Under unbalanced loading (15, 10, and 20 Ω), voltages remain balanced and symmetrical despite load asymmetry, confirming independent per-phase voltage regulation. Load currents differ proportionally to impedance: 15.32 A, 22.98 A, and 11.49 A for R, Y, B phases respectively.

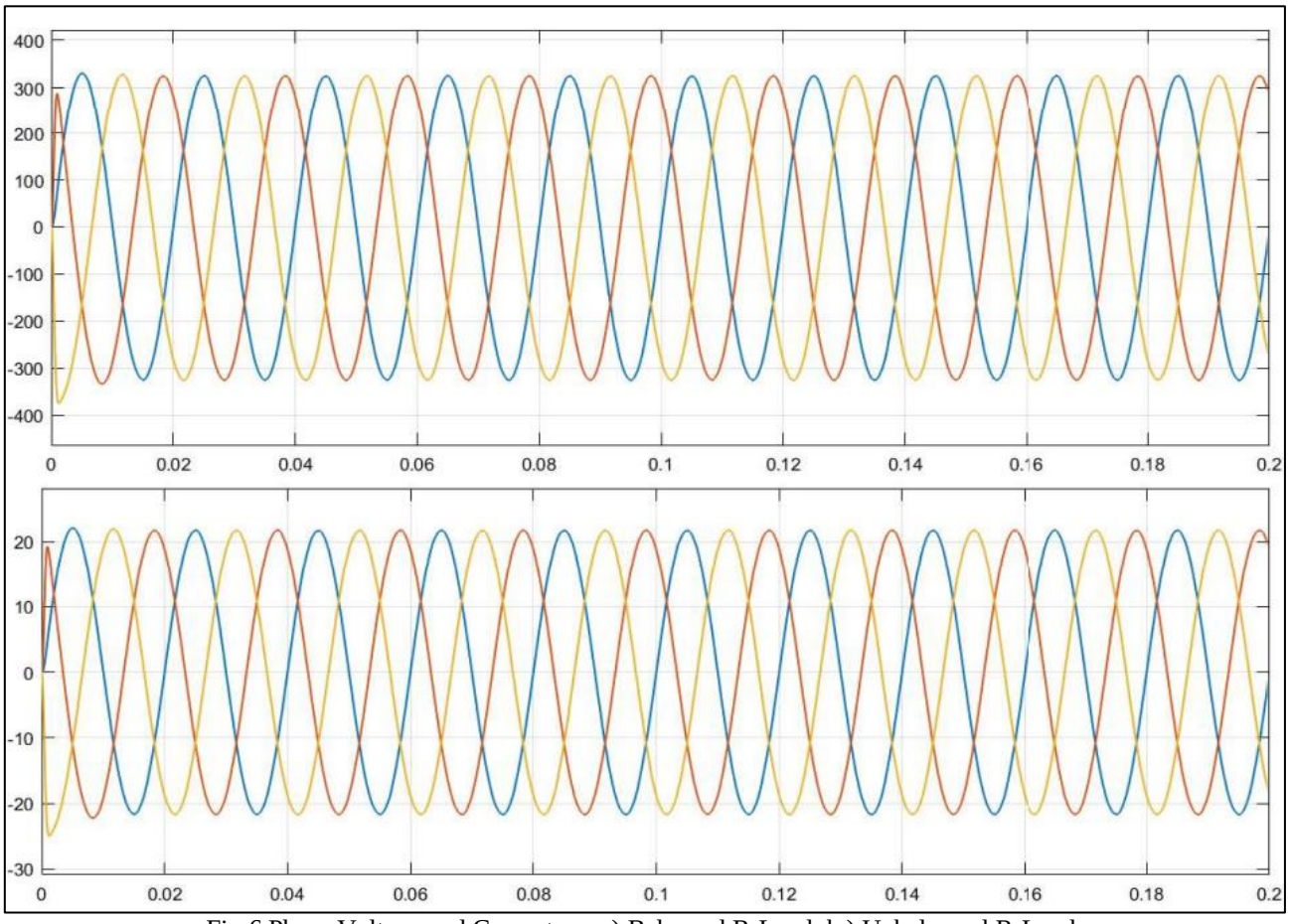

Fig 6 Phase Voltage and Current — a.) Balanced R-Load, b.) Unbalanced R-Load.

➢ *Balanced and Unbalanced RL Loads*

Fig. 7 shows voltage and current waveforms under RL loading. The inductive component introduces a phase lag between voltage and current, visible in the waveforms. Despite the reactive power demand, the PR controller maintains well-regulated output voltages. Balanced RL gives 10.58 A RMS per phase. The unbalanced RL case (varying R and L per phase) produces 10.58 A, 6.969 A, and 11.35 A, reflecting both resistance and inductance variations, yet output voltages remain symmetrical.

ISSN No: -2456-2165 https://doi.org/10.38124/ijisrt/26apr633

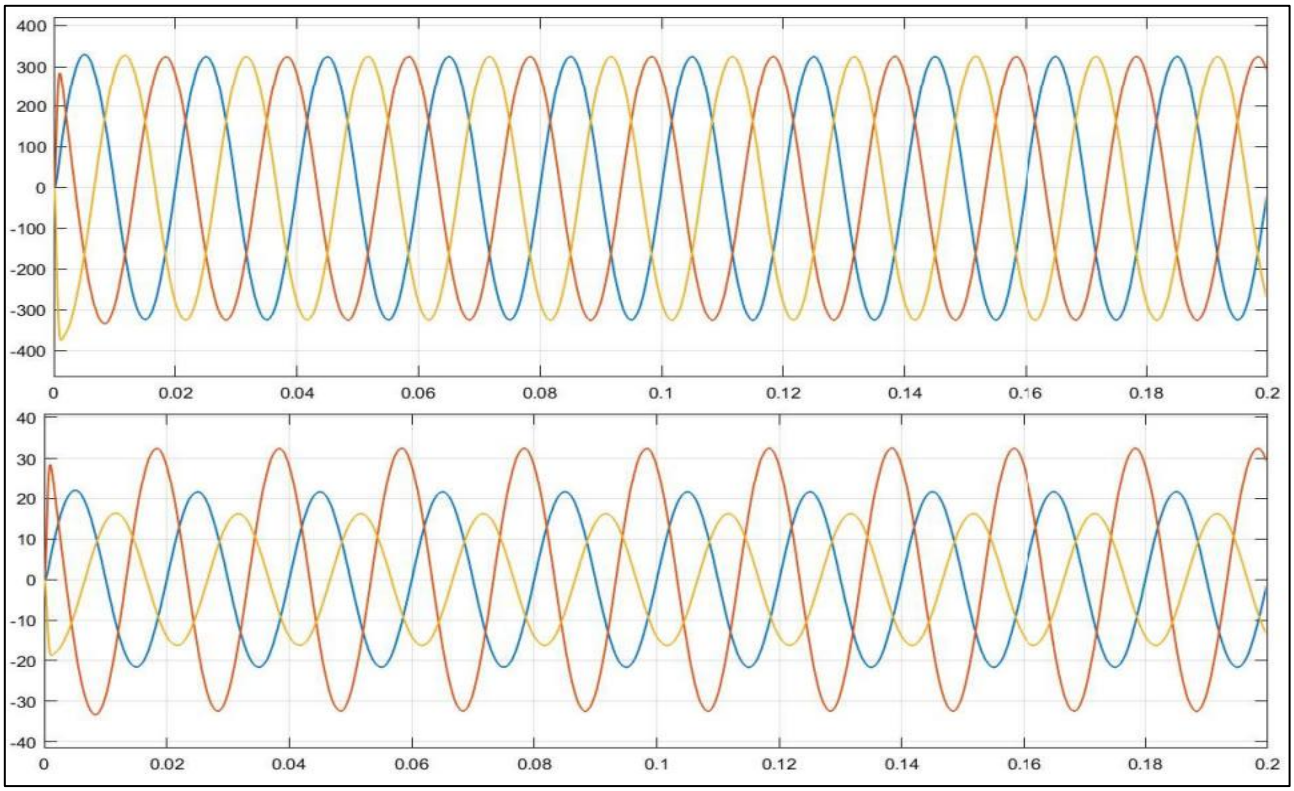

Fig 7 Phase Voltage and Current — a.) Balanced RL-Load, b.) Unbalanced RL-Load.

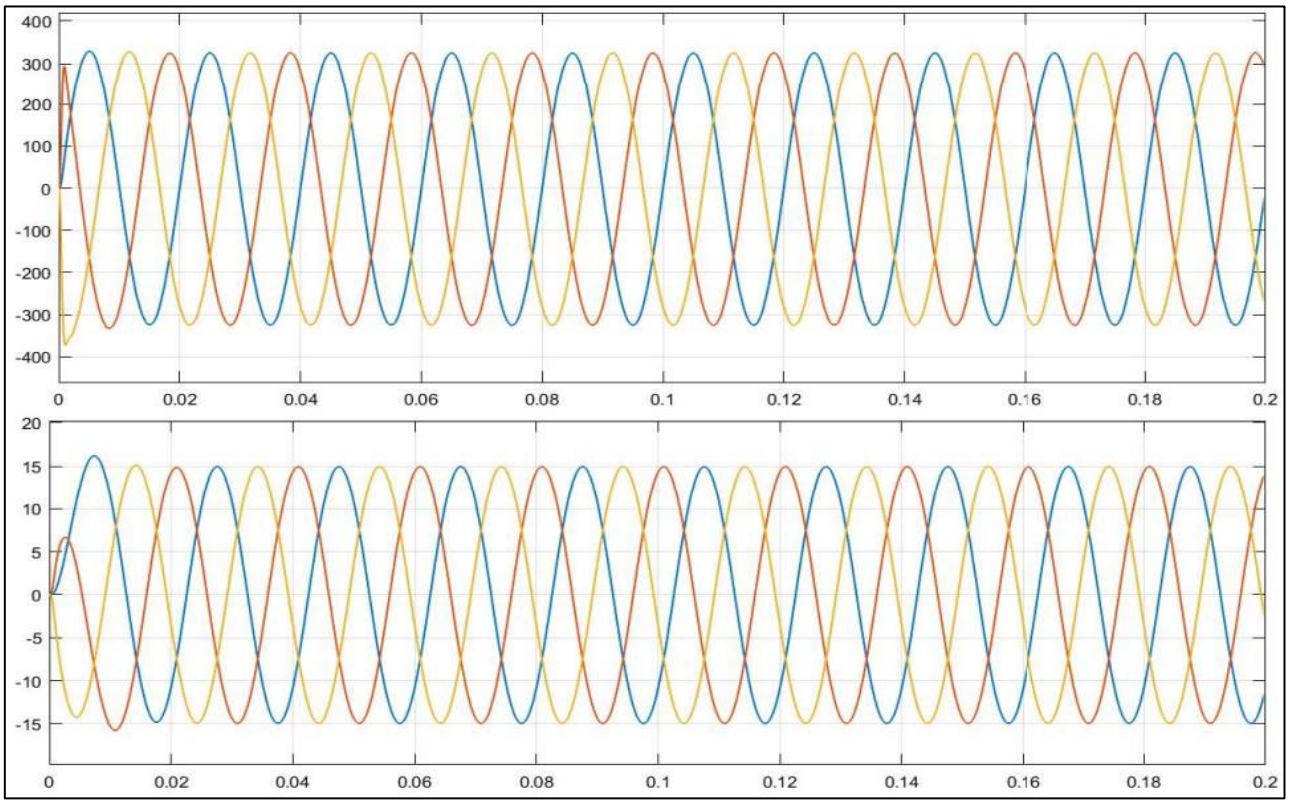

Fig 8 Phase Voltage and Current — Balanced RL-Load (Detailed View Showing Phase Lag).

➢ *Non-Linear Load Results*

The non-linear load (three-phase diode bridge rectifier with DC resistive load) draws pulsed, non-sinusoidal currents, generating significant harmonic content. Despite highly distorted current waveforms, the PR controller maintains sinusoidal output voltages with acceptable THD, demonstrating robustness against load-induced harmonic disturbances. The RMS currents are 22.72 A, 3.64 A, and 5.336 A for R, Y, and B phases, reflecting the asymmetric distribution of rectifier current.

ISSN No: -2456-2165 https://doi.org/10.38124/ijisrt/26apr633

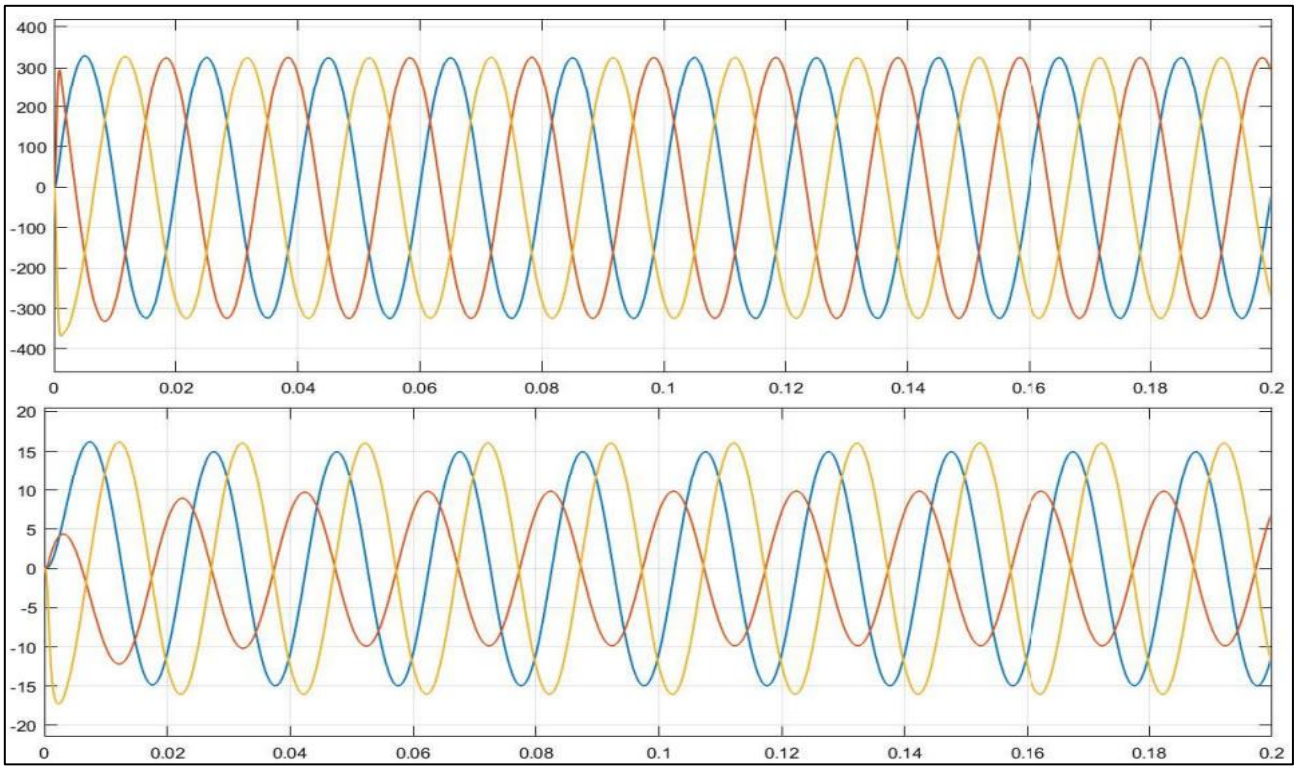

Fig. 9: Phase Voltage and Current Under Non-Linear (Diode Rectifier) Load.

The parallel combination of non-linear load with balanced RL load (Fig. 10) and unbalanced RL load (Fig. 11) creates the most demanding harmonic profiles. RMS currents reach 31.71 A (R-phase, balanced parallel) and 34.09 A (R-phase, unbalanced parallel). Despite this severity, output voltage quality remains acceptable, validating the PR controller's disturbance rejection capability.

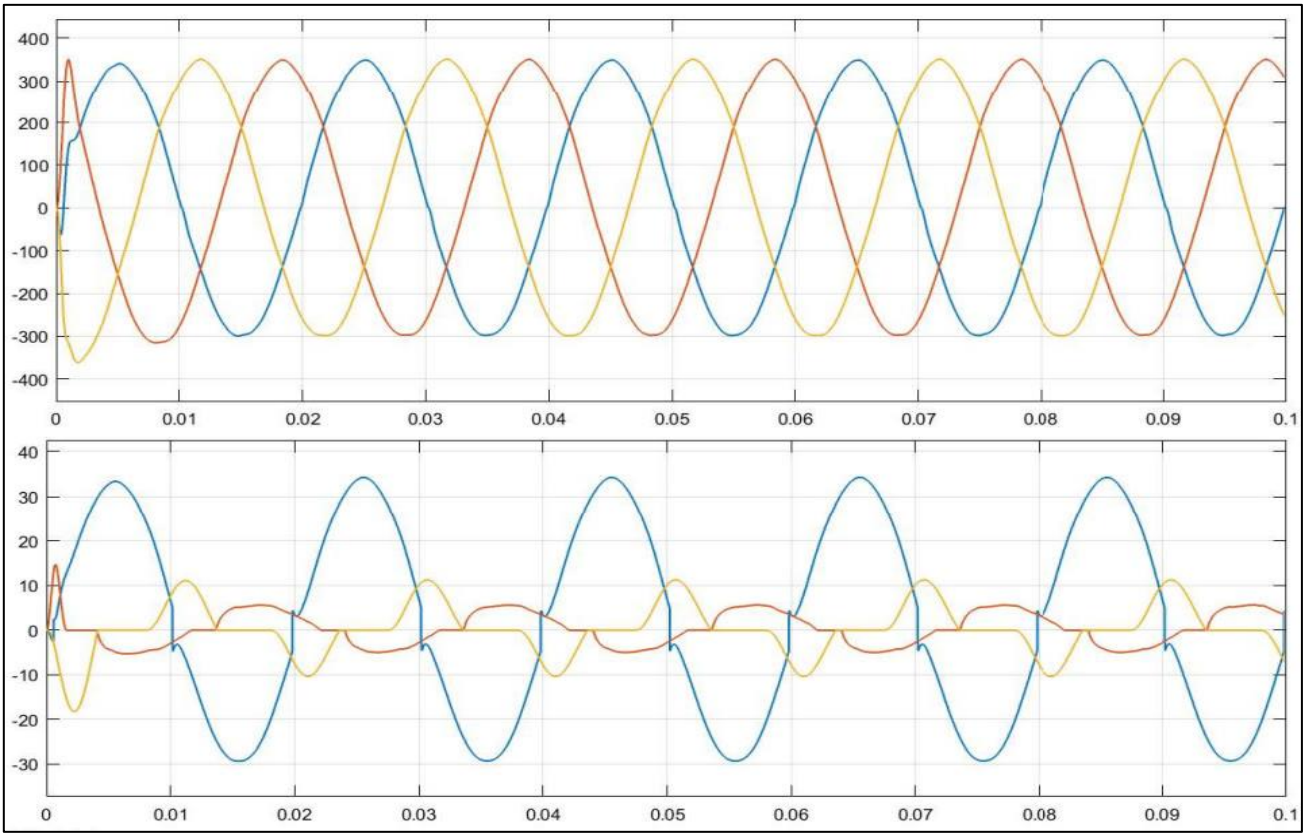

Fig 10 Phase Voltage and Current — Non-Linear Load ‖ Balanced RL.

ISSN No: -2456-2165 https://doi.org/10.38124/ijisrt/26apr633

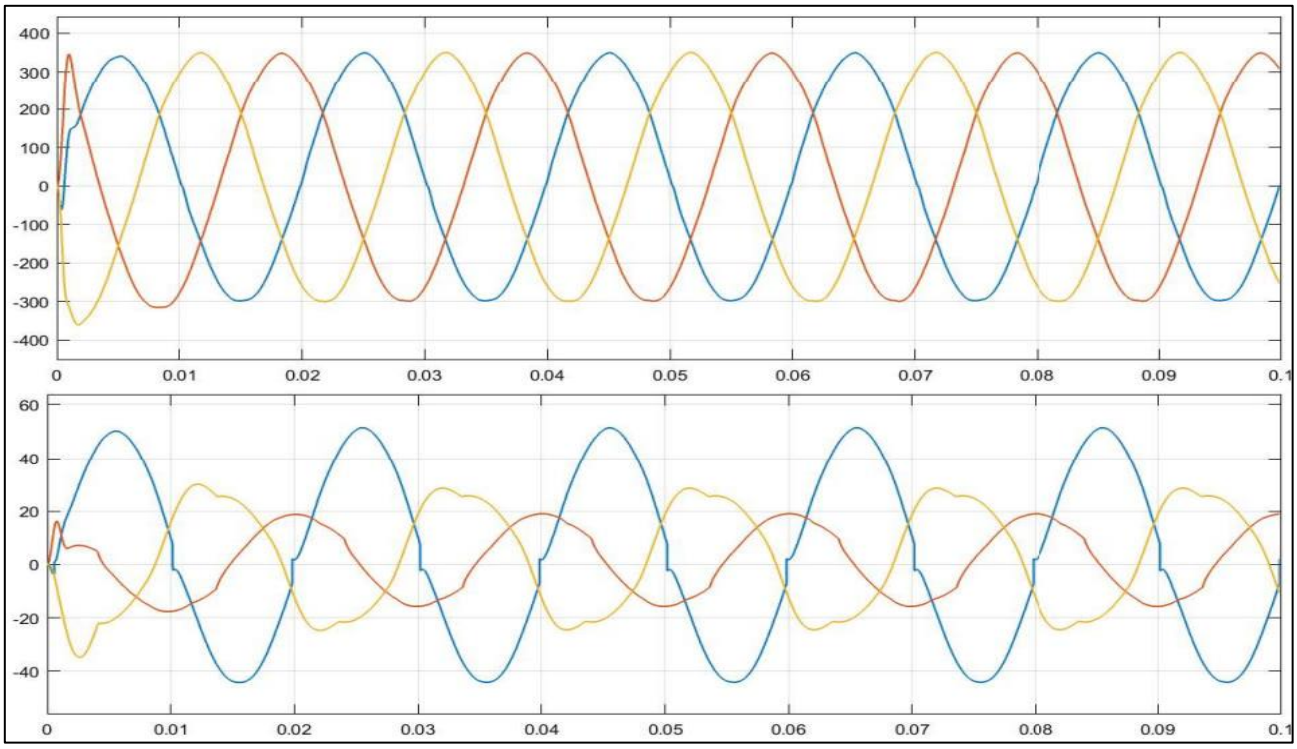

Fig 11 Phase Voltage and Current — Non-Linear Load ‖ Unbalanced RL.

➢ *Inductor Current Waveforms*

Three-phase LC filter inductor currents are presented in Figs. 12–14. Under balanced RL loading (Fig. 12), inductor currents are smooth and sinusoidal, confirming effective PWM harmonic attenuation by the LC filter. The inner current loop tracks the reference current with negligible error. Under non-linear loading (Fig. 13), inductor currents contain harmonic content from the rectifier, but the filter inductance limits di/dt and smooths the dominant ripple. Under the parallel non-linear + RL load (Fig. 14), both fundamental and harmonic components are present simultaneously.

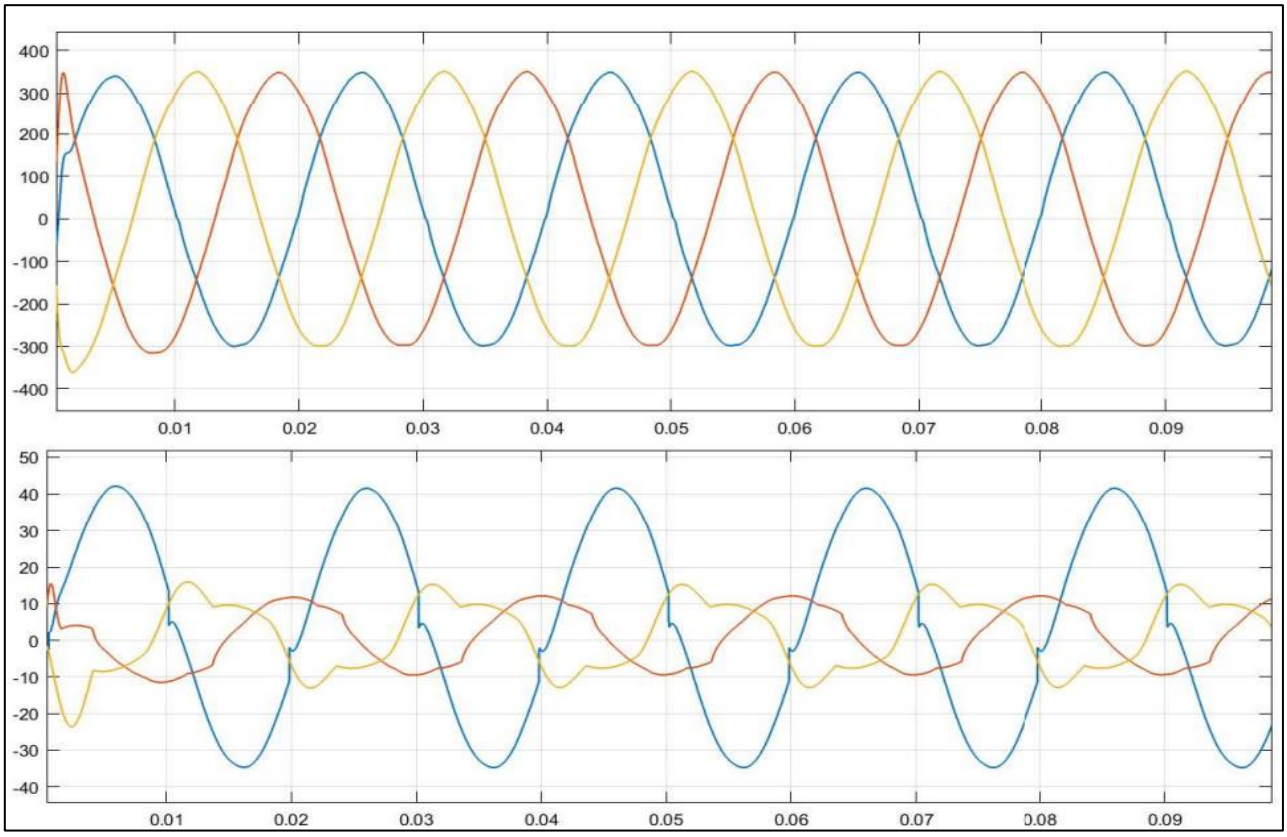

Fig 12 Three-Phase Inductor Current — Balanced RL-Load.

ISSN No: -2456-2165 https://doi.org/10.38124/ijisrt/26apr633

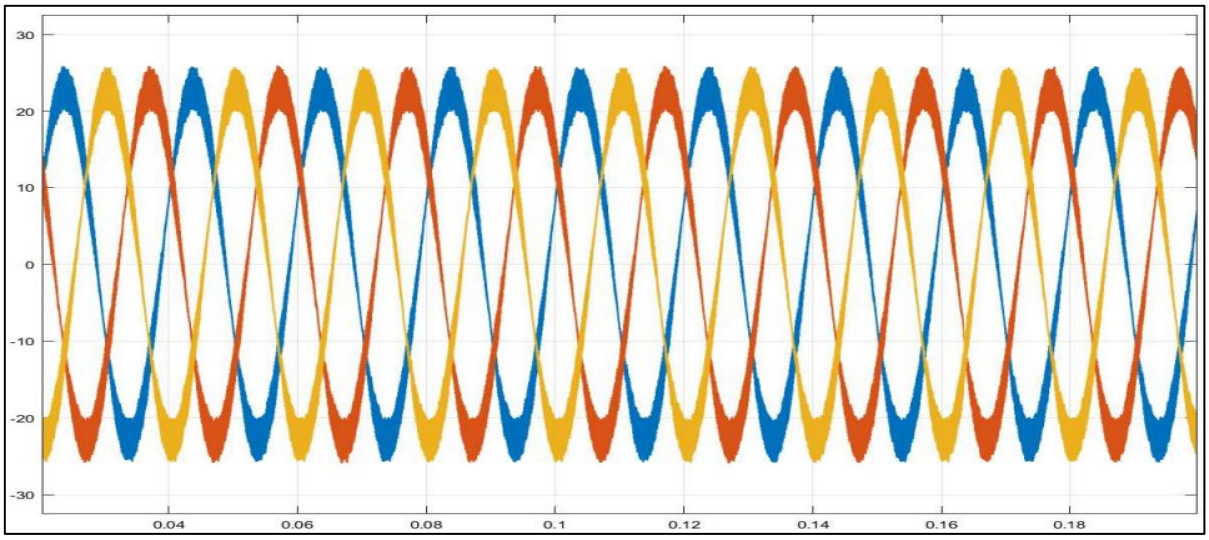

Fig 13 Three-Phase Inductor Current — Non-Linear Load.

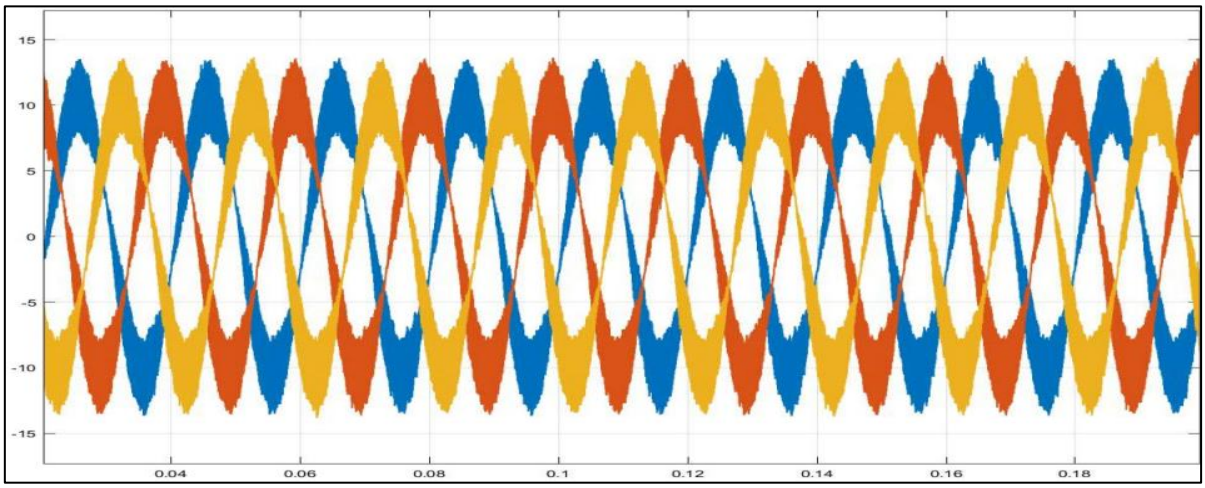

Fig 14 Three-Phase Inductor Current — Non-Linear Load in Parallel with RL-Load.

➢ *Neutral Current Analysis*

The fourth-leg neutral current waveforms are shown in Figs. 15–19. Under balanced three-phase loading, the neutral current is negligibly small due to cancellation of symmetric phase currents (Fig. 16 – balanced R, Fig. 18 – balanced RL). Under unbalanced loading (Figs. 17, 19), sinusoidal fundamental-frequency neutral current flows proportional to phase imbalance. Under non-linear loading (Fig. 20), the neutral current contains predominantly triplen harmonics (3rd, 9th, 15th) from the rectifier. In all cases the fourth leg successfully carries this neutral current, protecting the DC bus.

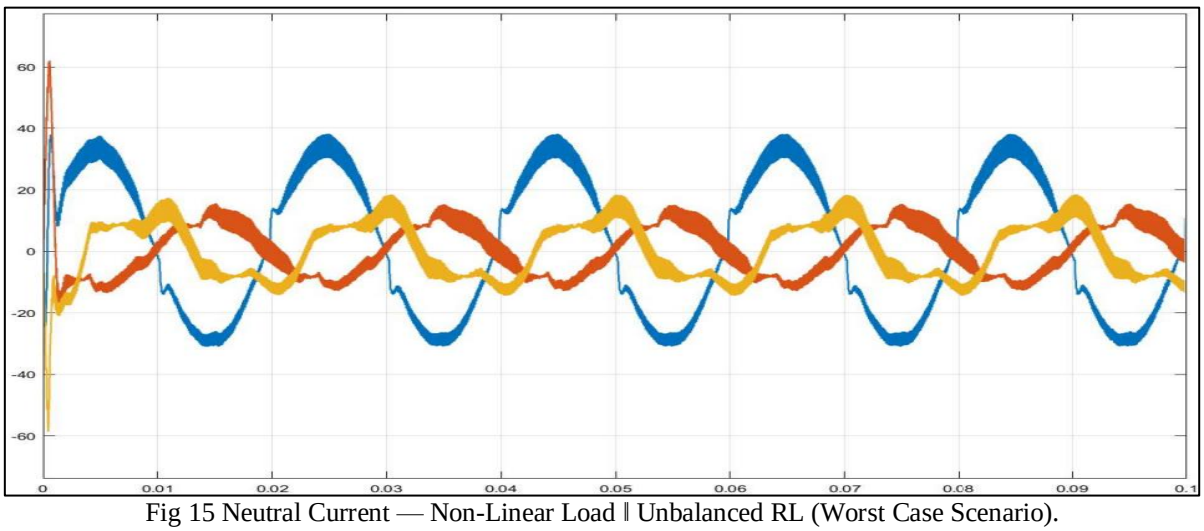

Fig 15 Neutral Current — Non-Linear Load ‖ Unbalanced RL (Worst Case Scenario).

ISSN No: -2456-2165 https://doi.org/10.38124/ijisrt/26apr633

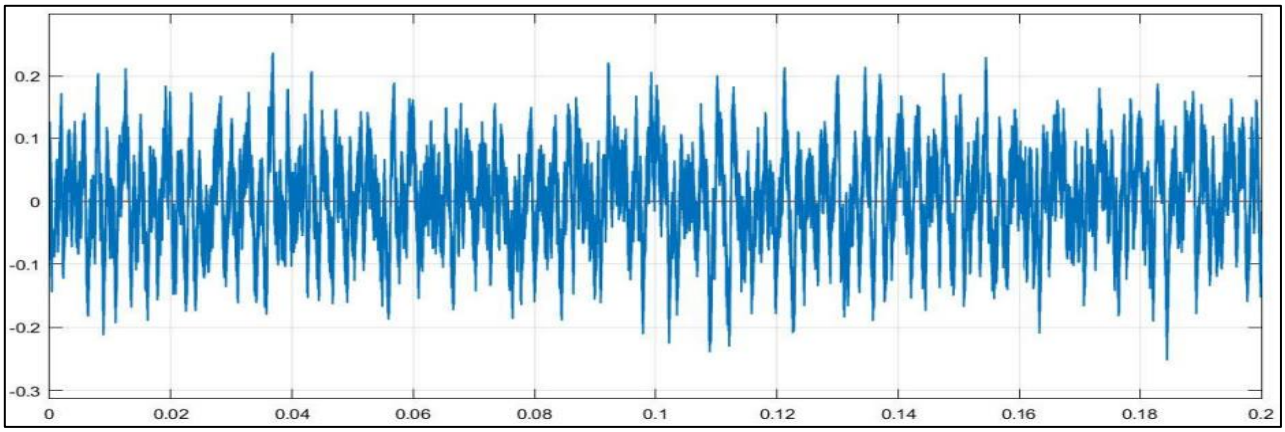

Fig 16 Neutral Current — Balanced R-Load (Near-Zero, Confirms Phase Balance).

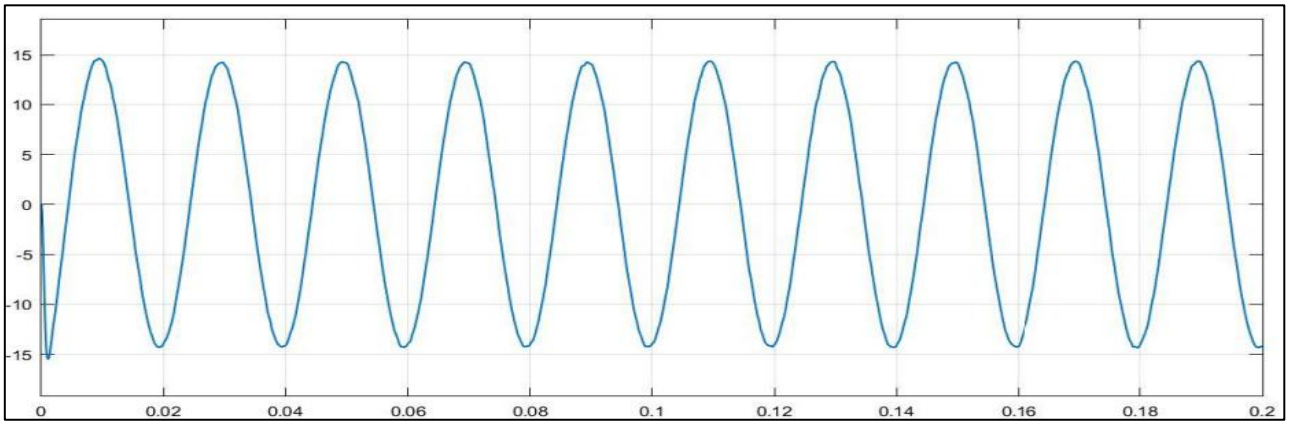

Fig 17 Neutral Current — Unbalanced R-Load.

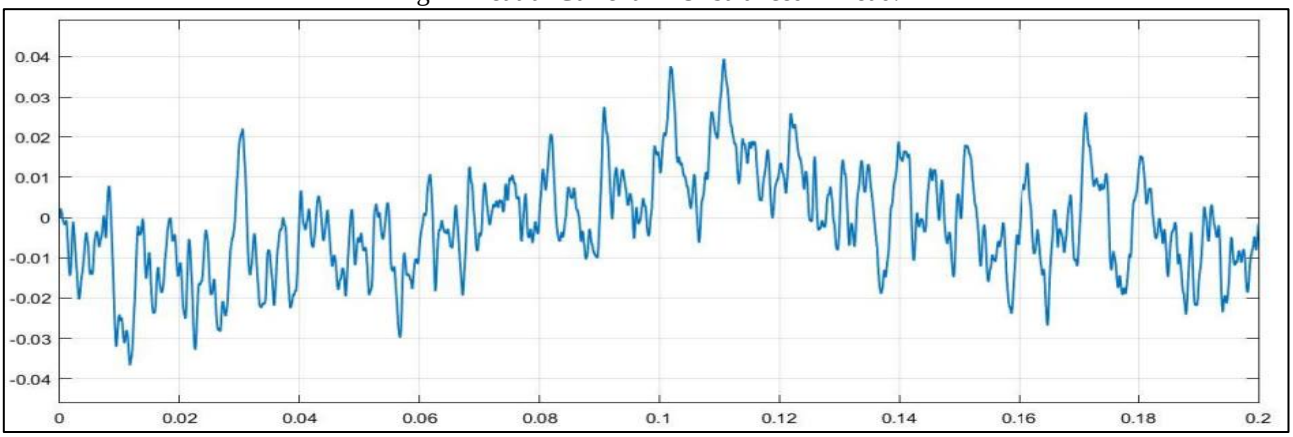

Fig 18 Neutral Current — Balanced RL-Load.

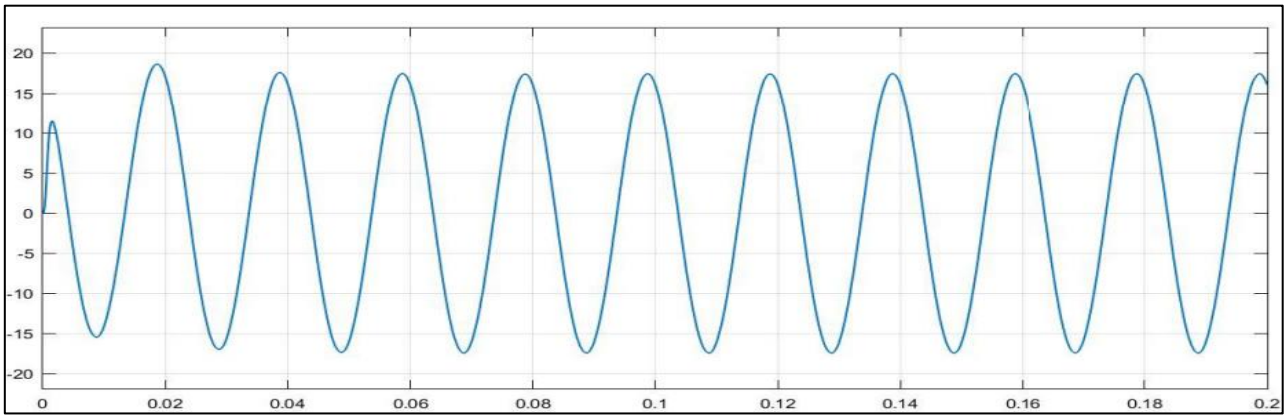

Fig 19 Neutral Current — Unbalanced RL-Load.

ISSN No: -2456-2165 https://doi.org/10.38124/ijisrt/26apr633

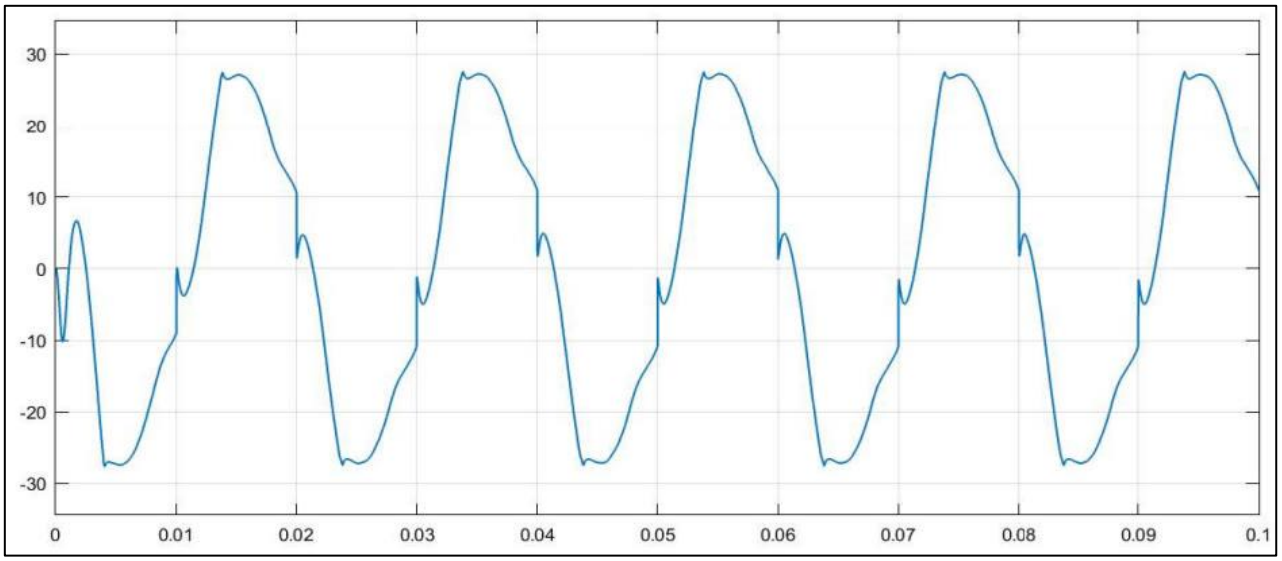

Fig 20 Neutral Current — Non-Linear Diode Rectifier Load with Triplen Harmonics.

➢ *RMS Current and THD Summary*

Table II summarizes the RMS load currents across all seven loading conditions and all three phases. THD is lowest for purely linear (R and RL) loads and rises substantially under non-linear loading due to harmonic voltage drops across filter impedances. The unbalanced non-linear + RL case presents the highest demand, with R-phase RMS reaching 34.09 A. Despite this, output voltages remain well regulated in all cases, confirming the PR controller's effectiveness.

Table 2 RMS Load Current (A)

Load Condition	R-ph (A)	Y-ph (A)	B-ph (A)
Balanced R	15.32	15.32	15.32
Unbalanced R	15.32	22.98	11.49
Balanced RL	10.58	10.58	10.58
Unbalanced RL	10.58	6.969	11.35
Non-linear	22.72	3.640	5.336
NL + Bal. RL	31.71	12.68	13.76
NL + Unbal. RL	34.09	12.69	19.84

V. CONCLUSION

This paper has presented the design, frequency-domain analysis, and comprehensive simulation of a stand-alone PR-controlled three-phase four-leg VSI. The four-leg topology resolves voltage imbalance and DC utilization limitations of split-capacitor three-leg inverters through active neutral current control. The PR controller achieves zero steady-state sinusoidal tracking error without dq transformation; the Bode plot confirms the 70+ dB resonant gain peak at exactly 50 Hz, and the root locus confirms closed-loop stability across all practical gain settings. The offset-voltage SVPWM maximizes DC bus utilization at a factor of 1.15.

Simulation across seven loading conditions validates: (i) symmetric regulated output voltages independent of load type or imbalance; (ii) THD is consistently lower for linear than non-linear loads; (iii) the fourth leg successfully conducts fundamental and triplen harmonic neutral currents under all unbalanced and non-linear scenarios; and (iv) the LC filter effectively attenuates switching ripple. The highest demand condition — non-linear load in parallel with unbalanced RL — yields R-phase RMS current of 34.09 A and triplen-harmonic-rich neutral current, both handled effectively by the control system.

Practical implementation of the ideal PR controller presents challenges due to the infinite-gain resonance; quasi-PR realizations with a finite damping bandwidth are recommended for hardware deployment. Future work will focus on DSP-based hardware implementation, quasi-PR controller evaluation, grid-connected operation, and seamless islanded-to-grid-connected mode transfer.

REFERENCES

[1]. T. Ye, N. Y. Dai, C.-S. Lam, M.-C. Wong, and J. M. Guerrero, "Analysis, Design and Implementation of a Quasi-PR Controller for a Multi-Functional Capacitive-Coupling Grid-Connected Inverter," IEEE Trans. Ind. Appl.

[2]. A. Hintz, U. R. Prasanna, and K. Rajashekara, "Comparative Study of Three-Phase Grid Connected Inverter Sharing Unbalanced Three-phase and/or Single-phase Systems," IEEE Trans. Ind. Appl.

[3]. C. B. Jacobina, I. S. de Freitas, and A. M. N. Lima, "DC-Link Three-Phase-to-Three-Phase Four-Leg Converters," IEEE Trans. Ind. Electron., vol. 54, no. 4, pp. 1953–1961.

ISSN No: -2456-2165 https://doi.org/10.38124/ijisrt/26apr633

[4]. J. C. Vasquez, J. M. Guerrero, M. Savaghebi, J. Eloy-Garcia, and R. Teodorescu, "Modeling, Analysis, and Design of Stationary Reference Frame Droop Controlled Parallel Three-Phase VSI."
[5]. C. Tan, Q. Chen, K. Zhou, and L. Zhang, "A Simple High-Performance Current Control Strategy for V2G Three-Phase Four-Leg Inverter with LCL Filter," IEEE Trans. Transport. Electrif., vol. 5, no. 3, pp. 695–701.
[6]. M. Sharifzadeh, G. Chouinard, and K. Al-Haddad, "Compatible Selective Harmonic Elimination for Three-Phase Four-Wire NPC Inverter," IEEE Trans. Ind. Informat.
[7]. J.-H. Kim and S.-K. Sul, "A Carrier-Based PWM Method for Three-Phase Four-Leg Voltage Source Converters," IEEE Trans. Power Electron., vol. 19, no. 1, pp. 66–75.
[8]. X. Guo et al., "Leakage Current Elimination of Four-Leg Inverter for Transformerless Three-Phase PV Systems," IEEE Trans. Power Electron.
[9]. D. Xiao, K. S. Alam, and M. F. Rahman, "Predictive Duty Cycle Control for Four-Leg Inverters with LC Output Filter," IEEE Trans. Ind. Electron.
[10]. D. C. Patel, R. R. Sawant, and M. C. Chandorkar, "Three-Dimensional Flux Vector Modulation of Four-Leg Sine-Wave Output Inverters," IEEE Trans. Ind. Electron., vol. 57, no. 4, pp. 1261–1269.
[11]. B. Long et al., "Model Predictive Control of a Three-Phase Two-Level Four-Leg Grid-Connected Converter Based on Sphere Decoding," IEEE Trans. Power Electron.
[12]. Z. Liu, J. Liu, and J. Li, "Modeling, Analysis, and Mitigation of Load Neutral Point Voltage for Three-Phase Four-Leg Inverter," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 2010–2021.
[13]. P. Lohia, M. K. Mishra, K. Karthikeyan, and K. Vasudevan, "A Minimally Switched Control Algorithm for Three-Phase Four-Leg VSI," IEEE Trans. Power Electron., vol. 23, no. 4, pp. 1935–1944.
[14]. J. P. R. A. Mello, C. B. Jacobina, and M. B. de R. Correa, "Three-Phase Four-Wire Inverters Based on Cascaded Three-Phase Converters," IEEE Trans. Ind. Appl.
[15]. S. Bayhan, H. Abu-Rub, and R. S. Balog, "Model Predictive Control of Quasi-Z Source Four-Leg Inverter," IEEE Trans. Ind. Electron.
[16]. S. Zhou et al., "Implementation of Cross-coupling Terms in PR Current Control Schemes," IEEE Trans. Power Electron.
[17]. B. Amini et al., "Interface Converter Control of Distributed Generation in Microgrids Using Fractional PR Controller," Electr. Power Syst. Res.
[18]. A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple Analytical and Graphical Methods for Carrier-Based PWM-VSI Drives," IEEE Trans. Power Electron., vol. 14, no. 1, pp. 49–61.
[19]. D.-W. Chung, J.-S. Kim, and S.-K. Sul, "Unified Voltage Modulation Technique for Real-Time Three-Phase Power Conversion," IEEE Trans. Ind. Appl., vol. 34, no. 2, pp. 374–380.
[20]. J.-H. Kim, S.-K. Sul, and P. N. Enjeti, "Carrier-Based PWM Method with Optimal Switching Sequence for a Multilevel Four-Leg Voltage-Source Inverter," IEEE Trans. Ind. Appl., vol. 44, no. 4, pp. 1239–1248.