Design and Analysis of 6T SRAM Cell and 64x64 Memory Array for Low-Power Applications

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Abstract: Static Random-Access Memory (SRAM) plays a crucial role in digital systems, enabling high-speed data storage and retrieval, which is essential for efficient computational performance. Its inherent advantages—such as rapid access times, low latency, true random-access capability, and strong reliability—have established SRAM as the preferred memory choice in cache designs and real-time data processing applications. This project investigates the performance and stability of conventional 6-transistor (6T) SRAM cells implemented in deep sub-micron technology nodes, specifically comparing 65nm, 45nm, and 22nm CMOS technologies. The analysis highlights that SRAM cells designed at the 22nm node achieve notable reductions in power consumption and delay compared to larger technology nodes, aligning with findings reported in prominent journals such as IEEE Transactions on Very Large-Scale Integration (VLSI) Systems. These improvements underscore the benefits of aggressive scaling while maintaining operational stability and robustness against process variations. The results validate that careful design and sizing optimisations at advanced technology nodes can effectively balance performance and area constraints, making 6T SRAM cells viable for high-density cache memory applications in modern digital architectures.

Keywords: *6T SRAM, Power Consumption, Delay, 64×64 Memory Array, Pre-Decoder, Process Variations, 22nm CMOS Technology.*

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I. INTRODUCTION

Very Large-Scale Integration (VLSI) technology is all about making integrated circuits (ICs) that have hundreds of thousands to billions of transistors on one silicon wafer. VLSI has come a long way, making it possible to create advanced microprocessors, memory modules, and system-on-chip (SoC) architectures that are faster, smaller, and use less energy. You need to know a lot about different fields to develop VLSI systems. These include semiconductor device physics, electrical circuit design, physical layout methodologies, and verification processes.

As Moore's Law says, the size of transistors keeps getting smaller. This means that designers can fit more features onto a smaller area of silicon, which makes the device work quicker and use less power. But this scale comes with a lot of problems, like short-channel effects, larger leakage currents, and differences induced by the way things are made. These problems require new ways of designing things and good ways to deal with them. Memory is an important part of digital systems because it stores program instructions, temporary data, and the results of calculations. Most of the time, memory technologies are divided into two groups: volatile and non-volatile. SRAM and DRAM are examples of volatile memory types that need constant power to keep data. Non-volatile memories, on the other hand, keep data even when power is turned off. SRAM is a popular choice for volatile memory because it is fast and can support random data retrieval. This makes it good for cache memory and register storage.

It's extremely crucial to make low-power Static Random Access Memory (SRAM) for things like implantable medical devices and wireless communication systems, where saving power is important for making batteries last longer and making sure the system works reliably. The frequencies that these systems usually work at are between hundreds of kilohertz and tens of megahertz. Power efficiency is becoming more and more important because SRAM takes up a lot of space on modern SoCs. It presently makes up around 70% of the total die size, and this number is expected to keep growing. As technology gets better and SRAM arrays get bigger, leakage current has become a big problem that wastes power and makes these memory structures use more energy overall.

SRAM cells are very important for figuring out the overall speed, size, and power of digital integrated circuits. A standard SRAM architecture has a number of important

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parts, such as the memory array for storing data, row and column decoders for choosing specific memory locations, precharge circuits for getting bitlines ready for read operations, and sense amplifiers for accurately picking up stored data. The memory array is made up of many separate storage cells, each of which can hold one bit of information. ability to hold one binary digit.

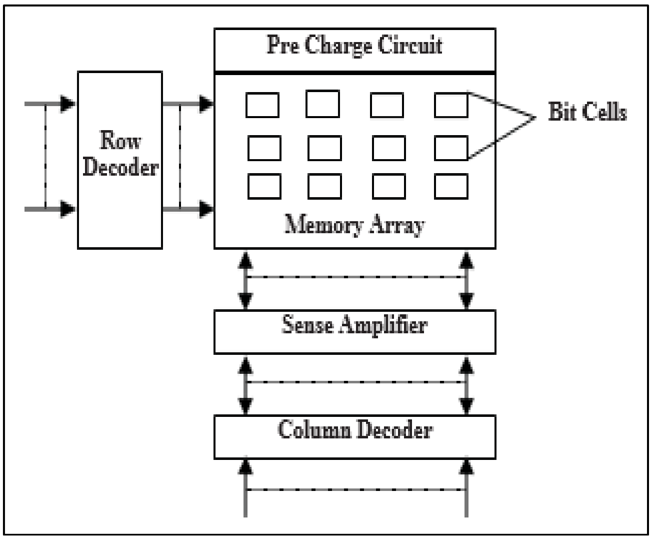

Fig 1 Architecture of SRAM

II. RELATED WORK

Calhoun and Chandrakasan looked at what affects Static Noise Margin (SNM) in their study of subthreshold SRAM cells made with 65 nm CMOS technology. Their research assessed the influence of transistor size, supply voltage, temperature, and both local and global process changes. The results showed that changes in threshold voltage have the biggest effect on SNM. From this discovery, they created an analytical model that could anticipate how SNM would act, especially in the worst-case scenarios that were shown by the tail of the statistical distribution [1].

Chang et al. suggested a better 8T SRAM cell structure that would make it more resistant to changes in the manufacturing process and allow it to work reliably at low supply voltages for high-performance cache applications. This design made things more stable while keeping the same amount of space as a regular 6T SRAM cell. The researchers tackled implementation problems at the array level by changing the way 6T designs are made. They were able to make them more tolerant of changes and work better at low voltages without needing extra voltage sources [2].

Chang et al. also made a 32 kb SRAM array utilizing 90 nm CMOS technology and a 10-transistor bit-cell in another paper. This design allowed for bit-interleaving and used a differential sensing system. The cell's stability was greatly enhanced by splitting the read and write routes. Also, using a dynamic DCVSL approach lessened the impacts of bit-line leakage noise, making it possible to work reliably at supply voltages as low as 160 mV. The leakage power of this 10T cell was found to be similar to that of standard 6T SRAM cells [3].

Date et al. came up with a good importance sampling method to make it easier to figure out the yield of SRAM. Their method coupled hypersphere sampling with an automated way to find the best shift vectors, which made Monte Carlo simulations much more efficient. This strategy kept accuracy while cutting the number of simulation runs needed by up to six orders of magnitude, even when looking at very low failure probabilities like 10^{-10} [4].

Dreslinski et al. looked into Near-Threshold Computing (NTC) as a way to make digital circuits use less energy. They characterized NTC as functioning at supply voltages near the transistor threshold voltage, enabling significant reductions in energy usage while preserving satisfactory performance standards. The paper also looked at the main problems that come up when trying to use NTC and talked about current research efforts to solve these problems. The authors highlighted its prospective applications, spanning from low-power sensor devices to high-performance computing platforms [5].

Guo and others did a lot of research on variability to see how stable SRAM is in 45 nm CMOS technology. Their work was all about coming up with quick and accurate ways to test how well functional memory arrays can read and write. By employing direct bit-line measuring techniques in constructed test chips, they attained substantial concordance with standard SRAM performance metrics and minimum operating voltage (V_MIN), particularly under conditions approaching failure [6].

Pasandi and Fakhraie put forward a proposal for a 256 kb 9T SRAM cell that made both reading and writing faster. The proposed cell had a read static noise margin that was 219% better and an ION/IOFF ratio that was 113% better than the usual 6T SRAM cell when the supply voltage was 300 mV. The proposed design also has a lower minimum operating voltage of 350 mV, which is far lower than the 725 mV required for standard SRAM cells [7].

Ahmad et al. built an 11T SRAM cell based on Schmitt-trigger ideas to make it more stable and use less power. This single-ended design showed big improvements in both read and write static noise margins while keeping the leakage power low. A lot of Monte Carlo simulations showed that the cell is strong enough to handle changes in process, voltage, and temperature. It also performed better than standard SRAM cell designs on a number of assessment metrics [8].

Table 1 Summary of Literature Survey

Reference paper	Description	Key Points
Jayram Shrivas et al. [20]	Discussed 7T SRAM bit cells using a sleep method to reduce SRAM leakage power. A high-k gate dielectric material was used.	- 7T cell reduces discharge power. - Sleep transistor reduces leakage, wake-up transistor decreases latency. - High-threshold-voltage PMOS transistor used.
Shalini Singh et al. [21]	Implemented 1KB memory with SRAM using a 7T SRAM cell with low leakage current. Tools like Cadence Virtuoso were used for design.	- Leakage current: 20.16 pA. - Average latency: 21 ns. - Power for read: 51.57 mW, write: 447.3 mW. - Noise margin and stability impacted by voltage.
Alex Gong et al. [22]	Focused on improving read stability and periodic precharge issues in SRAM design with a novel architecture, incorporating sense-amplifying cells.	- Increased read resilience. - 8-transistor cell design. - 30% increase in area compared to 6T SRAM. - Lower power consumption under same conditions.
Rashmi Bisht et al. [23]	Developed an SRAM array with differential sense amplifiers and cross-coupled CMOS inverters to reduce static power dissipation.	- Noise immunity through differential sense amplifiers. - Full CMOS SRAM more stable than resistive load SRAM. - Power consumption: 24.58 mW.
Himanshu Banga et al. [24]	Demonstrated a 16x16 SRAM with reduced die area and leakage power using sleep and forced transistor techniques.	- Forced transistor 99.94% quicker than sleep approach. - Forced transistor reduced power usage by 56.92%. - Designed in UMC 180 nm technology.
Shyam Akashe et al. [25]	Developed a read static noise margin-free 5-transistor SRAM cell to address performance and power consumption issues in standard SRAM cells.	- 21.66% smaller area compared to 6T SRAM. - 28.57% faster performance. - 72.10% less leakage current than 6T SRAM. - Latency 70% lower than 6T SRAM.
S. Ahmad et al. [7]	Proposed a Schmitt-trigger-based 11T SRAM cell for low-power operation with improved SNM and robustness.	- 11T SRAM improves SNM and reduces leakage power. - Higher ION/IOFF ratio improves robustness. - The proposed cell outperforms others in terms of stability, delay, and power
G. Pasandi & S. M. Fakhraie (2015)	Introduced a 9T SRAM cell for near-threshold operation with enhanced write and read operations.	- 9T SRAM increases read SNM by 219% and reduces write/read power by 92%/93%. - Reduces minimum operating voltage (VDDmin) to 350 mV. - Increased SRAM cell area by 83%, but the design enables more efficient sharing of read/write circuitry.

III. SRAM ARRAY ARCHITECTURE AND OPERATION

In Static Random-Access Memory (SRAM) design, the memory cell acts as the primary structural unit and typically consumes a large fraction of the total chip area. A standard six-transistor (6T) SRAM cell employs a straightforward and space-efficient arrangement featuring two access transistors along with two cross-coupled inverters. Together, these inverters establish a bistable latch capable of retaining a single bit of data. Through the access transistors, the internal storage nodes are connected to the complementary Bit Lines (BL and $\overline{BL}$), with this connection regulated by the Word Line (WL).

Operation of the SRAM cell falls into three distinct phases: hold, read, and write. In hold mode, the Word Line is held low, which deactivates the access transistors and isolates the cell from the Bit Lines. Under these conditions, the cross-coupled inverters sustain each other via positive feedback, ensuring the stored value remains intact as long as power is applied. No periodic refresh cycles are necessary to maintain the data.

To read data from the cell, both Bit Lines are first raised to a high voltage level. When the Word Line is activated, the state stored inside the cell begins to pull one of the Bit Lines lower. If the node Q holds a ‘1’ and the node $\overline{Q}$ holds a ‘0’, a path opens from $\overline{BL}$ down to ground. This path runs through the access transistor on the $\overline{Q}$ side and the pull-down transistor beneath it. As current flows, the voltage on $\overline{BL}$ starts to drop. On the other side, BL holds its charge because the pull-up transistor connected to Q keeps it near the supply level. This creates a small voltage gap between the two line. A sense amplifier then measures this gap and strengthens it into a full Q.

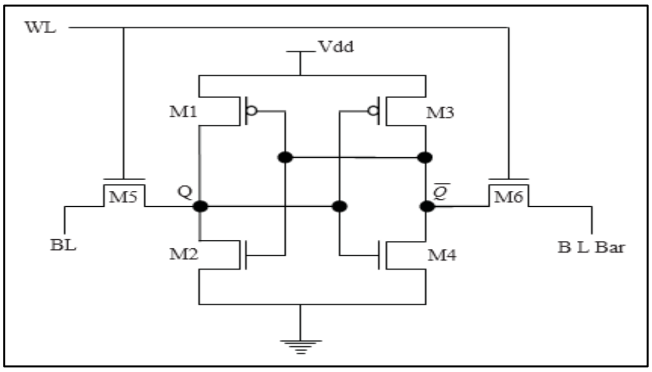

Fig 2 6T SRAM Cell

The normal 6T SRAM cell has problems working in some situations, especially when it comes to read steadiness. The pull-up, pull-down, and access transistors interact and have different drive strengths during a read process, which is what causes these problems. Process differences become more noticeable as device sizes keep getting smaller into the deep submicron range. As a result, device parameters change more, and the total reliability of the circuit increases. Because these limits exist, different designs for memory cells have come up. Fig. 3 shows the 8T SRAM cell [21], which is an early version. With two extra nMOS transistors, this design separates the read process from the internal storage nodes. By separating them in this way, read disturb problems are mostly prevented, and cell stability enhances. Although the extra transistors do make leakage power higher, the amount of leakage can change based on the data being stored.

The work showcased here tries to improve SRAM arrays' overall performance and power efficiency. This is made possible by using advanced circuit design techniques, a well-thought-out 6T SRAM cell layout, and mindful merging of sense amplifiers. Both efficiency and energy.

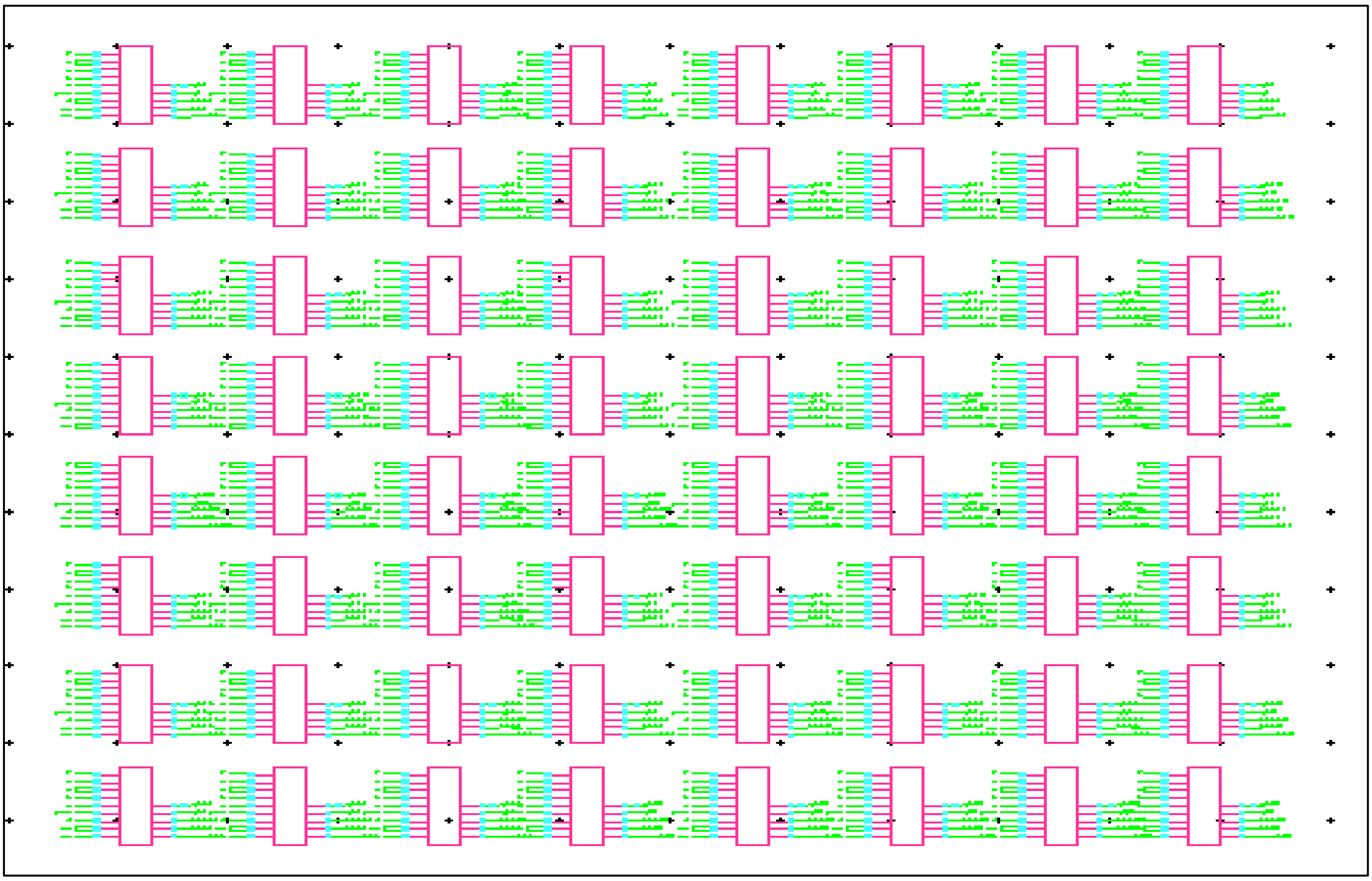

Fig 3 6T SRAM of 64 x 64 Array

➢ *SRAM Timing Diagram*

An SRAM cell operates in three primary modes: standby (idle), read (retrieving data), and write (updating stored data). During read and write operations, the cell must maintain sufficient read stability and write stability, respectively, to ensure reliable performance. The behavior in each state can be described as follows:

In standby mode, when the Word Line (WL) is not asserted, the access transistors (M5 and M6) disconnect the cell from the Bit Lines (BL and $B\overline{L}$). The cross-coupled inverters formed by transistors M1–M4 continue to reinforce each other as long as they are connected to the supply voltage, preserving the stored value.

In principle, a read operation could be performed by enabling the WL and reading the state of the cell through a single access transistor and its corresponding bit line (for example, M6 and BL). However, in practical circuits, the Bit Lines are long and have significant parasitic capacitance, which slows down the read process. To improve read speed, both bit lines are first precharged to a high voltage (logic '1'). When the WL is asserted, both access transistors (M5 and M6) become conductive, allowing the internal node voltages to influence the Bit Lines. This results in a small voltage difference between BL and $B\overline{L}$, reflecting the stored logic value. A sense amplifier detects this differential, amplifies it, and determines whether a logic '1' or '0' is stored in the cell. Figure 3 illustrates the read operation sequence.

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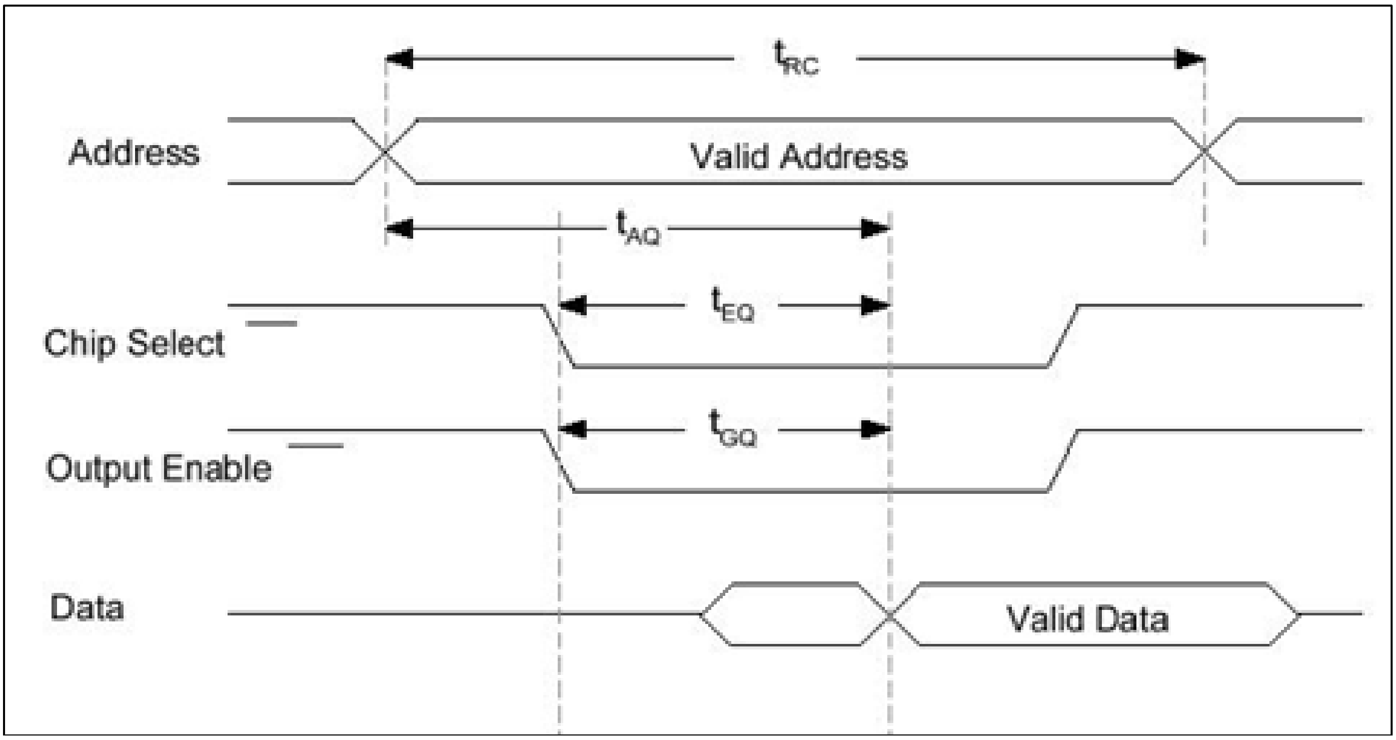

Fig 4 6T SRAM single Cell Read Timing Diagram

The write operation in an SRAM cell begins by placing the desired data on the Bit Lines. To write a logic '0', for instance, BL is set to '1' and $B\overline{L}$ to '0'; to write a logic '1', the voltages are reversed. Once the correct values are applied to the Bit Lines, the Word Line (WL) is asserted, allowing the data to be latched into the cell. This process works because the Bit Line drivers are intentionally designed to be stronger than the transistors within the cell, enabling them to override the current state of the cross-coupled inverters.

In practice, the access NMOS transistors (M5 and M6) must be stronger than the pull-down NMOS (M1 and M3) or pull-up PMOS (M2 and M4) transistors. Since PMOS transistors are inherently weaker than NMOS of the same size, a slight voltage change at one pair of inverters (e.g., M3 and M4) propagates to the opposite pair (M1 and M2), making it easier to flip their state as well. This feedback mechanism ensures that the cross-coupled inverters amplify the write process, reliably storing the intended value. Figure 4 illustrates the write operation sequence.

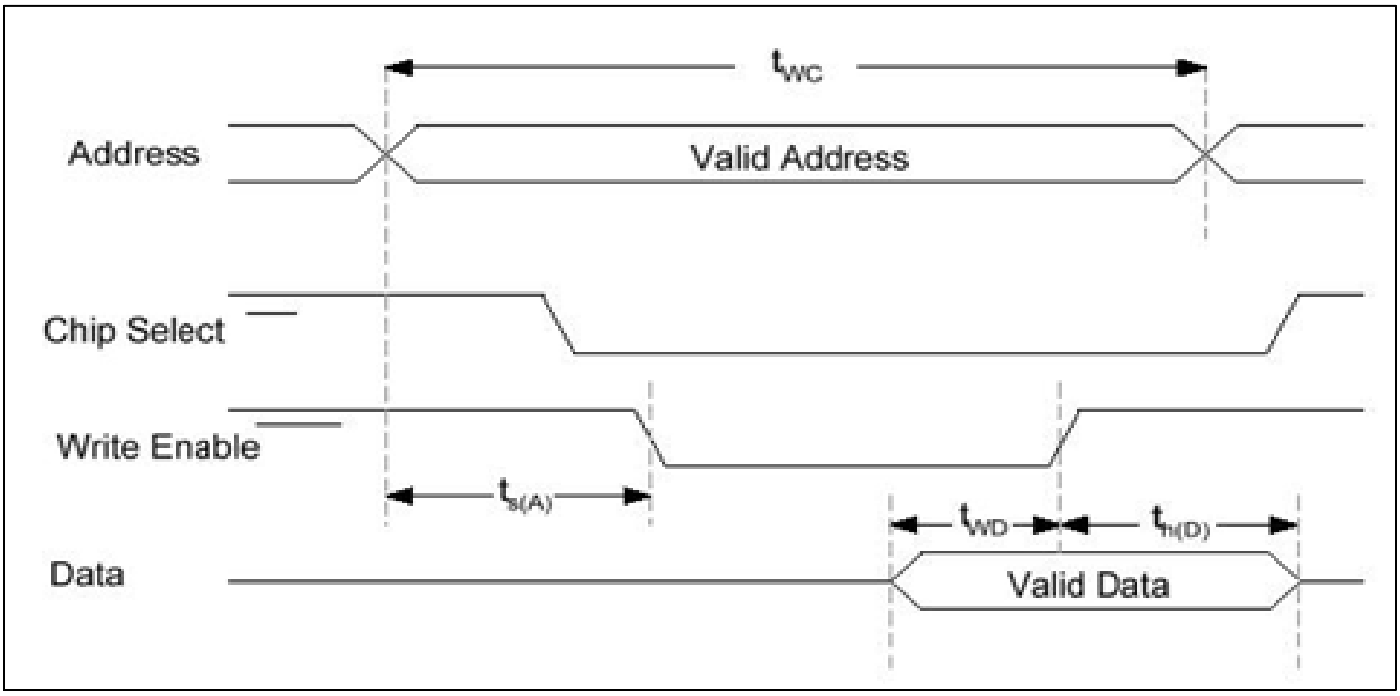

Fig 5 6T SRAM Single Cell Write Timing Diagram

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IV. IMPLEMENTATION OF 64X64 SRAM CELL

For minimizing of number of transistors, only a row decoder is used to implement 4 KB of SRAM Memory. 6x64 decoder is used to decode 64 rows as shown in Fig 5.

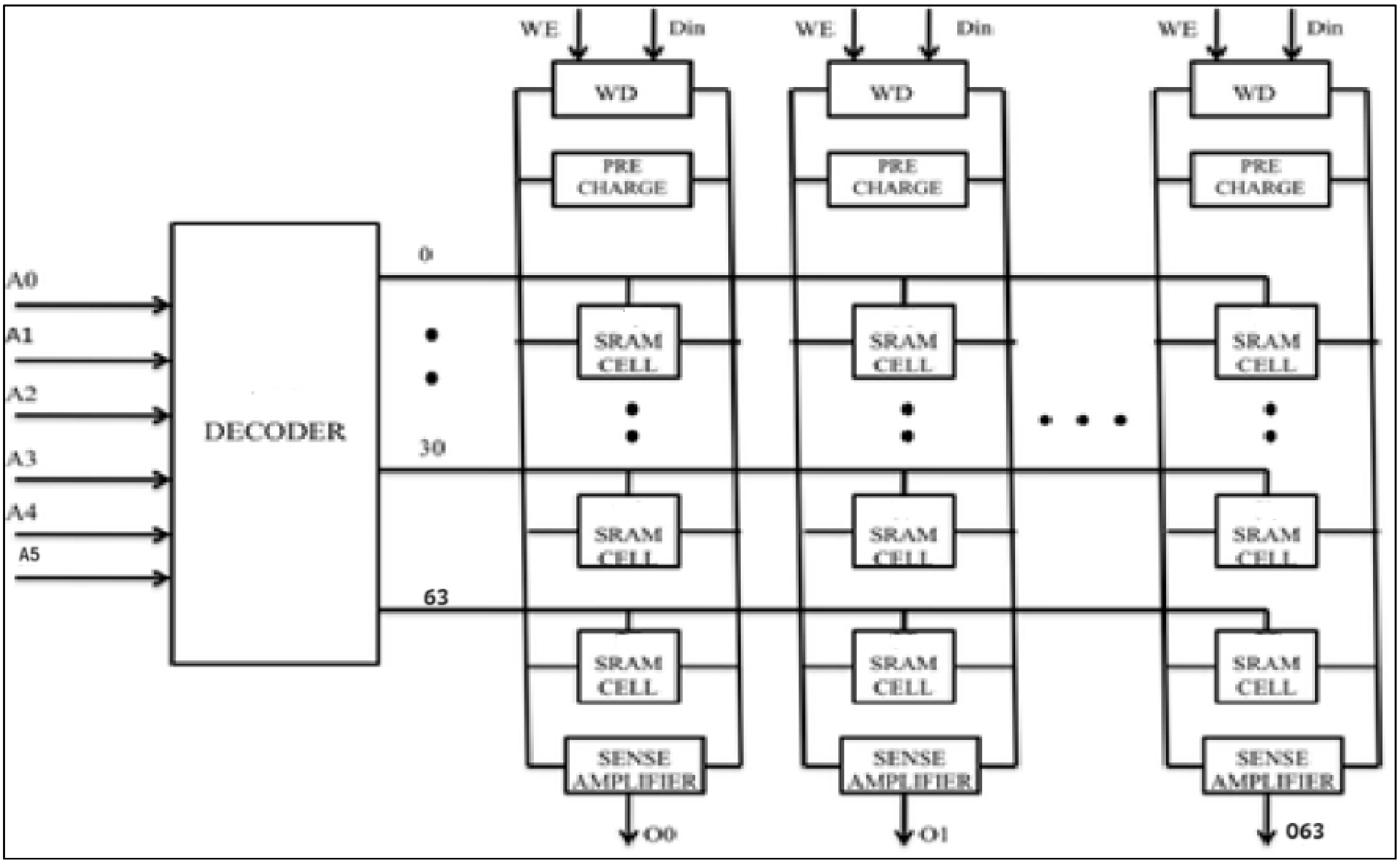

Fig 6 Proposed SRAM Memory Model

The proposed memory model is composed of several key components: the Decoder, 6T SRAM cell, Write Driver, Sense Amplifier, and Precharge Circuit. Each block plays a critical role in ensuring correct operation, and the same architecture is employed to implement a 64×64 memory array using EDA tools.

A standard 6T SRAM cell includes two cross-coupled CMOS inverters, formed by four transistors, which store the data, and two NMOS access transistors that control connectivity to the Bit Lines during read and write operations. Typically, PMOS devices are weaker than NMOS devices, so the NMOS pull-down transistors dominate during read operations. Proper transistor sizing is essential to maintain both read stability and write ability.

Before a read operation, the precharge circuit raises both Bit Lines (BL and $B\overline{L}$) to the supply voltage (VDD), establishing equal initial conditions. This precharging ensures faster and more reliable reads, reduces sensing errors, and lowers overall power consumption. Precharge is generally implemented using PMOS transistors controlled by a precharge enable signal.

During read operations, the Sense Amplifier detects the small voltage difference between BL and $B\overline{L}$ and amplifies it to a full logic level. This allows rapid and accurate data retrieval, supports low-voltage swing operation for improved power efficiency, and enhances noise margins through differential amplification. Common Sense Amplifier designs include differential latch-type and current mirror-based configurations.

The Word Line Driver is responsible for activating the appropriate Word Line based on the decoded row address. It must provide sufficient drive strength to switch long, capacitive Word Lines efficiently, fully enable the access transistors, and ensure that only one Word Line is active at any given time to prevent read/write conflicts.

V. RESULTS & DISCUSSION

The two main inputs to the write driver are the data input signal (D) and the Word Enable signal. When the Word Enable signal is asserted (typically active high), the circuit is activated, allowing the data input to determine the logic levels on the bit lines.

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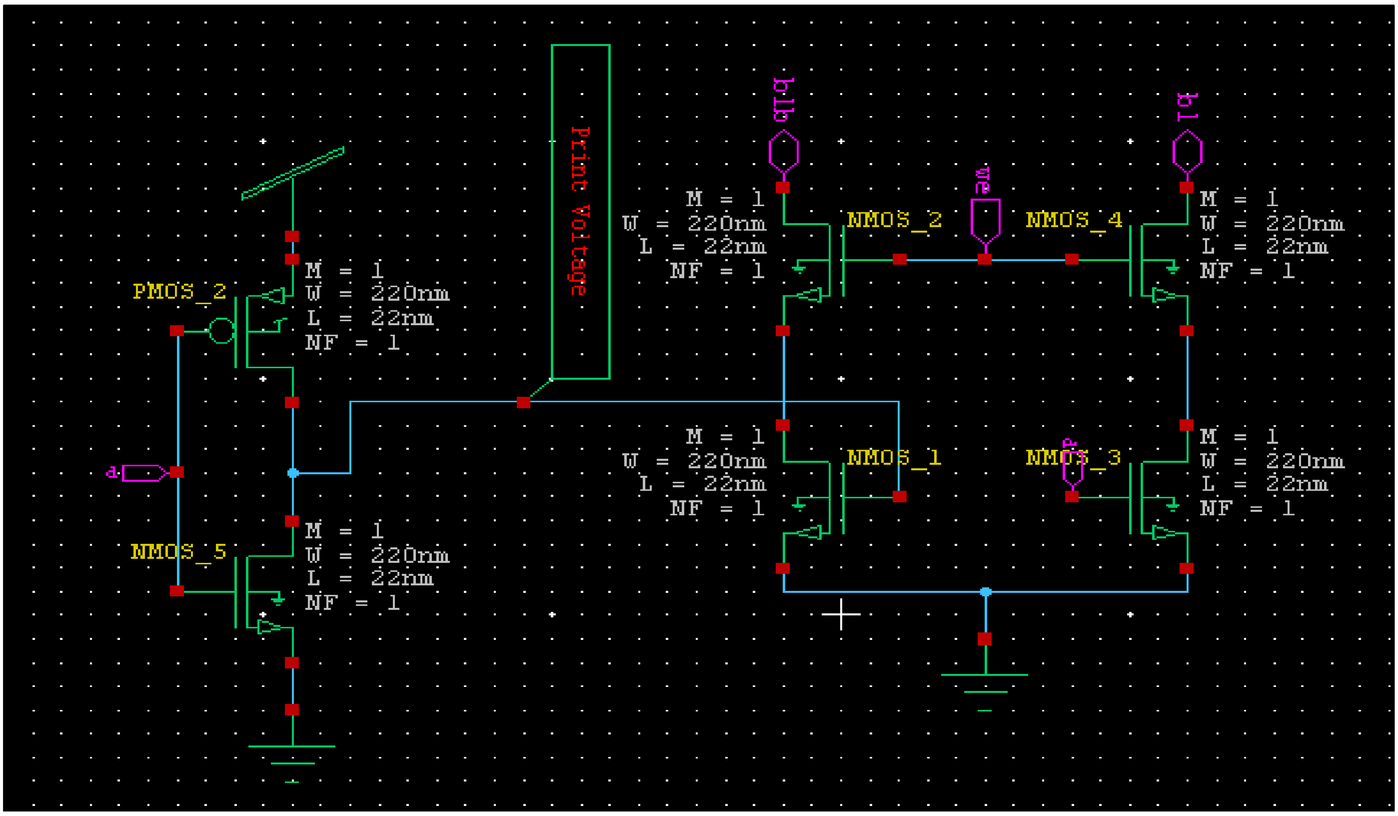

Fig 7 Write Driver Circuit

The simulation concludes with the. end statement, marking the end of the SPICE netlist. This testbench provides insights into the write driver's performance, energy consumption, and timing characteristics under scaled 22nm conditions.

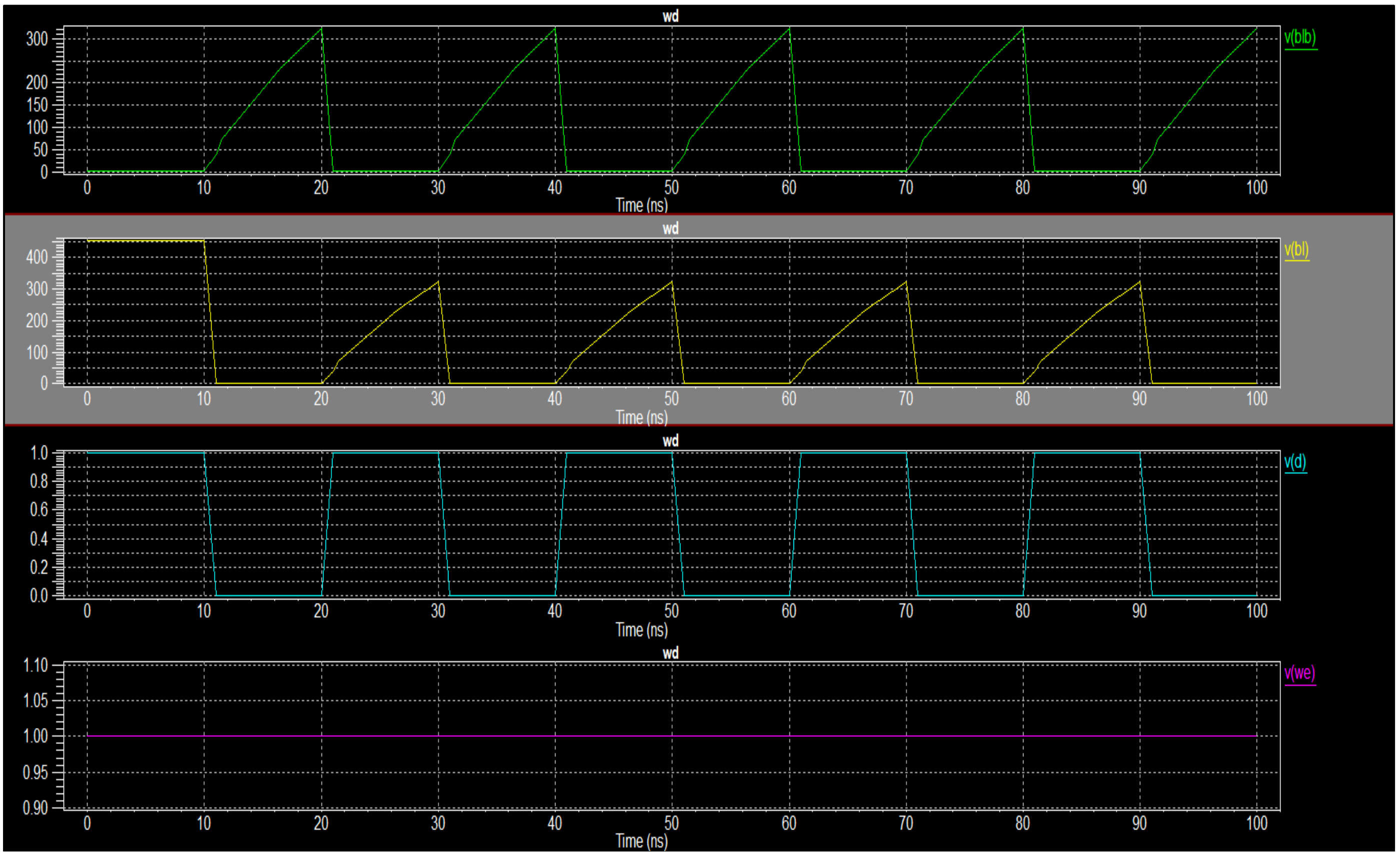

Fig 8 Write Driver Waveform

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The precharge circuit is typically implemented using three PMOS transistors—two connected between VDD and the bit lines (BL and BLB), and a third acting as a switch controlled by the 'pre' signal. This configuration ensures that both bit lines are precharged simultaneously and symmetrically, maintaining the differential nature of the read/write path.

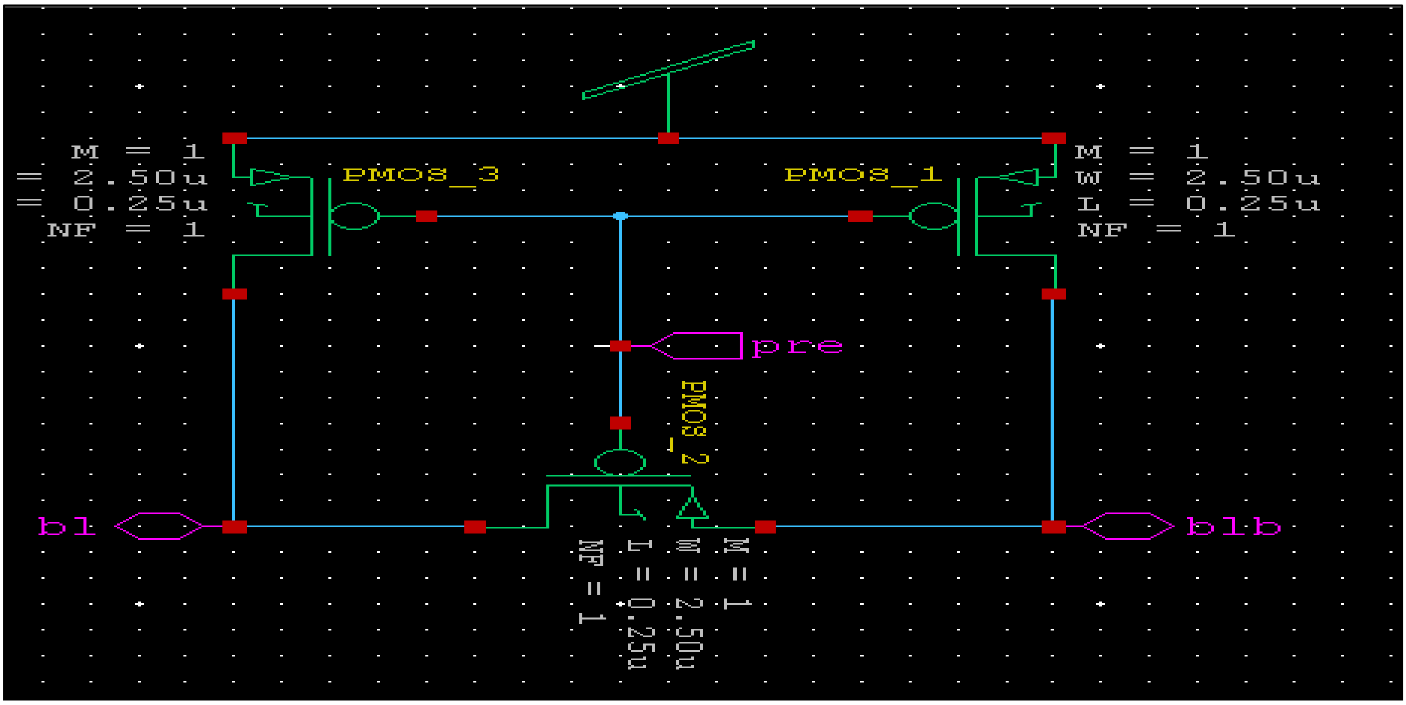

Fig 9 Precharge Circuit

This precharge mechanism is especially important in high-speed and low-power SRAM designs, as it minimizes the delay in bit line settling and reduces the chances of incorrect sensing due to noise or voltage imbalance.

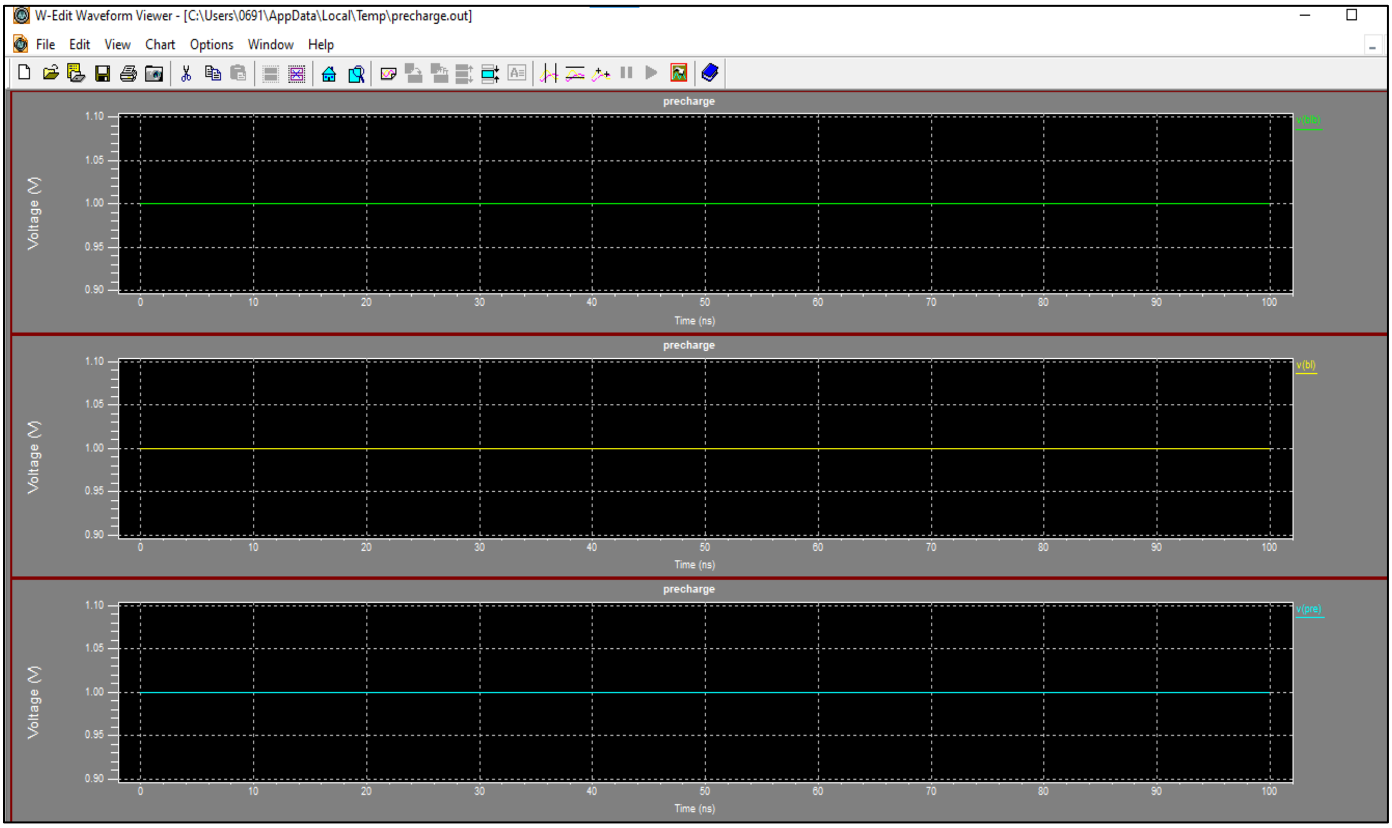

Fig 10 Precharge Circuit Waveform

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➢ *Sense Amplifier*

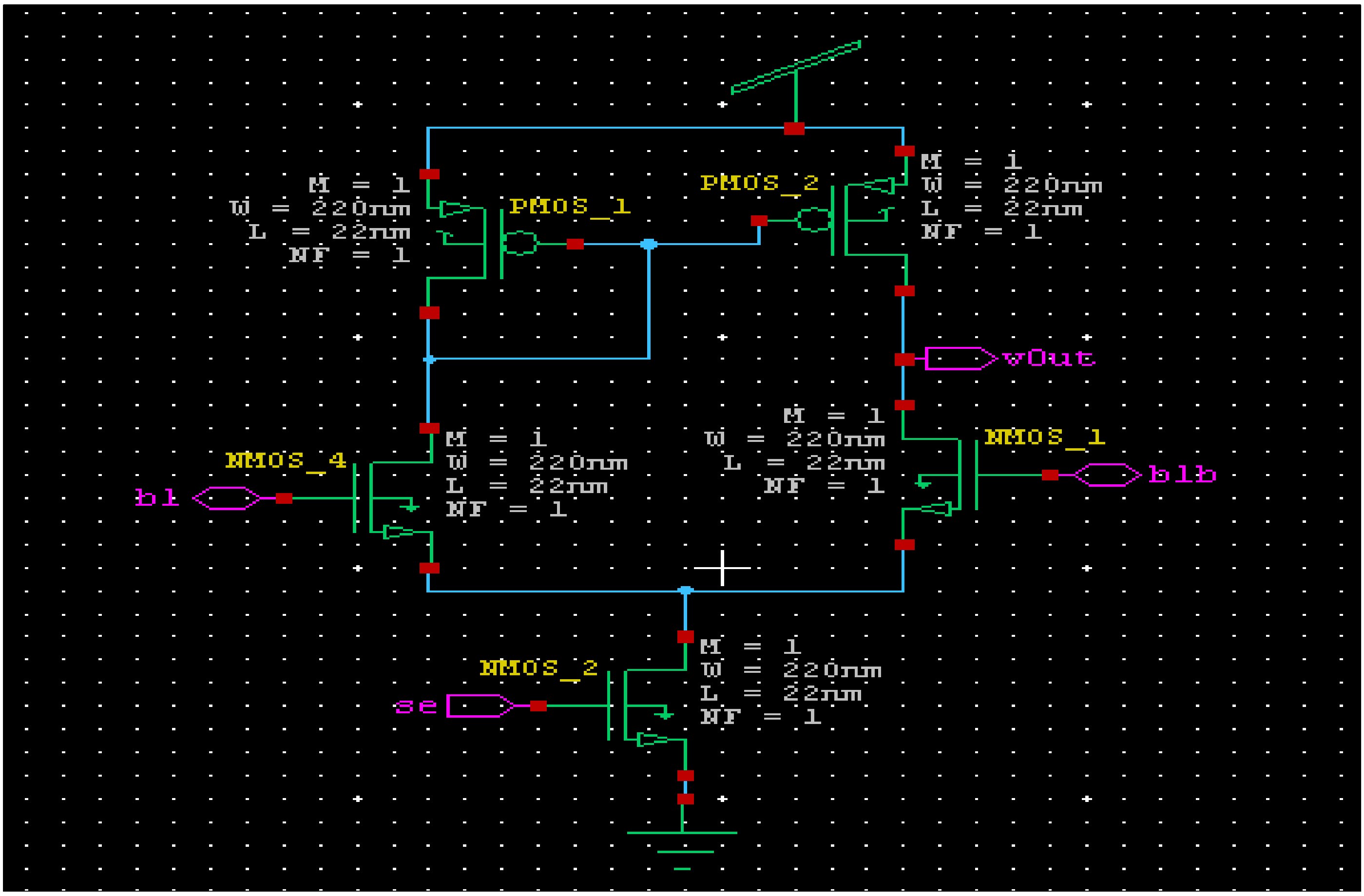

Fig 11 Sense Amplifier Circuit

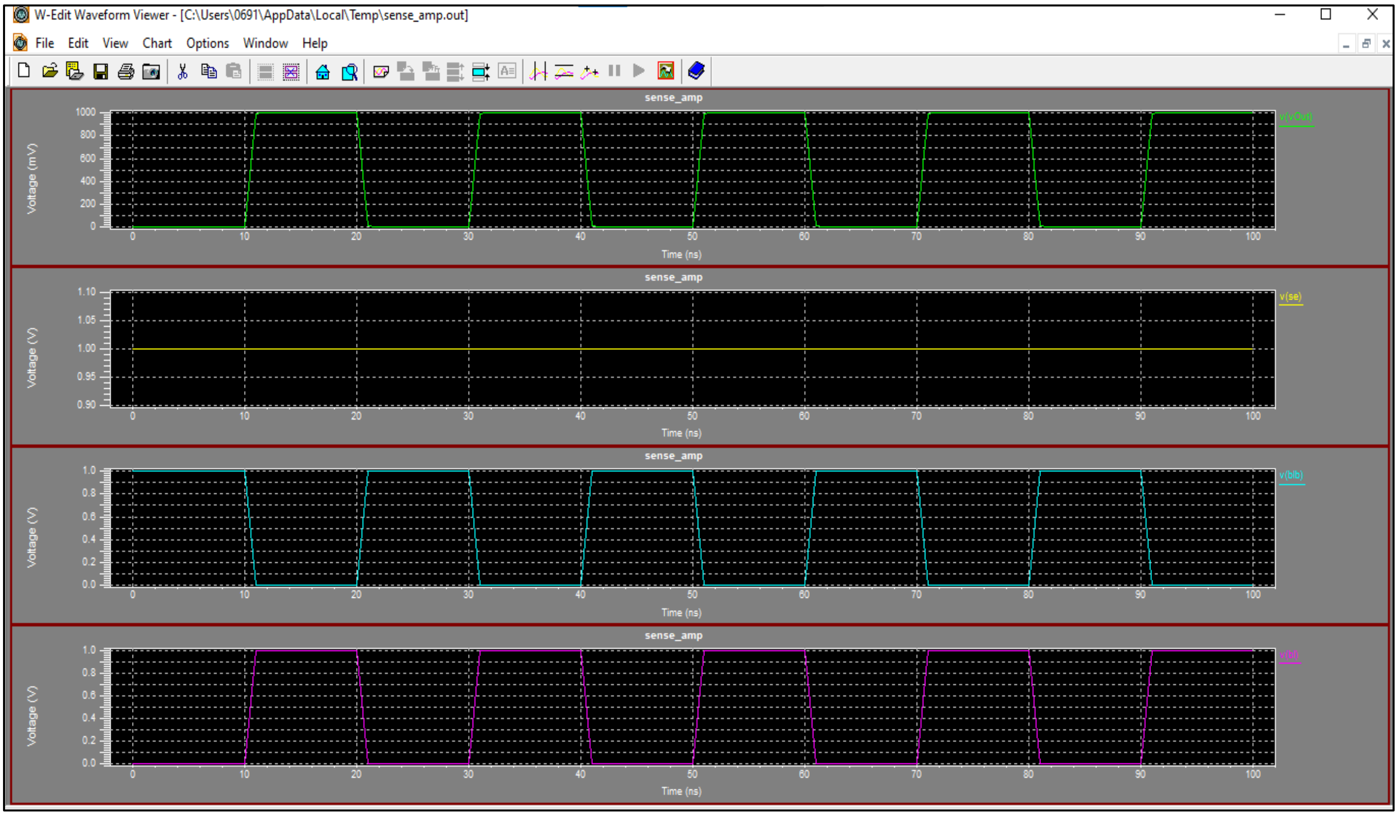

Fig 12 Sense Amplifier Waveforms

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- *6T SRAM Cell*

The simulation results of SRAM shown below and circuit operation explained section3.

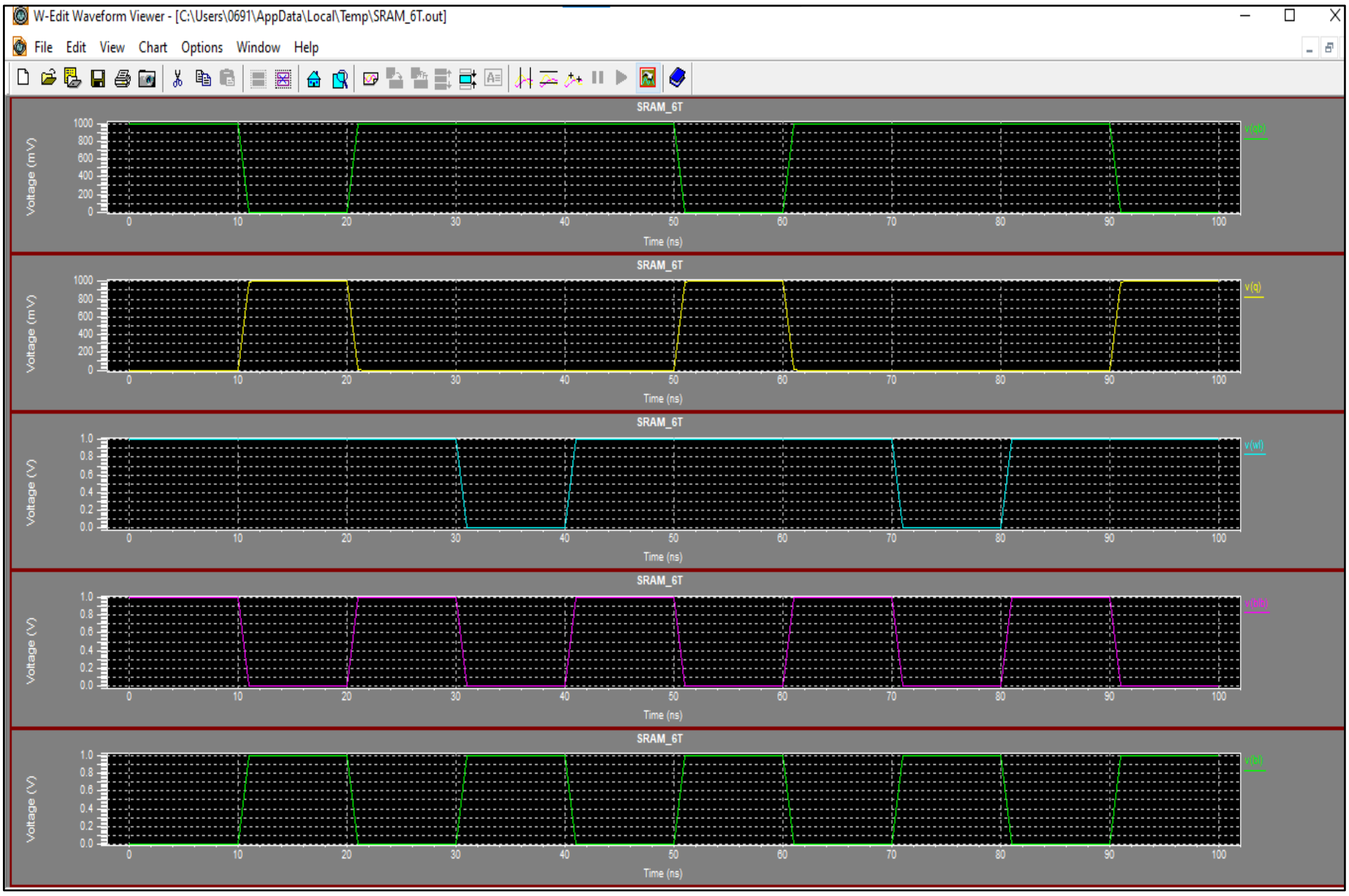

Fig 13 SRAM 6T Circuit Waveforms

- *Integrated SRAM Cell*

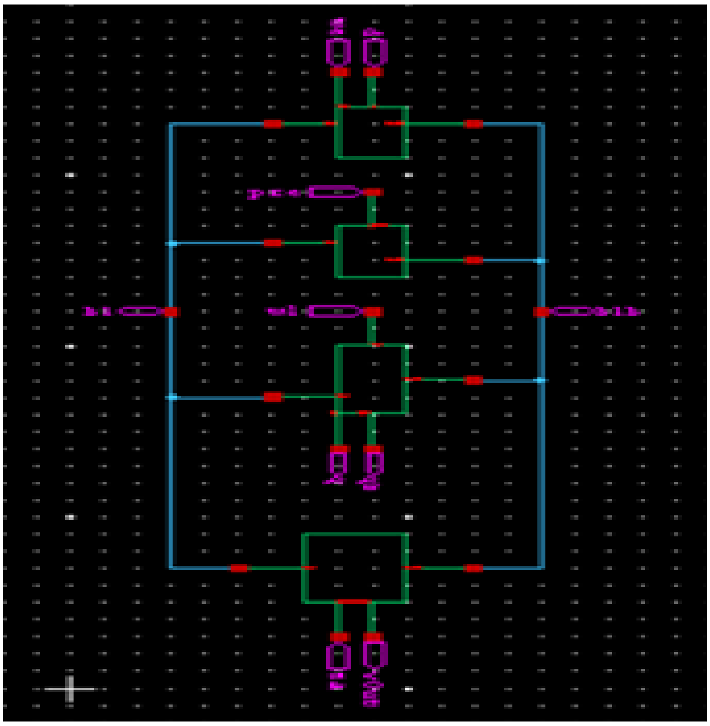

Fig 14 Integrated SRAM Circuit

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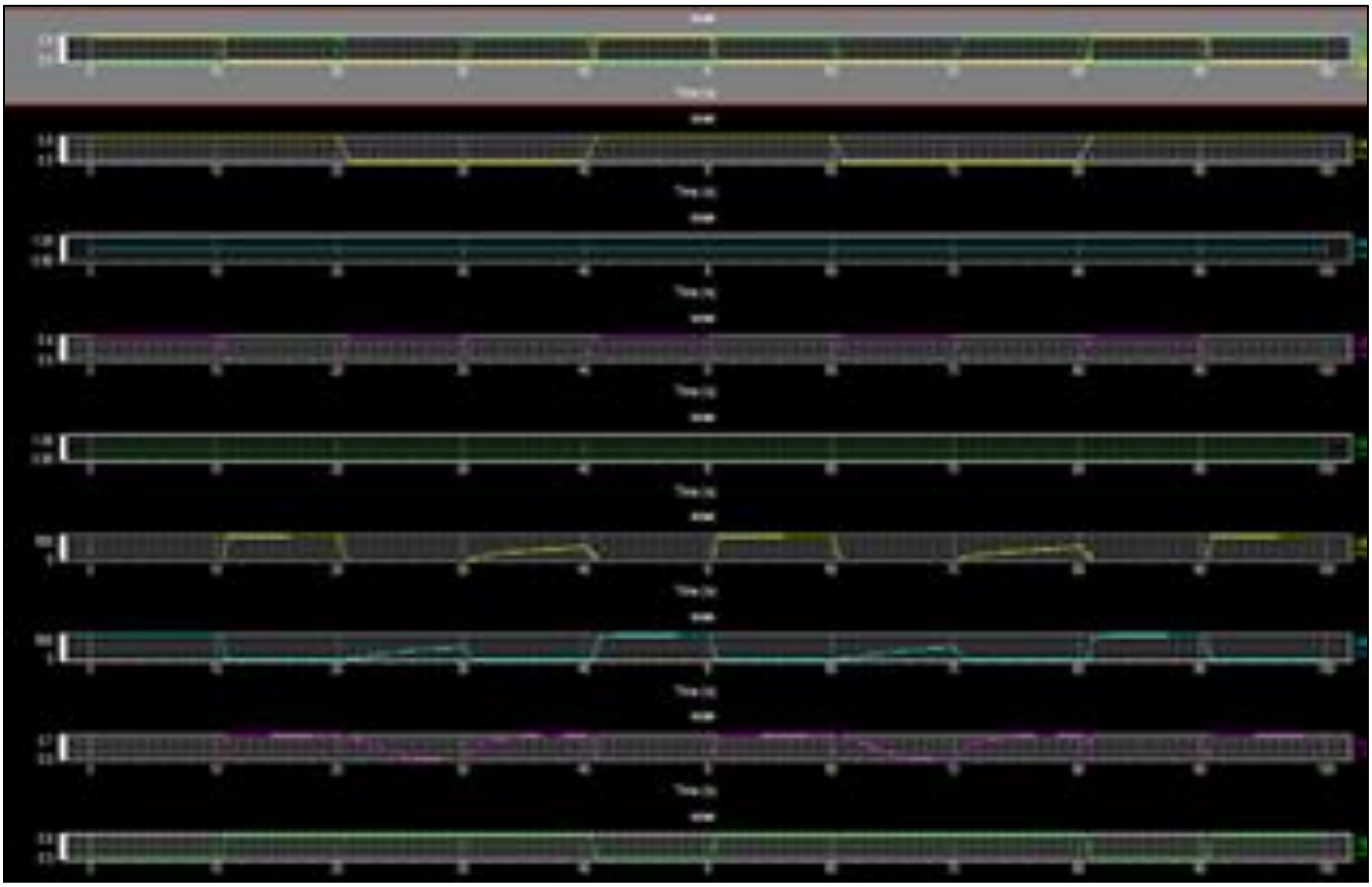

Fig 15 Integrated SRAM Circuit Waveforms

➢ *x 64 Decoder*

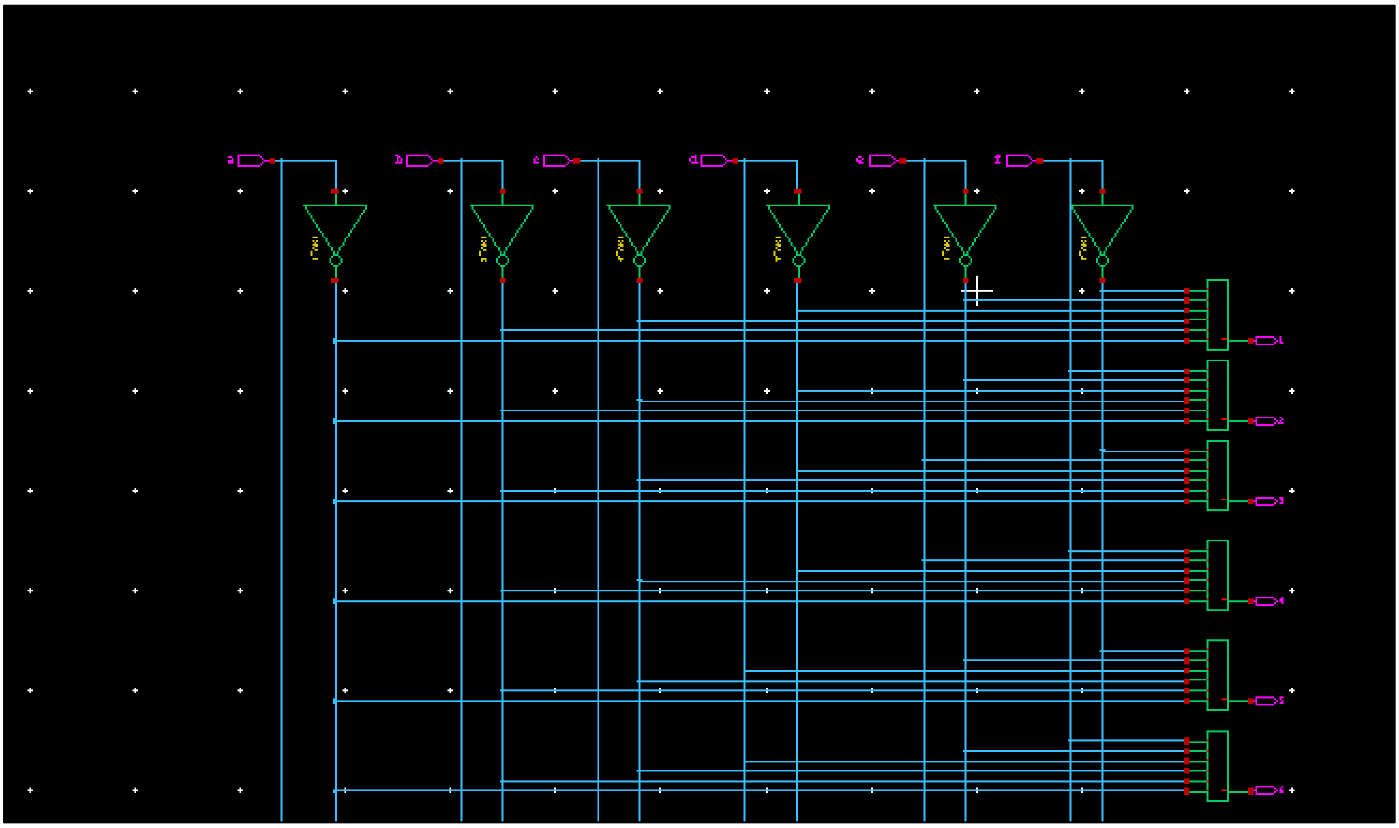

Fig 16 6x64 Decoder Zoom Circuit

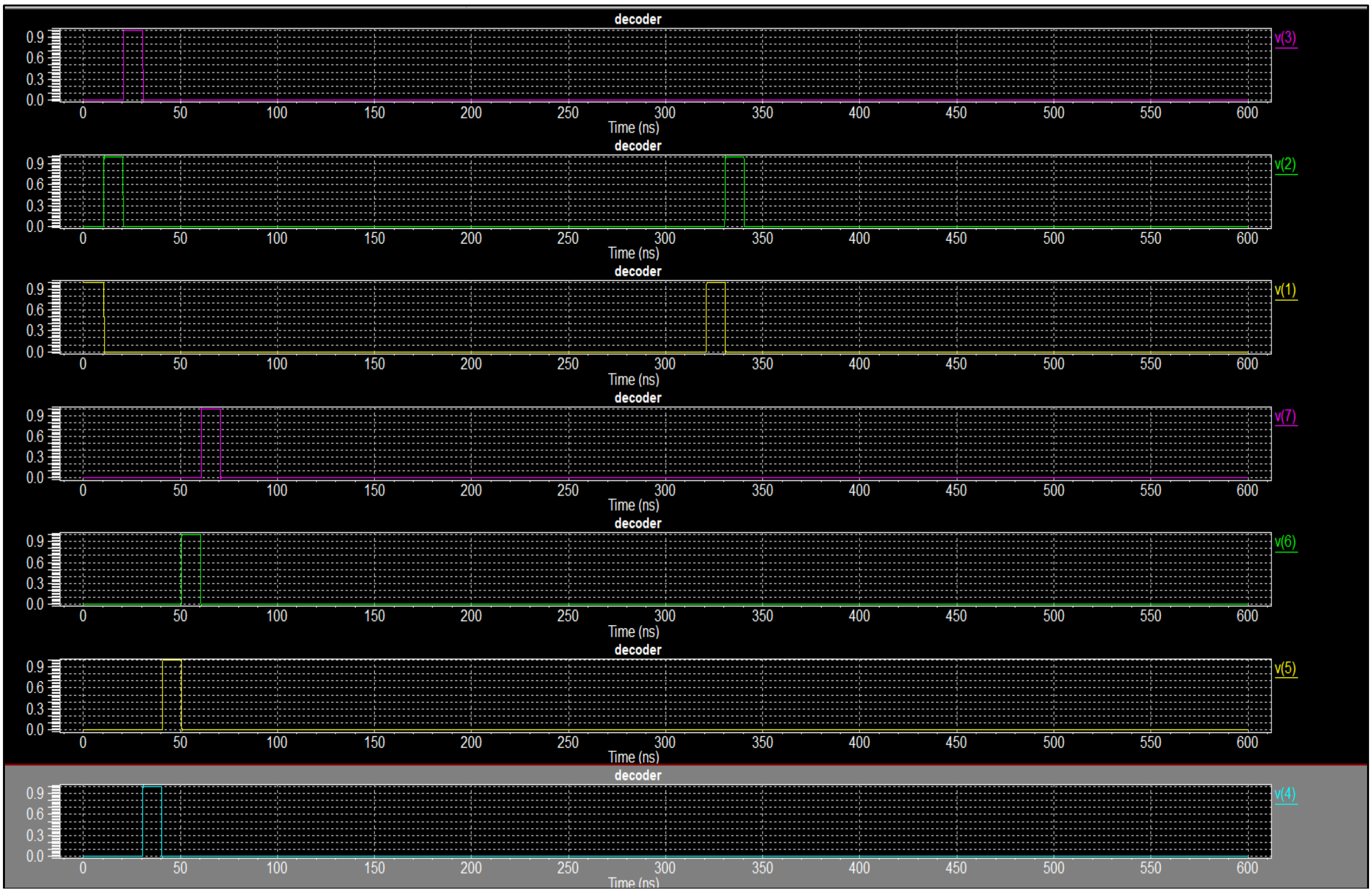

Fig 17 6x64 Decoder Waveforms

➢ *1x64 SRAM Array*

Consist of one Row with 64 columns to store 64 bits in one row.

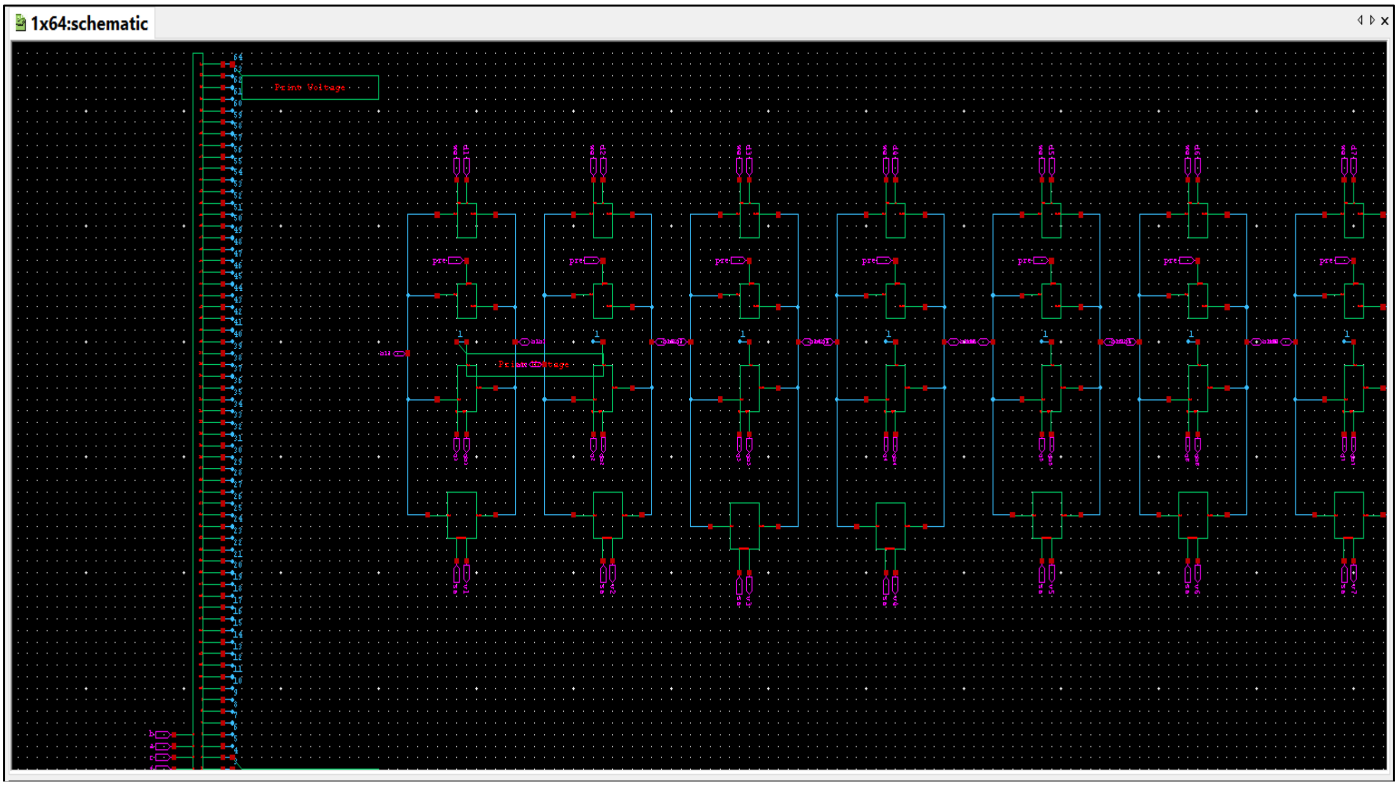

Fig 18 1x64 SRAM Array Circuit Zoom

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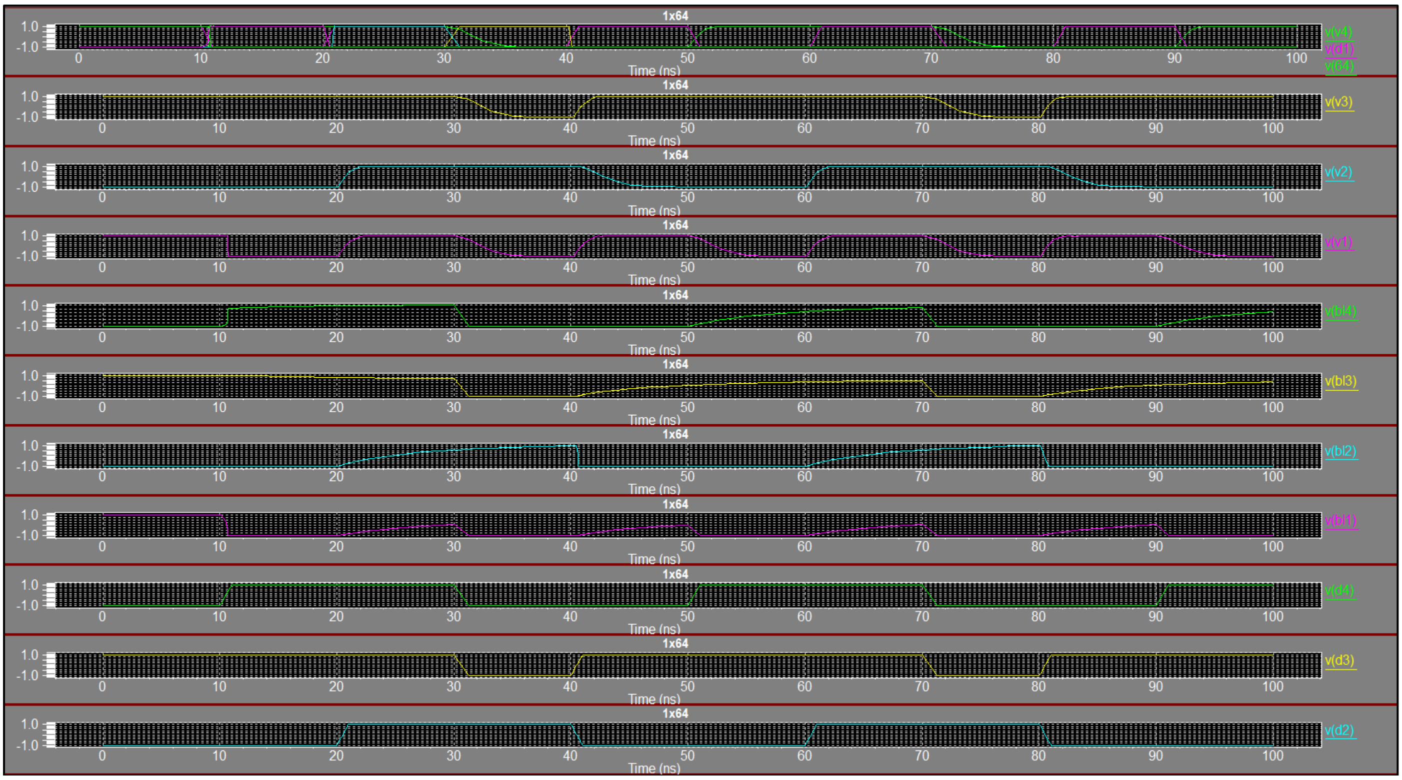

Fig 19 1x64 SRAM array circuit waveforms

VI. CONCLUSION

This study focuses on the design and evaluation of a 1 KB SRAM array constructed using 6T SRAM cells in CMOS technology. The memory array, organized for bit-level storage, provides a total capacity of 1024 bits. The design emphasizes low power consumption, reduced leakage currents, and compact cell dimensions.

Simulation and analysis highlighted notable differences in power usage between read and write operations. The 6T SRAM cells employed in the array exhibited minimal leakage, contributing to overall energy efficiency. Key performance metrics, including power dissipation during read and write cycles, were benchmarked against previous designs, showing measurable improvements. The proposed memory array was implemented and verified using the Tanner EDA tool, based on a 22 nm CMOS process.

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