ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/26jul1399

Comparative Experimental Evaluation of Three Digitally Controlled Boost PFC Topologies for a BLDC Motor Drive

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Publication Date: 2026/08/01

Abstract: Power-factor correction (PFC) is essential in modern motor-drive systems to comply with harmonic-current limits (e.g., IEC 61000-3-2), reduce input-current distortion, and lower reactive-power burden on the supply. This paper presents a fair head-to-head experimental comparison of three boost-based active PFC front ends for a brushless DC (BLDC) motor drive: (i) classic boost PFC, (ii) bridgeless boost PFC, and (iii) two-phase interleaved boost PFC. All three converters are digitally controlled using an outer DC-bus voltage loop and an inner input-current loop on the same hardware platform, and all three are tested with the same BLDC motor, the same load profile, and the same instrumentation, so that the observed differences reflect only the topology change. Twenty-four operating points are recorded at a fixed motor speed of 3,950 RPM with shaft torque varied from no-load to 3.5 N.m using a HIOKI smart power analyzer. Across the load range, the measured mean power factor improves from 0.9255 (Classic) to 0.9385 (Bridgeless) and 0.9501 (Interleaved); the peak measured reactive power drops from 905 VAR (Classic) to 790 VAR (Bridgeless) and 664 VAR (Interleaved), corresponding to a 26.6 per cent reduction in worst-case reactive-power demand from Classic to Interleaved. A qualitative component-count and complexity comparison is also presented to support topology selection in practical motor-drive design.

Keywords: *Power-Factor Correction (PFC); Classic Boost PFC; Bridgeless PFC; Interleaved PFC; BLDC Motor Drive; Digital Control; Reactive Power; Power Quality; Experimental Comparison.*

How to Cite: Sachin Rathod; Mahesh Jivani; Kalpesh Gajera (2026) Comparative Experimental Evaluation of Three Digitally Controlled Boost PFC Topologies for a BLDC Motor Drive. *International Journal of Innovative Science and Research Technology*, 11(7), 2299-2305. https://doi.org/10.38124/ijisrt/26jul1399

I. INTRODUCTION

The widespread adoption of variable-speed motor drives in domestic appliances, electric vehicles, industrial pumps, and HVAC systems has increased the importance of power-quality compliance at the AC input of such drives. Diode-bridge rectifiers followed by bulk-capacitor filters, the most common front-end in low-cost drives, draw highly distorted, peaked input currents. The resulting low displacement-and-distortion power factor reduces grid utilization, increases I^2R losses in cabling and transformers, and can lead to non-compliance with international harmonic-emission standards such as IEC 61000-3-2 [1].

Active power-factor correction (PFC) addresses these issues by shaping the input current to be sinusoidal and in phase with the supply voltage while regulating a stable DC bus for the downstream motor-drive inverter [2][4]. Among the many active PFC topologies surveyed in [5], [6], boost-based variants are the most widely adopted because they provide continuous input current, accept a universal AC input range, and admit a relatively simple dual-loop control structure. The three most widely referenced single-phase boost variants are the classic boost PFC, the bridgeless boost PFC [7], and the interleaved boost PFC [8].

Each of these three topologies has been studied individually in literature, and theoretical comparisons across them have appeared in several survey papers [10] [12]. However, head-to-head experimental comparisons under strictly matched conditions; same hardware controller, same control structure, same motor, same load profile, and same instrumentation, remain comparatively rare in the published literature, particularly in the context of small-to-medium-power BLDC motor drives. Most reported results combine measurements from different platforms, different motors, or different control firmware, which makes the published numbers difficult to compare directly.

➢ *The Contributions of this Paper are Threefold:*

- A fair head-to-head experimental comparison of three digitally controlled boost PFC topologies: classic, bridgeless, and two-phase interleaved, implemented on the

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/26jul1399

same controller hardware and tested on the same BLDC motor drive under identical load conditions.

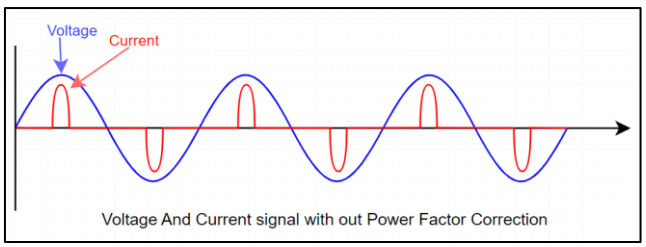
- Quantitative power-quality metrics: power factor, apparent power, RMS input current, and reactive power; extracted at eight load points per topology, providing a directly comparable dataset of 24 measurements suitable for design decisions.
- A practical component-count and complexity comparison that supports topology selection in real-world drive design, including a discussion of the qualitative cost and control-effort trade-offs.

The remainder of this paper is organized as follows. Section II discusses the importance of power factors in motor-drive systems. Section III reviews the principal sources of power loss in boosting PFC stages. Section IV presents the digital control structure common to all three topologies. Section V describes the implemented PFC topologies. Section VI details the experimental setup, and Section VII reports the measured results, including the comparison of PF, RMS current, and reactive power. Section VIII presents the qualitative component-count comparison and practical guidance for topology selection. Section IX concludes the paper and outlines future directions.

II. IMPORTANCE OF POWER FACTOR IN MOTOR-DRIVE SYSTEMS

In a motor-drive front-end, the power factor (PF) is a key indicator of how effectively input apparent power is converted into useful real power delivered to the DC bus and ultimately to the motor. For a single-phase system, PF is defined as the ratio of real power P to apparent power $S = V \cdot I$, where V and I are the RMS line voltage and current respectively. A low PF directly increases the RMS line current for the same active power, raising I^2R losses in supply cables, EMI filters, transformers, and switching devices. Poor input-current quality also stresses electrolytic capacitors, increases device heating, and may produce DC-bus ripples that translates into torque ripples and audible noise in the BLDC drive [9].

Equivalently, low PF means that the supply must deliver a large reactive component $Q = \sqrt{(S^2 - P^2)}$ that performs no useful work but must still be supported by the upstream electrical infrastructure. Utility tariff structures often penalize loads with low PF because the reactive component reduces the active-power capacity of the distribution network. An active PFC stage shapes the line current to be nearly sinusoidal and in phase with the supply voltage, reducing both total harmonic distortion (THD) and reactive-power demand, improving compliance with IEC 61000-3-2 [1], and improving utilization of the installed electrical infrastructure.



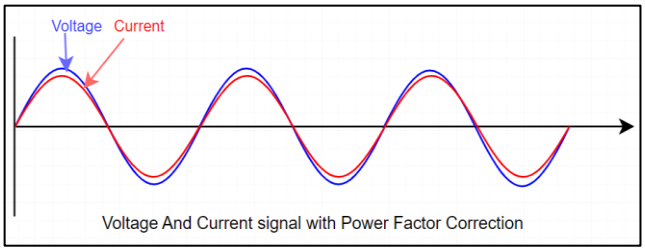


Fig 1 Phase Relationship Between Voltage and Current

III. SOURCES OF POWER LOSS IN BOOST PFC STAGES

➢ *Switching Losses*

Switching losses originate from the finite turn-on/turn-off transition times of the MOSFET (or IGBT), the simultaneous overlap of voltage and current during commutation, and the gate-drive energy dissipated each cycle. They scale approximately linearly with switching frequency. Higher switching frequency reduces inductor and capacitor size but increases switching losses, requiring careful design trade-offs [2], [3].

➢ *Conduction Losses*

Conduction losses arise from the on-state resistance of the MOSFET ($R_{DS,on}$), the forward voltage drop of the diodes, and the DC and AC copper losses of the boost inductor. In the classic boost PFC, the input diode bridge contributes additional conduction loss because two bridge diodes conduct in series for each half-cycle. Bridgeless topologies were introduced specifically to eliminate the bridge and reduce these losses [7], [10].

➢ *Magnetic Core Losses*

Inductor core losses include hysteresis and eddy-current loss, and depend on flux-density swing, switching frequency, and core material. Proper inductor design (core material, gap, winding arrangement) is essential to limit core temperature rise at high switching frequencies, especially in interleaved configurations where multiple inductors share thermal space.

➢ *Reverse-Recovery Losses*

In hard-switched boost converters, the reverse-recovery current of the freewheeling diode produces a short-duration high current spike at switch turn-on, increasing both losses and EMI. Fast-recovery silicon diodes or wide-bandgap (SiC) Schottky diodes are typically used to mitigate this effect, particularly at higher switching frequencies.

➢ *Digitally Controlled Boost PFC: Control Structure*

All three implemented topologies share a common dual-loop digital control structure, illustrated in Fig 2. An outer voltage loop regulates the DC-bus voltage v_o to a reference V_{ref} using a discrete-time PI controller. The output of the voltage loop, scaled by a normalized version of the rectified input voltage, generates the instantaneous reference for the current i_{ref}. This ensures the desired input current waveform is in phase with the input voltage. An inner current loop, also implemented as a PI controller, forces the measured inductor (or input) current to follow i_{ref} by adjusting the PWM duty cycle of the boost switch [13], [14].

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/26jul1399

The control loop is executed on an embedded controller TMPM4KLFYAUG with PWM frequency f_sw = 40 kHz, voltage-loop bandwidth in the tens of Hz, and current-loop bandwidth approaching one tenth of the switching frequency. ADC sampling is synchronized with the PWM carrier to minimize switching-noise pickup. For bridgeless topology, an additional zero-crossing detector identifies the AC line polarity and selects which switch is actively modulated during each half-cycle.

IV. IMPLEMENTED PFC TOPOLOGIES

➢ *Classic Boost PFC*

The classic boost PFC, shown in Fig 2, consists of a single-phase diode-bridge rectifier followed by a boost converter (inductor L, switch S, diode D, output capacitor C). The control structure shapes the rectified input current to a half-sinusoid in phase with the rectified input voltage. The topology uses only a single switching device, making it cost-effective for small-to-medium-power motor drives. Its main drawbacks are the conduction loss of the input diode bridge — two bridge diodes are always in series with the line — and the resulting limit on achievable efficiency at higher load currents [11].

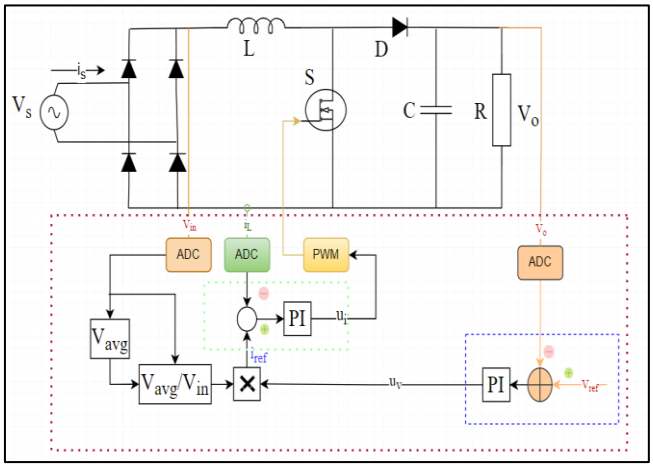


Fig 2 Classic Boost PFC Power Stage with Dual-Loop Digital Control (Outer DC-Bus Voltage Loop, Inner Input-Current Loop)

➢ *Bridgeless Boost PFC*

The bridgeless boost PFC (Fig 3) eliminates the input diode bridge by using a configuration in which two boost stages — each comprising a switch (S_1 or S_2), a diode (D_1 or D_2), and a shared or split inductor — operate alternately during the positive and negative half-cycles of the AC line. A zero-crossing or line-polarity detection block in the digital controller identifies which half-cycle is active and enables only the relevant switch [7], [10]. Removing the bridge reduces the number of series-conducting devices in the current line path and lowers conduction losses. The trade-offs are increased control complexity, higher common-mode EMI (because the line-to-ground voltage of the converter is no longer clamped by the bridge), and the need for floating gate drivers for at least one of the two switches.

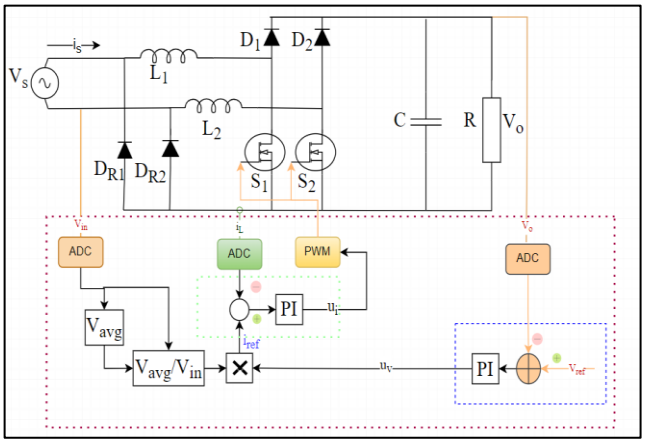


Fig 3 Bridgeless Boost PFC: Two Boost Stages Share the DC Bus and are Activated by Line-Polarity Detection

➢ *Two-Phase Interleaved Boost PFC*

The two-phase interleaved boost PFC (Fig 4) places two boost converters in parallel between a common rectifier and the DC bus, with their PWM signals phase-shifted by 180° [8], [12]. Each phase carries approximately half of the total input current. Because the inductor current ripples of the two phases are partially cancelled at the input node, the net input-current ripple — and therefore the EMI-filter requirement — is reduced. Interleaving also reduces RMS current stress in the bulk capacitor and can improve transient response. The trade-off is the doubling of inductors and switching devices, and a slightly more complex digital control because two current loops (one per phase) must be coordinated.

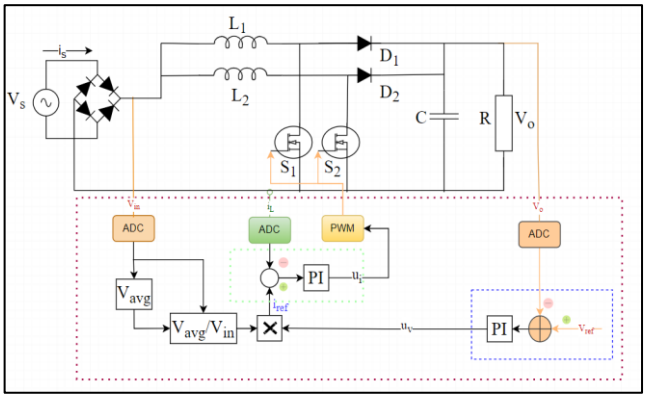


Fig 4 Two-Phase Interleaved Boost PFC: Phase-Shifted PWM (180°) Reduces Input-Current Ripple

➢ *Experimental Setup*

The three PFC front ends were tested with the same BLDC motor drive at a fixed shaft speed of 3,950 RPM. Mechanical loading was provided by an adjustable load coupled to the motor shaft, and the shaft torque was varied between no-load (≈ 0 N·m) and approximately 3.5 N·m. Eight operating points were recorded for each topology, giving a total of 24 measurements. The AC input voltage, RMS input current, real input power, and displacement-plus-distortion power factor were measured directly with a HIOKI smart power analyzer. Apparent power $S = V \cdot I$ and reactive power $Q = \sqrt{(S^2 - P^2)}$ were computed from these primary measurements. The same supply, motor, controller hardware, and load profile were used across all topologies, and only the PFC power stage and

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/26jul1399

its associated control firmware were changed between tests, so that the comparison reflects intrinsic topology differences rather than measurement-environment differences.

Hardware parameters: Classic PFC boost inductor L = 150 µH; Bridgeless PFC boost inductor L = 30 µH; Interleaved PFC boost inductor L = 75 µH; bulk DC-bus capacitor C = 550 µF / 450 V; switching frequency f_sw = 40 kHz; DC-bus reference V_ref = 380 V; AC supply 230 V / 50 Hz; motor: BLDC (5 kW, 16-pole).

This study deliberately scopes its measurements to power-factor and reactive-power behaviour. Total harmonic distortion (THD), conducted EMI, and PFC-stage-only efficiency (which would require a separate DC-bus power measurement) were not characterized in this work and are explicitly addressed as future work in Section IX.

V. EXPERIMENTAL RESULTS

Tables 1, 2, and 3 present the measured operating points for the Classic, Bridgeless, and Interleaved boost PFC topologies, respectively. Figures 5, 6, and 7 plot, respectively, the measured power factor, the reactive power, and the RMS input current as functions of shaft torque. The summary statistics for each topology are given in Table 4.

Table 1 Measured Operating Points — Classic Boost PFC (BLDC at 3,950 RPM)

Torque (N·m)	Vac (V)	Iin (A)	P_in (W)	Q (VAR)	PF
0.000	228.35	3.791	—	348	0.9164
0.588	227.23	4.823	1019	405	0.9294
1.108	226.63	5.484	1159	449	0.9322
1.500	225.87	6.117	1292	489	0.9352
2.020	224.48	7.270	1518	597	0.9304
2.413	223.60	8.075	1673	678	0.9263
2.932	222.64	9.052	1854	788	0.9202
3.285	221.83	10.057	2039	905	0.9140

Table 2 Measured Operating Points — Bridgeless Boost PFC (BLDC at 3,950 RPM)

Torque (N·m)	Vac (V)	Iin (A)	P_in (W)	Q (VAR)	PF
0.000	224.95	3.997	835	335	0.9281
0.608	223.39	5.517	1152	437	0.9346
1.167	222.27	6.419	1340	493	0.9393
1.667	221.05	7.406	1536	566	0.9384
2.099	220.54	8.361	1738	619	0.9427
2.334	220.11	9.078	1884	667	0.9426
2.766	219.29	9.888	2028	729	0.9418
3.305	218.27	10.630	2181	790	0.9402

Table 3 Measured Operating Points — Two-Phase Interleaved Boost PFC (BLDC at 3,950 RPM)

Torque (N·m)	Vac (V)	Iin (A)	P_in (W)	Q (VAR)	PF
0.010	229.19	3.756	809	292	0.9403
0.402	227.18	5.605	1201	422	0.9434
1.216	226.26	6.545	1376	496	0.9424
1.481	225.05	7.405	1578	537	0.9467
2.030	223.92	8.338	1776	576	0.9511
2.373	223.24	9.115	1935	603	0.9550
2.893	222.68	9.942	2102	623	0.9595
3.501	221.75	10.992	2321	664	0.9621

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/26jul1399

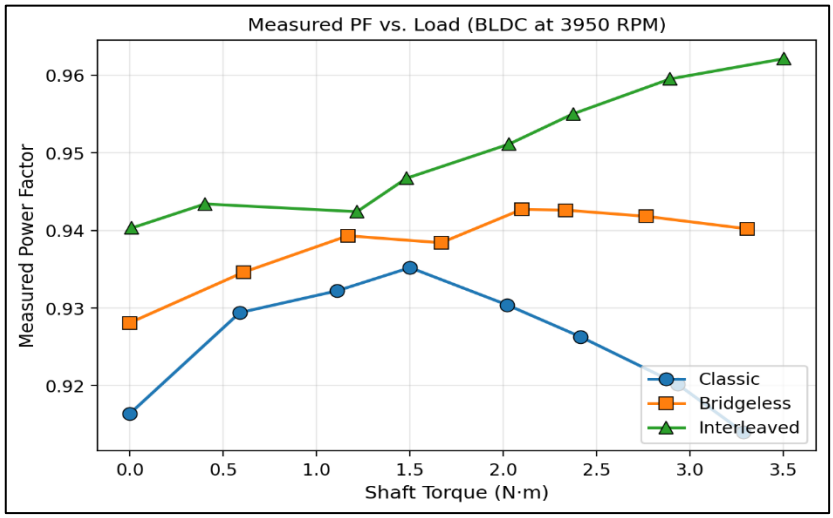


Fig 5 Measured Power Factor Versus Shaft Torque for the Three PFC Topologies

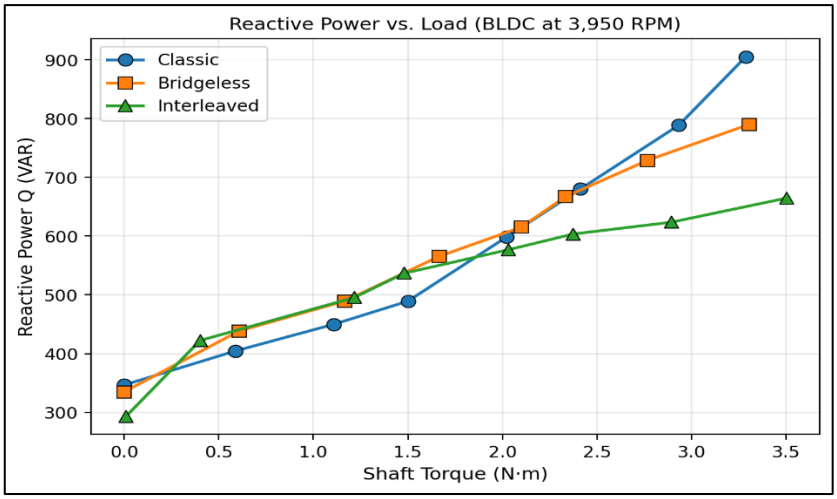


Fig 6 Computed Reactive Power Q Versus Shaft Torque for the Three PFC Topologies

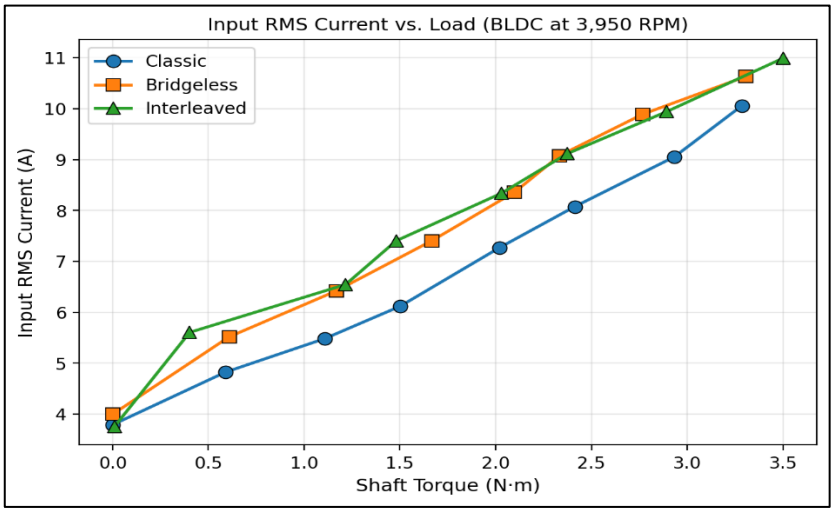


Fig 7 Measured RMS Input Current Versus Shaft Torque for the Three PFC Topologies

Table 4 Summary of Measured Power-Quality Performance per Topology

Topology	Min PF	Max PF	Mean PF	Max Q (VAR)	Q Reduction vs Classic
Classic Boost PFC	0.9140	0.9352	0.9255	905	—
Bridgeless Boost PFC	0.9281	0.9427	0.9385	790	12.7 %
Interleaved Boost PFC	0.9403	0.9621	0.9501	664	26.6 %

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➢ *Three Trends are Evident from the Experimental Data:*

- For every load level, the measured power factor follows the consistent ordering Interleaved > Bridgeless > Classic. The mean PF rises from 0.9255 (Classic) to 0.9385 (Bridgeless) and 0.9501 (Interleaved), an absolute improvement of approximately 0.025 between the two extremes.
- The Classic topology shows a non-monotonic PF profile that peaks near mid-load (≈ 1.5 N·m) and then decreases at high load. This is consistent with the growing diode-bridge conduction loss (which becomes a larger fraction of the input power as load increases) and with current-loop saturation effects observed at higher RMS currents. By contrast, the Interleaved topology improves monotonically with load, indicating that the interleaving benefit (lower input-current ripple, lower RMS device stress) becomes more pronounced as the converter moves further from light-load discontinuous-conduction operation.
- The reactive-power picture (Fig 6) is the most striking. While the three topologies behave similarly at light load, they diverge sharply above ≈ 2 N·m: at peak load the Classic topology demands 905 VAR, the Bridgeless 790 VAR (12.7 % reduction), and the Interleaved only 664 VAR (26.6 % reduction relative to Classic). For a multi-drive installation, this directly translates into reduced reactive-power burden on the upstream supply.

VI. COMPONENT COUNT AND PRACTICAL TOPOLOGY SELECTION

Although the Interleaved topology delivers the best power-quality performance, the choice of topology in practice is also driven by component count, control complexity, and bill-of-materials cost. Table 5 summarizes the qualitative differences observed during implementation. The relative-cost figures are indicative ratios based on component count and on the additional sensing and gate-drive requirements; they should be interpreted as design guidance rather than as precise vendor-quoted prices.

Table 5 Component Count and Qualitative Complexity Comparison

Component	Classic	Bridgeless	Two-Phase Interleaved
Diode bridge	1 (4 diodes)	—	1 (4 diodes)
Boost inductor(s)	1	1 (or 2)	2
Active switch (MOSFET)	1	2	2
Boost diode(s)	1	2	2
Bulk DC capacitor	1	1	1
Current sensor(s)	1	1	2
Zero-cross detector	—	Required	—
Approx. relative cost	1.0×	1.3–1.5×	1.6–1.8×

Based on the measured results and the component-count comparison, the practical guidance for topology selection in the small-to-medium-power BLDC motor-drive segment can be summarized as follows:

➢ Classic Boost PFC remains the most cost-effective choice for cost-constrained designs at low to medium power (< 500 W) where moderate PF (≈ 0.92) is acceptable and where the additional input-bridge conduction loss does not push the design beyond its thermal limits.
➢ Bridgeless Boost PFC is the recommended mid-range option at medium-to-high power, where the bridge conduction loss becomes a meaningful efficiency penalty. Its main implementation cost is the zero-crossing detection circuitry and the more complex firmware path; designers must also take care of the higher common-mode EMI introduced by removing the bridge.
➢ Two-Phase Interleaved Boost PFC is recommended where power-quality and ripple performance are the primary requirements, particularly above 1 kW or when the upstream supply is sensitive to reactive-power loading. The 26.6 % reduction in peak reactive power observed in this study justifies the additional component cost in installations where multiple drives operate concurrently.

VII. CONCLUSION AND FUTURE WORK

This paper has presented a fair head-to-head experimental comparison of three boost-based active PFC topologies for a brushless DC motor drive: classic, bridgeless, and two-phase interleaved boost PFC. All three converters were digitally controlled with the same dual-loop structure and tested on the same hardware platform under matched load conditions, providing a directly comparable dataset of 24 measurements. Across the measured load range, the Interleaved boost PFC achieved the highest mean power factor (0.9501), followed by the Bridgeless (0.9385) and the Classic (0.9255). The qualitative ordering Classic < Bridgeless < Interleaved was preserved at every load point, and the worst-case reactive-power demand was reduced by 26.6 % from Classic to Interleaved. A qualitative component-count and complexity comparison was also presented to support practical topology selection.

➢ *Several Extensions to this Study are Planned and are Explicitly Scoped Here as Future Work:*

- Total harmonic distortion (THD) and individual-harmonic compliance with IEC 61000-3-2 will be characterized for each topology under the same load profile. THD is the most direct power-quality metric and was not within the measurement scope of the present study.

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/26jul1399

- PFC-stage-only efficiency will be measured by instrumenting the DC-bus power directly, allowing the PFC losses to be separated from the inverter and motor losses.
- The load sweep will be repeated at multiple motor speeds (e.g., 1,500, 2,500, and 3,950 RPM) to characterize topology behavior across the full operating envelope of the drive.
- Conducted EMI and transient response (DC-bus dip and recovery time under load steps) will be measured to round out the power-quality assessment.
- Once the dataset has been expanded across multiple speeds and loads, data-driven prediction models (such as Random Forest or Gaussian Process regression) will be evaluated as a tool for predicting PF, THD, and efficiency at unmeasured operating points, supporting topology selection during the early design phase.

ACKNOWLEDGMENT

The authors gratefully acknowledge Aartronix Innovation Private Limited, Rajkot, Gujarat, India, for providing the hardware platform, instrumentation, and technical support required for the experimental work. The authors also acknowledge financial support from the Shodh Research Fellowship (Government of Gujarat).

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