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Design of 3-Bit and 4-Bit Flash ADC with Low Power and High Efficiency Using Vivado

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Abstract: This paper presents the design and implementation of a Low power and efficient Flash ADC. Several comparators and encoders were developed (AND/OR/XNOR/NOT, XOR, NAND/NOR, and inverter-based), integrated into full Flash ADCs, and their dynamic power, static power, and propagation delay measured A Flash ADC uses a parallel comparator network and a priority encoder for conversion of analog to signals into a digital output. This is achieved in a single clock cycle. In this work, both 3-bit and 4-bit Flash ADCs has been implemented in Vivado using different logic gate combinations to evaluate performance metrics such as dynamic power, static power, and propagation delay. The Flash ADC using NAND-NOR gates encoder and an inverter has used the least power in both 3-bit and 4-bit

Keywords: *Flash ADC, Comparator, Encoder, Verilog, Power Analysis, Dynamic Power, Static Power, Delay.*

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I. INTRODUCTION

Analog-to-Digital Converters (ADCs) are very important for many electronic systems and devices. Majority of signals in modern electronics are analog in nature. They require conversion into digital format for better performance and compatibility. Out of the many types of ADCs, Flash or parallel ADCs, are the fastest. These ADCs are best suited for applications where large bandwidth is critical, as they offer single step digital output by comparing input analog value to different reference voltages. Furthermore, Flash ADC is based on an architecture that performs iterative or successive processes to arrive at digital output in a single pass

II. LITERATURE SURVEY

In one of the related works, the authors make use of a quantization process to achieve digital output. In quantization, a reference voltage circuit splits the input voltage into multiple reference voltages at equal intervals. The input signal is compared to these quantized reference voltages simultaneously using comparators. Leading to the generation of a a sequence of signals, with '1's and '0's representing high and low states respectively.[1].

Various encoder designs have been proposed to reduce power and delay. The disadvantage of XOR gates based encoder is the large transistors count. As the resolution increases, the transistor count also increases significantly[2]. On the other hand, the encoder that consists of a combination of both NAND -NOR gates reduced power by a large margin. [3]. In another work, a low power 3-bit flash ADC was realized in 0.6 micron CMOS technology. The voltage resolution achieved was 34.13 mV while power consumed was 23.88 mW at 2.17 MHz.[4].

A number of different EDA tools are used to design and simulate the flash ADC such as Cadence. However, in this paper, Vivado is used to implement the flash ADC design.

III. IMPLEMENTATION

The Flash ADC will use a number of resistors and comparators which limits their resolution. The comparator must run at high speed which leads to higher power consumption. Hence, Flash ADCs faces challenges such as limited resolution, high power consumption. In addition, the reference ladder has to be low for supplying adequate bias current to the comparators.

- *Comparator*

The number of comparators required is proportional to the resolution required, higher resolution requires more comparators. Various comparators have been designed in 3 bit and 4 bit using Verilog to analyze their functionality, performance, and suitability for use in the Flash ADC. The comparator has been designed by using XNOR, AND, OR gates, another using XOR, AND, OR, NOT gates and last one using AND, OR gates. The 3-bit and 4-bit comparator designed using XNOR, AND, OR gates showed the best

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performance in both cases. The designs for the comparators are shown in fig.1 and 2 respectively for the 3-bit and 4-bit cases. The 3-bit comparator designed using AND-OR gates showed a dynamic power of 1.073 W and 4 bit is 0.958 W while the dynamic power of comparator with XOR-AND-OR-NOT gates is 0.996 W and in the case of 4-bit comparator, the value is 0.904 W and the dynamic power of comparator with XNOR-AND-OR gates is 0.598 W for 3-bit. In the case of 4-bit comparator, the value is 0.532 W.

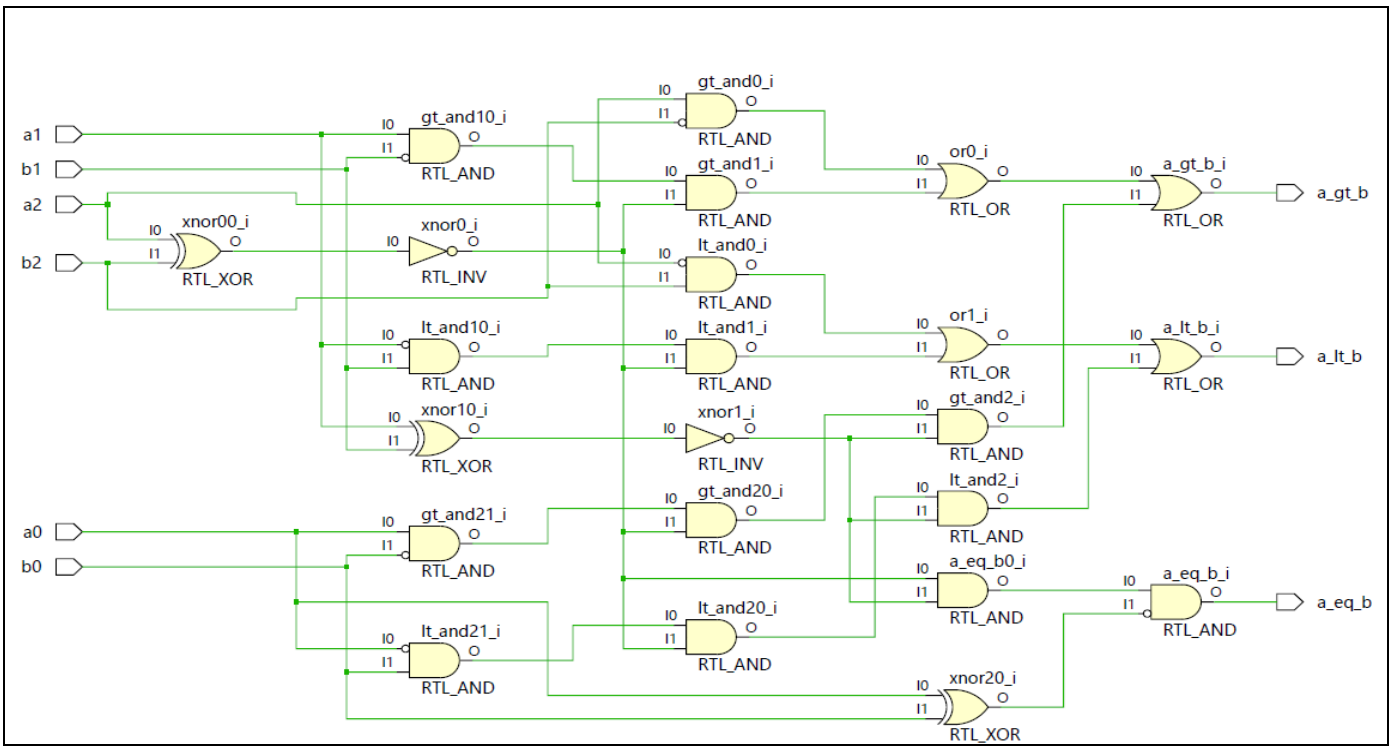

Fig 1 3-Bit Comparator Using XNOR-AND-OR Gates

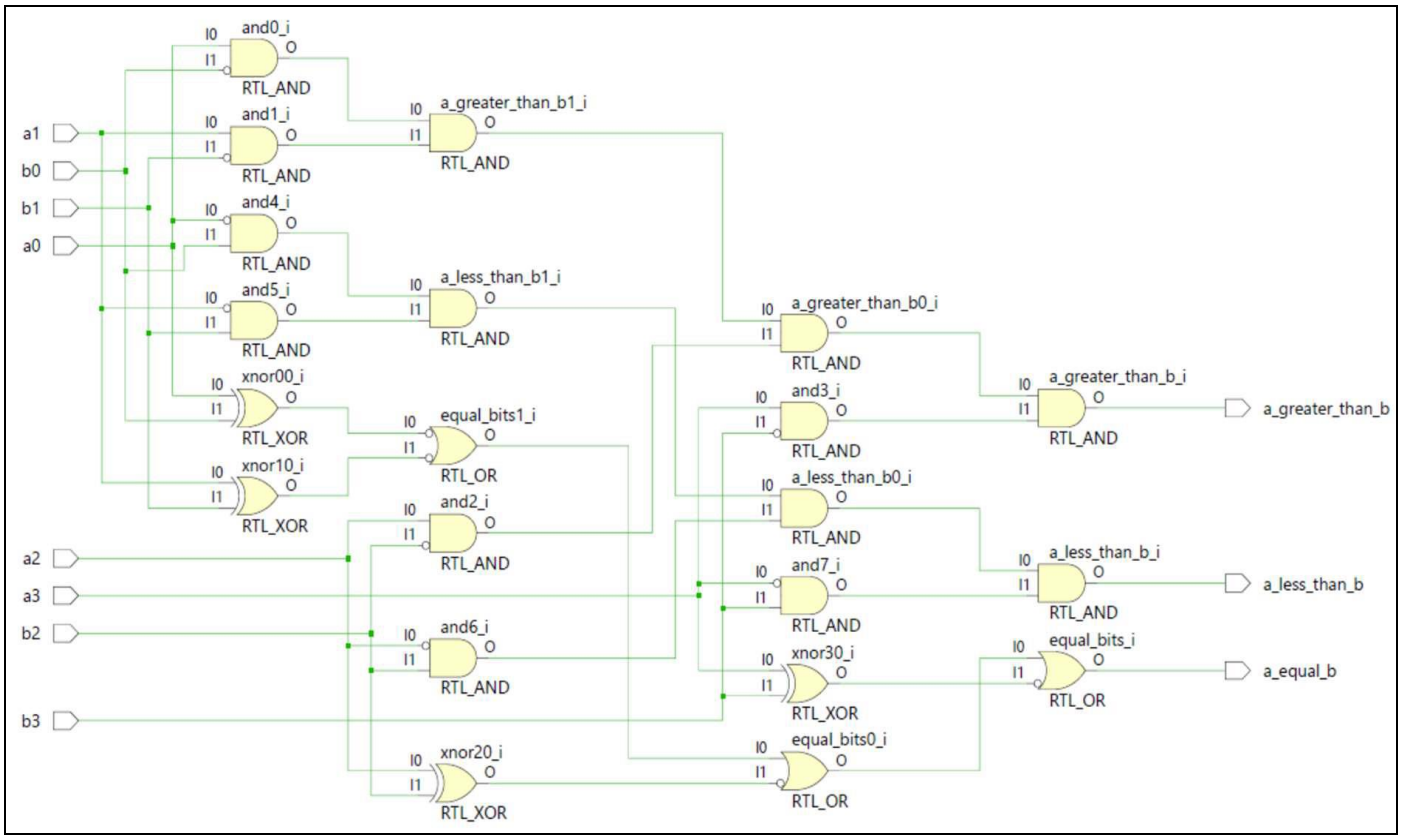

Fig 2 4-Bit Comparator Using XNOR-AND-OR Gates

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➢ *Encoder*

3 and 4-bit encoders have been designed using combinations of XOR, AND, OR, NAND and NOR gates to analyze their functionality, performance, and suitability for use in the Flash ADC. The 3-bit and 4-bit encoder designed using NAND-NOR gates shown in fig. 3 and 4 displayed the best performance.

The dynamic power of 3-bit encoder designed using AND-OR gates was 1.15 W and 4 bit is 1.07 W while the dynamic power of XOR encoder is 1.03 W. The dynamic power of 4-bit encoder with XOR gate is 0.912 W. The lowest dynamic power was achieved for the encoder with NAND-NOR gates with a value of 0.497 W for 3 bit and 0.395 W in the case of 4-bit encoder.

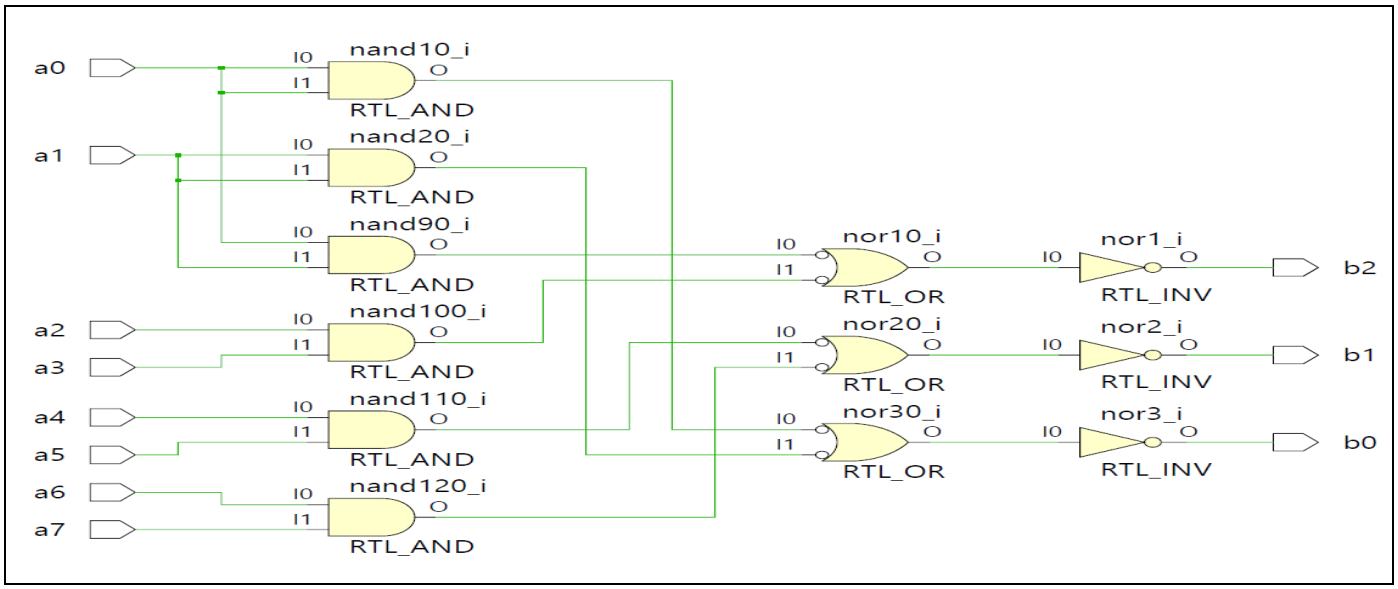

Fig 3 3-Bit Encoder Using NAND-NOR Gates

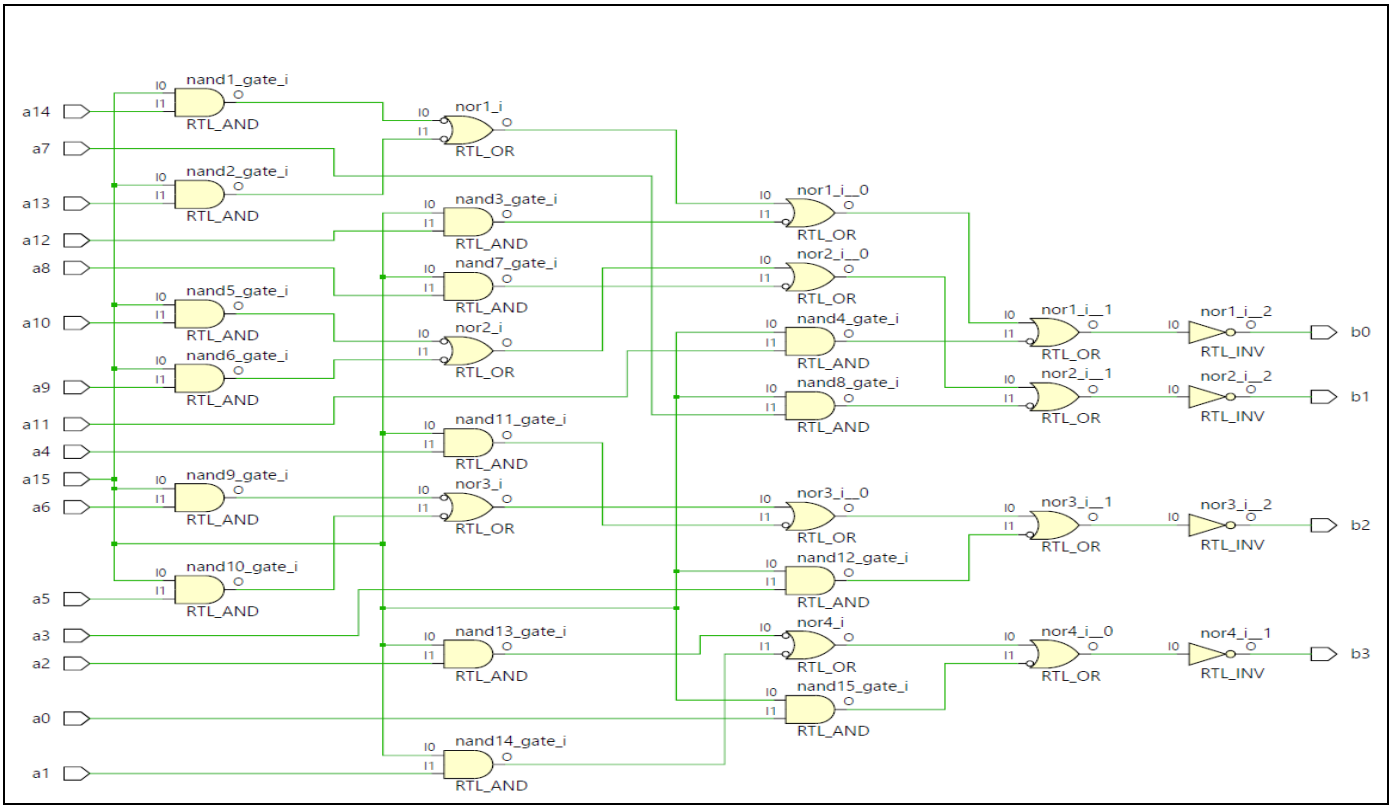

Fig 4 4-Bit Encoder Using NAND-NOR Gates

➢ *Flash ADC*

The Flash ADC has been designed in 3 bit and 4 bit using Verilog to analyze their functionality, performance, and the Flash ADC which operates in low power. The Flash ADC with the combination of inverters and NAND NOR gates have shown the lowest power in both 3-bit and 4-bit shown below.

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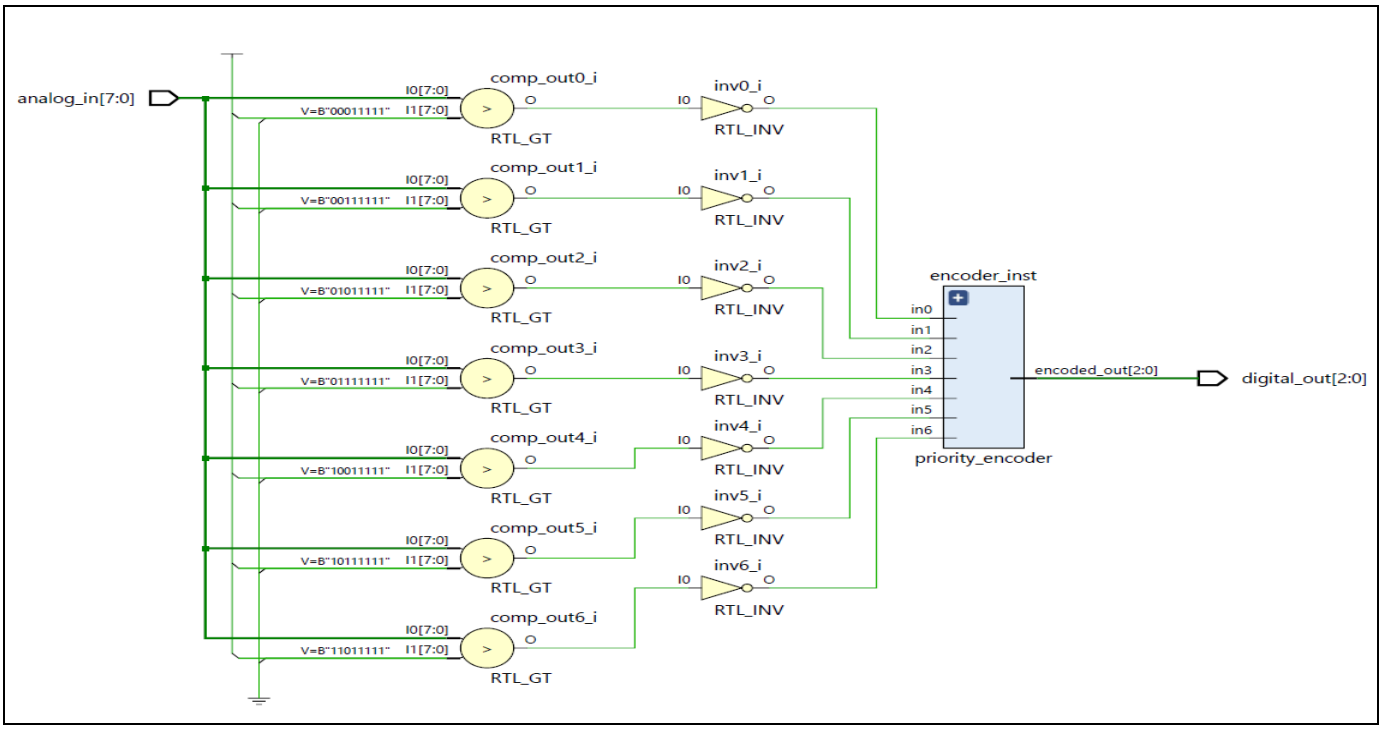

Fig 5 3-Bit Flash ADC Using NAND-NOR Gates Encoder

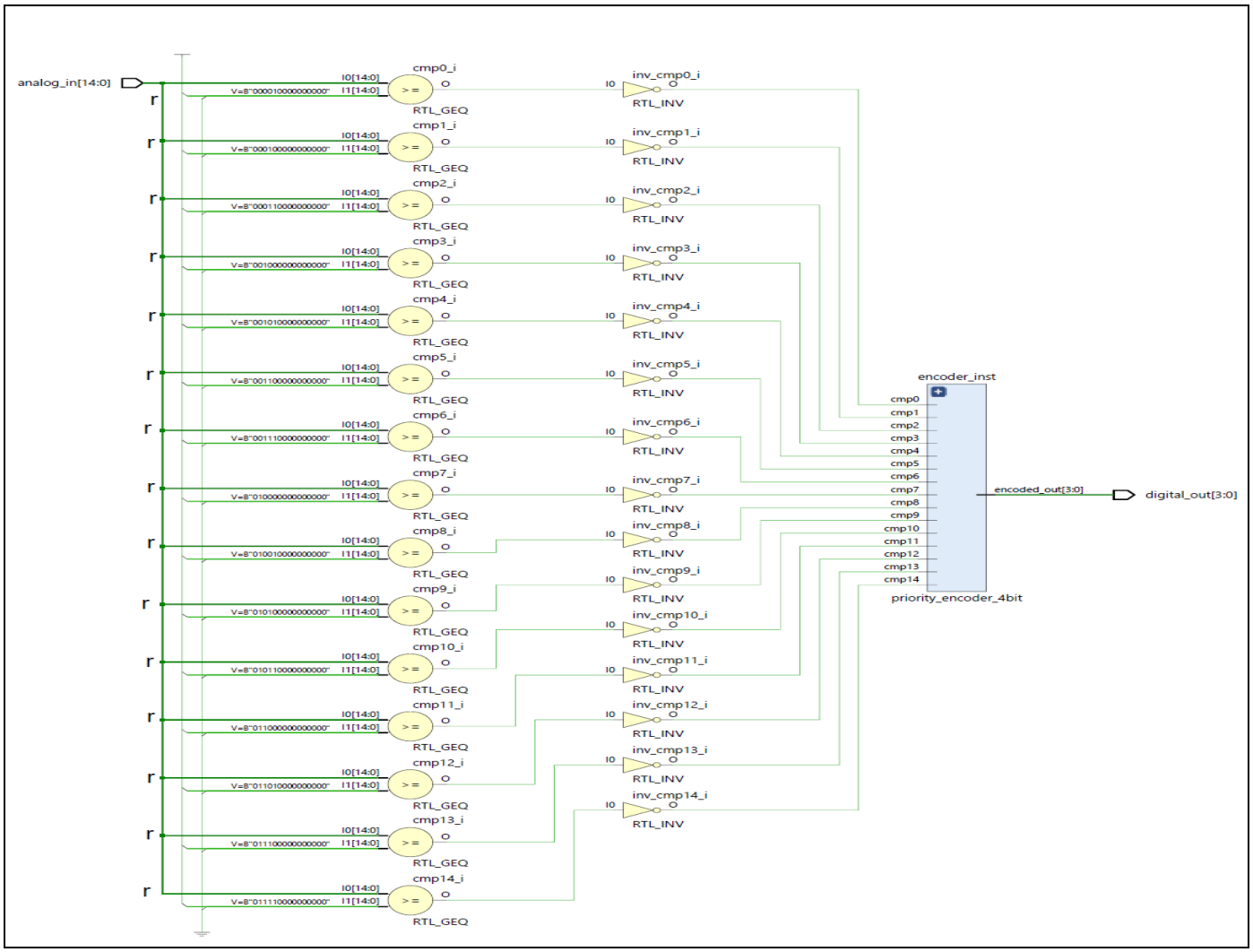

Fig 6 4-Bit Flash ADC Using NAND-NOR Gates Encoder

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IV. RESULTS

In this work the efficiency of Flash ADC design is determined experimentally based on performance metrics such as Dynamic power, static power, delay.

Table 1 3-Bit Flash ADC Performance Parameters

3-bit	Performance parameters	
	Total Power (W)	***Delay (ns)***
Flash ADC using AND OR	1.113	5.12
Flash ADC using XOR encoder	0.816	4.35
Flash ADC using NAND NOR encoder	0.221	1.89

Table 2 4-Bit Flash ADC Performance Parameters

4-bit	Performance parameters	
	Total Power (W)	***Delay (ns)***
Flash ADC using AND OR	1.491	5.86
Flash ADC using XOR encoder	0.982	4.72
Flash ADC using NAND NOR encoder	0.329	2.75

Table 3 3-Bit Flash ADC Power Consumption Percentage

3-bit	Performance parameters	
	Dynamic Power (W)	***Static power (W)***
Flash ADC using AND OR	93%	7%
Flash ADC using XOR encoder	90%	10%
Flash ADC using NAND NOR encoder	69%	31%

Table 4 4-Bit Flash ADC Power Consumption Percentage

4-bit	Performance parameters	
	Dynamic Power (W)	***Static power (W)***
Flash ADC using AND OR	94%	6%
Flash ADC using XOR encoder	89%	11%
Flash ADC using NAND NOR encoder	75%	25%

The Flash ADC using NAND/NOR is more efficient in in both 3-bit and 4-bit due to less switching activity and energy consumption.

The inverter NAND/NOR Flash ADC is significantly more power-efficient in both 3-bit and 4-bit.

The Flash ADC using an inverter/NAND/NOR gate encoder demonstrably outperforms the XOR encoder design across both power and delay metrics. This is primarily because inverter, NAND, and NOR gates are fundamental, more efficient logic primitives than other gates

The Flash ADC with the inverter and NAND/NOR gate encoder is also much faster, exhibiting a lesser delay of compared to others design in both 3-bit and 4-bit.

The other 2 Flash ADCs are inferior in terms of power and speed when compared to the Flash ADC that has inverter and NAND/NOR gate due to a more complex logic structure, higher transistor count, or greater switching activity within the circuit.

The 3-Bit and 4-bit Flash ADC using NAND-NOR Encoder is more power-efficient and faster compared to the regular 3-Bit and 4-bit types.

Both the NAND-NOR encoder and comparator using AND-OR-XNOR-NOT provide more efficient logic operations, resulting in reduced power consumption in both dynamic and signal power categories.

The signal paths in the NAND-NOR encoder are less complex, leading to lower signal power consumption.

The comparator uses the inverter for signal processing which delivers sharper logic levels and reducing glitches.

It is used to simplify the encoder logic, as inverted inputs may allow direct feeding into logic gates without additional conversion stages.

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Fig 7 3-Bit Flash ADC Waveform

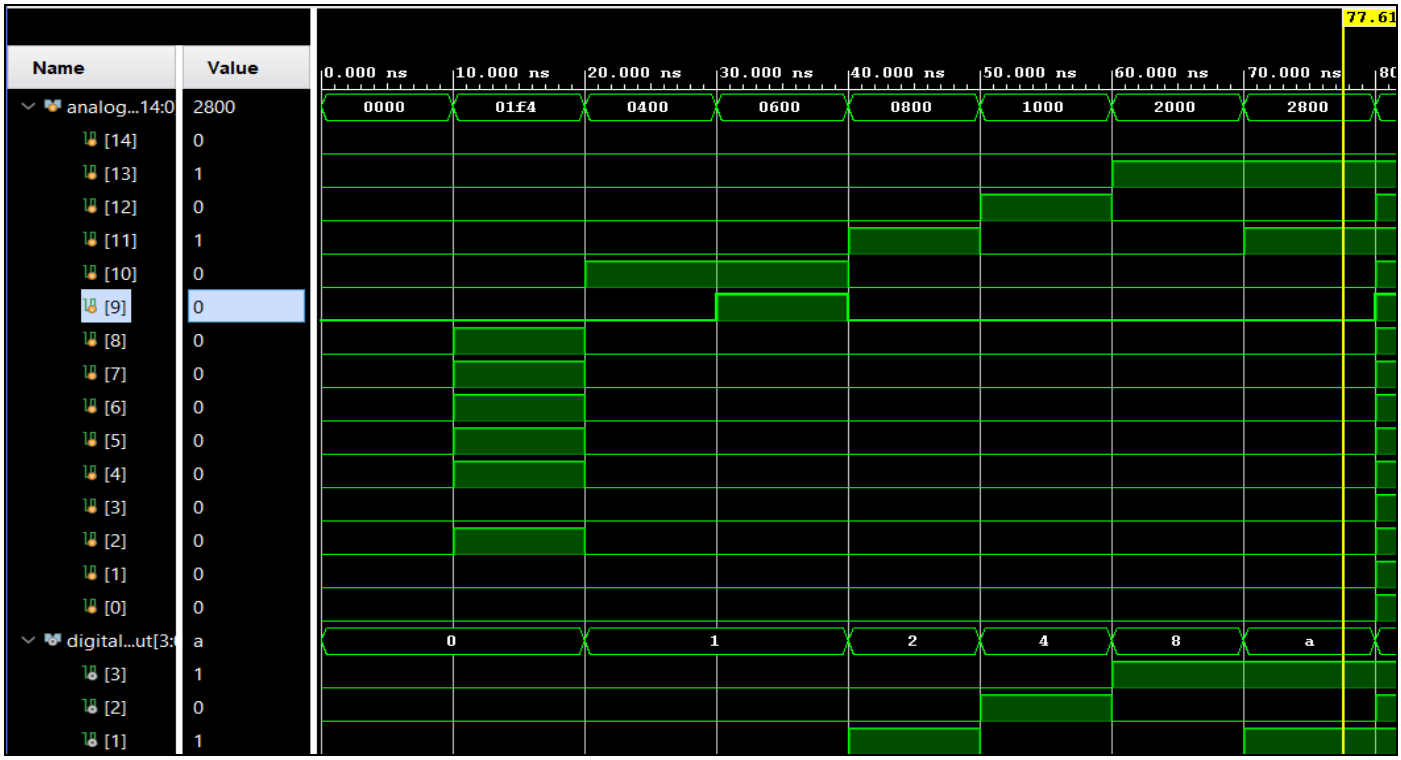

Fig 8 4-Bit Flash ADC Waveform

V. CONCLUSION

In the present work 3 and 4-bit flash ADCs that show low power and high efficiency were designed using different encoders and comparator architectures. Different logic designs were analyzed and it was observed that Flash ADC with inverter and NAND-NOR gates encoder improves performance when compared to others in both 3-bit and 4-bit cases.

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