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Comparative Study of R–2R and Current Steering DACs for 3–5 Bit Resolutions

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Abstract: Digital-to-Analog Converters (DACs) play a vital role in modern mixed-signal systems by transforming digital data into precise analog outputs. This research presents a comparative analysis of two prominent DAC architectures—R– 2R Ladder and Current Steering DAC—implemented in Cadence Virtuoso using 180nm CMOS technology for 3-bit and 5-bit resolutions. The study focuses on evaluating linearity parameters such as Differential Non-Linearity (DNL) and Integral Non-Linearity (INL), along with performance metrics including speed, design complexity, and application suitability. Simulation results obtained using the Spectre simulator confirm accurate and monotonic digital-to-analog conversion for both architectures. The R–2R Ladder DAC demonstrates excellent simplicity and power efficiency, making it ideal for low- to medium-speed applications. Conversely, the Current Steering DAC exhibits superior linearity, faster response, and minimal glitch energy, proving advantageous for high-speed and high- frequency systems. The comparative findings highlight the trade-offs between ease of implementation and performance precision, offering insights into selecting appropriate DAC architectures for specific mixed-signal design requirements. This study validates the effectiveness of both designs and establishes a framework for optimizing DAC performance in future CMOS-based integrated circuit applications.

Keywords: *R–2R Ladder DAC, Current Steering DAC, Cadence Virtuoso, INL, DNL, 3-bit, 5-bit.*

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I. INTRODUCTION

Digital-to-Analog Converters (DACs) are fundamental com ponents in signal processing systems, enabling conversion of digital data into corresponding analog voltages or currents. DACs are extensively used in communication systems, in strumentation, audio devices, and embedded systems where precise analog outputs are required [1], [3]. Among several DAC architectures, the R–2R Ladder DAC and Current Steering DAC stand out for their simplicity, speed, and scalability [4], [5]. The R–2R Ladder DAC uses resistors in a binary-weighted configuration to generate an analog output proportional to the digital input. It offers good accuracy and ease of implementation for low to medium resolutions. In contrast, the Current Steering DAC employs controlled current sources for each bit, providing high-speed operation suitable for high-frequency and high-resolution applications. This paper presents a comparative analysis of both DAC architectures implemented in Cadence Virtuoso at 180nm CMOS technology [5], [8], [11]. Circuits with 3-bit and 5-bit resolutions are designed, simulated, and analyzed based on linearity parameters (INL and DNL). The goal is to highlight the differences in design complexity, accuracy, and suitability for different applications [7], [10].

II. CIRCUIT IMPLEMENTATION IN CADENCE

The circuit design and simulation were performed in Cadence Virtuoso using the Spectre simulator. Both R–2R and Current Steering DACs were designed for 3-bit and 5-bit resolutions. Resistor and current source values were selected carefully to ensure uniform voltage/current scaling and refer ence matching for each bit [2], [4], [9].

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➢ *R–2R 3-bit Resolution Circuit*

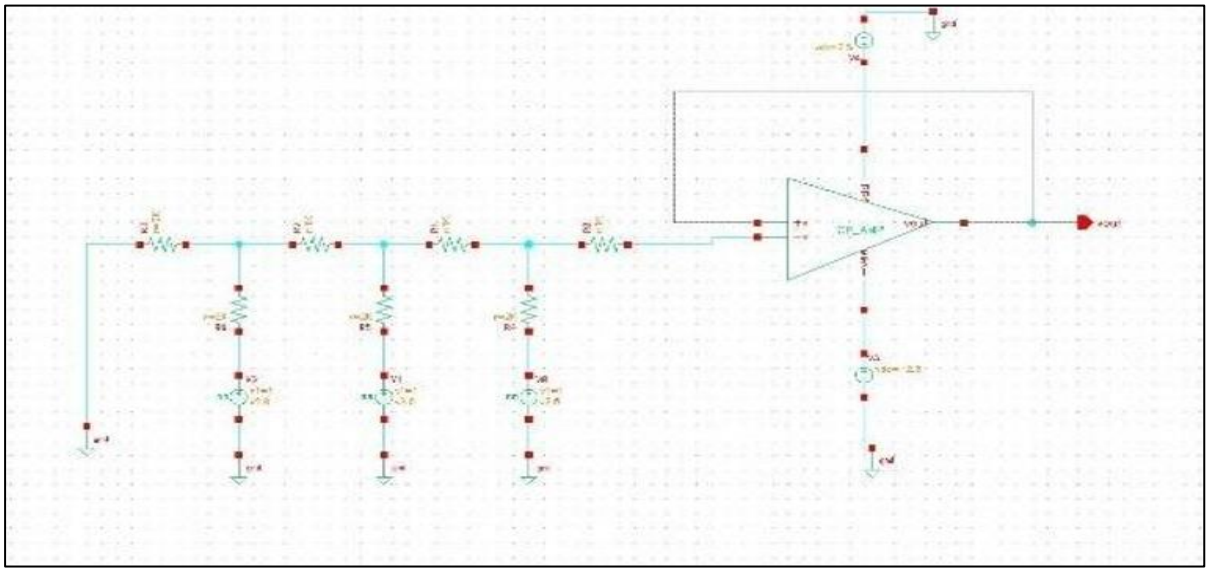

Fig 1 R–2R Ladder DAC with 3-bit Resolution Implemented in Cadence Virtuoso.

The R–2R Ladder Digital-to-Analog Converter (DAC) is a simple and widely used resistive network that converts digital binary inputs into corresponding analog output voltages. In a 3-bit R–2R ladder DAC implemented in Cadence Virtuoso, the circuit consists of resistors arranged in a repetitive structure of only two resistance values—R and 2R—connected in a ladder-like configuration. Each bit of the digital input controls a switch that connects either to the reference voltage (Vref) or ground, thereby determining the contribution of that bit to the output voltage. The most significant bit (MSB) contributes the largest portion of the analog output, while the least significant bit (LSB) contributes the smallest. The output voltage is obtained by summing the weighted currents through the resistive network, resulting in a staircase-like analog output proportional to the binary input This design offers high linearity, simple implementation, and ease of scaling for higher resolutions, making it ideal for integration and simulation in analog mixed-signal environments like Cadence Virtuoso [5], [8], [11].

➢ *R–2R 5-bit Resolution Circuit*

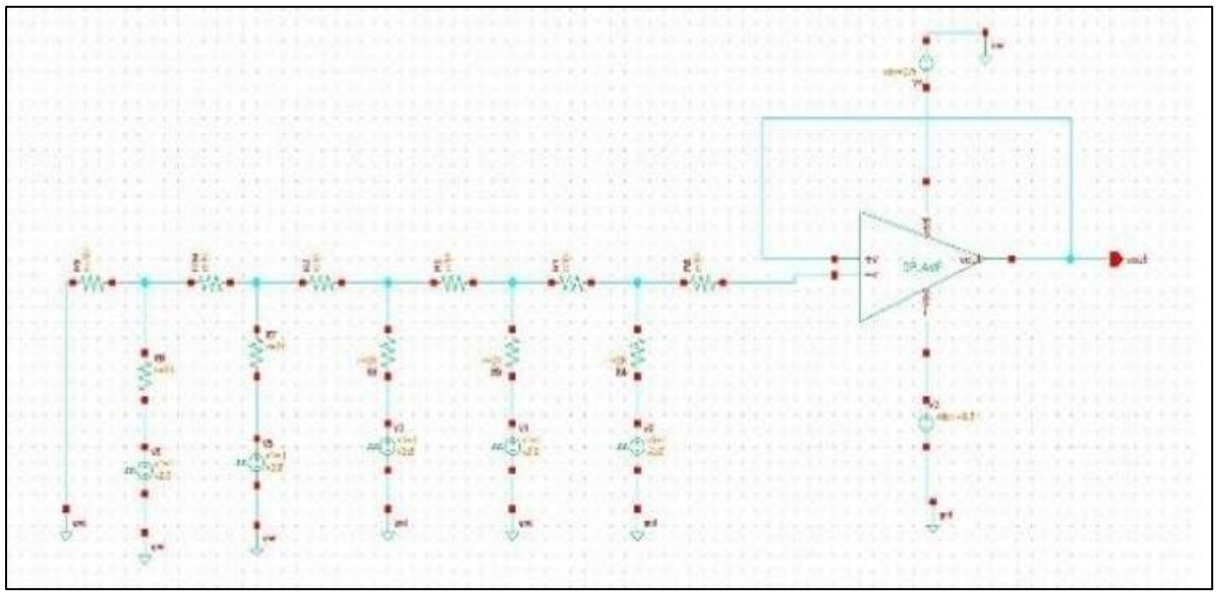

Fig 2 R–2R Ladder DAC with 5-bit Resolution Implemented in Cadence Virtuoso.

The R–2R Ladder Digital-to-Analog Converter (DAC) with 5-bit resolution implemented in Cadence Virtuoso operates on the same fundamental principle as the 3-bit version but provides finer output resolution with 32 discrete analog levels. It consists of a repeating network of resistors having only two values, R and 2R, forming a ladder-like structure that efficiently converts 5-bit binary digital input signals into corresponding analog output voltages[2], [4], [9].

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Each digital input bit controls an electronic switch that connects either to the reference voltage (Vref) or ground, contributing a weighted portion of the total output based on its bit significance. The most significant bit (MSB) determines the largest voltage step, while the least significant bit (LSB) produces the smallest. The output voltage is a precise weighted sum of all bit contributions, creating a smooth staircase analog waveform. The 5-bit R–2R DAC offers improved resolution and accuracy compared to lower-bit DACs while maintaining design simplicity, excellent linearity, and ease of implementation in Cadence Virtuoso for circuit analysis, layout, and performance verification[5], [8], [11].

- *Current Steering 3-bit Resolution Circuit*

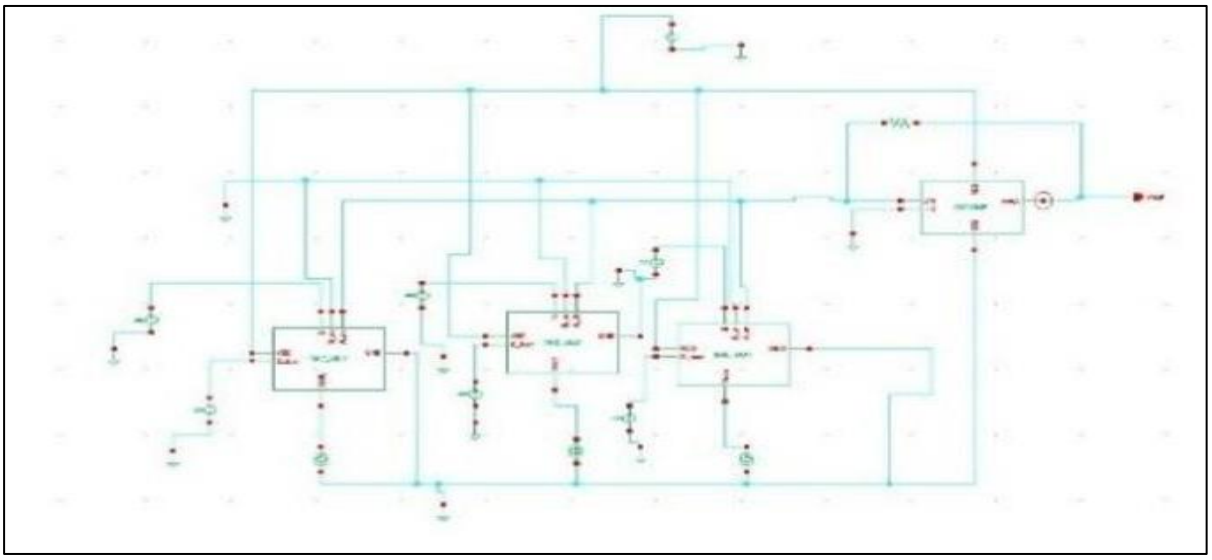

Fig 3 Current Steering DAC with 3-bit Resolution Implemented in Cadence Virtuoso.

The Current Steering Digital-to-Analog Converter (DAC) with 3-bit resolution implemented in Cadence Virtuoso converts digital input codes into corresponding analog output currents by using a set of precisely matched current sources and switching transistors. In this architecture, each bit of the digital input controls a current source that delivers a specific fraction of the total output current, with the most significant bit (MSB) contributing the largest current and the least significant bit (LSB) the smallest. [2], [4], [9] The current sources are typically implemented using matched MOS transistors to ensure accuracy and linearity. When a digital input is applied, current steering switches direct the output currents either toward the output node or to ground, depending on the bit value (1 or 0). The total output current, which is the sum of the active current sources, produces an analog voltage when passed through a load resistor. This DAC architecture offers high-speed operation, good linearity, and compact design, making it suitable for high-frequency applications and efficient implementation, simulation, and performance verification in Cadence Virtuoso [5], [8], [11].

- *Current Steering 5-bit Resolution Circuit*

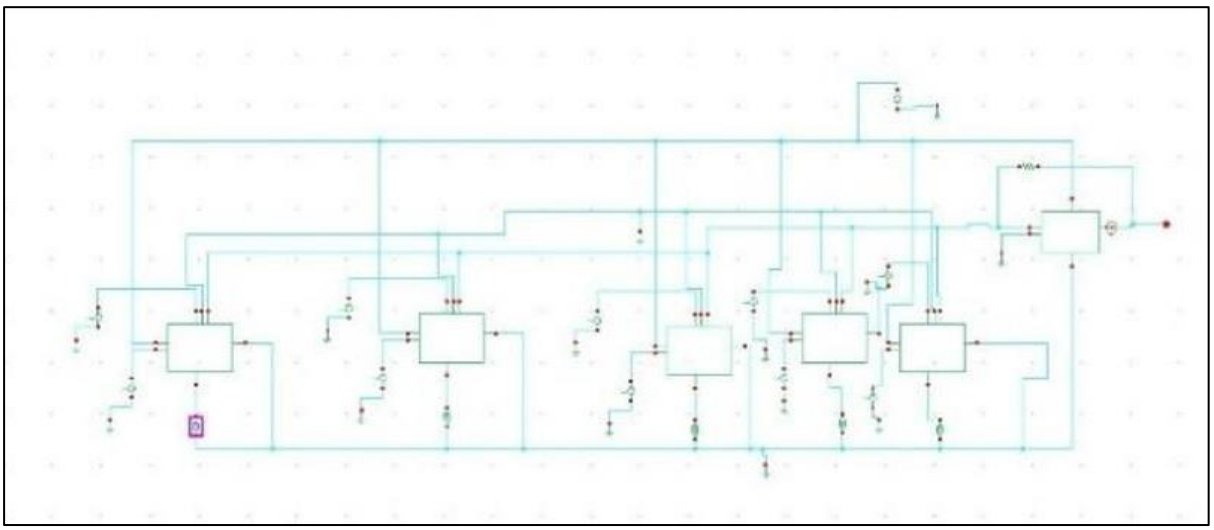

Fig 4 Current Steering DAC with 5-bit Resolution Implemented in Cadence Virtuoso

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The Current Steering Digital-to-Analog Converter (DAC) with 5-bit resolution implemented in Cadence Virtuoso is a high-speed DAC architecture that converts a 5-bit digital input into a corresponding analog output current using an array of precisely matched current sources. Each of the five input bits controls a binary-weighted current source, where the most significant bit (MSB) contributes the highest current and the least significant bit (LSB) contributes the smallest. Depending on the digital input code, current steering switches—typically implemented with MOS transistors— direct each current either to the output node or to ground. The sum of the steered currents forms the total output current, which can be converted into an analog voltage across a load resistor [2], [4], [9]. This architecture ensures fast conversion speeds, excellent linearity, and low glitch energy compared to resistive DACs. The 5-bit current steering DAC provides 32 discrete output levels, offering higher resolution and improved accuracy. Its implementation in Cadence Virtuoso allows detailed simulation, layout verification, and performance analysis, making it suitable for high-speed and mixed-signal integrated circuit applications [5], [8], [11].

III. SIMULATION RESULTS

The designed circuits were simulated in Cadence using Specter. The output voltage for all digital input codes was measured and plotted. The following figures show the output waveforms and the transient analysis for both DAC types and resolutions. We received a uniform and theoretically ideal staircase waveform output with 8 and 32 steps for 3- and 5-bit resolution, respectively.

- *R–2R 3-bit Resolution*

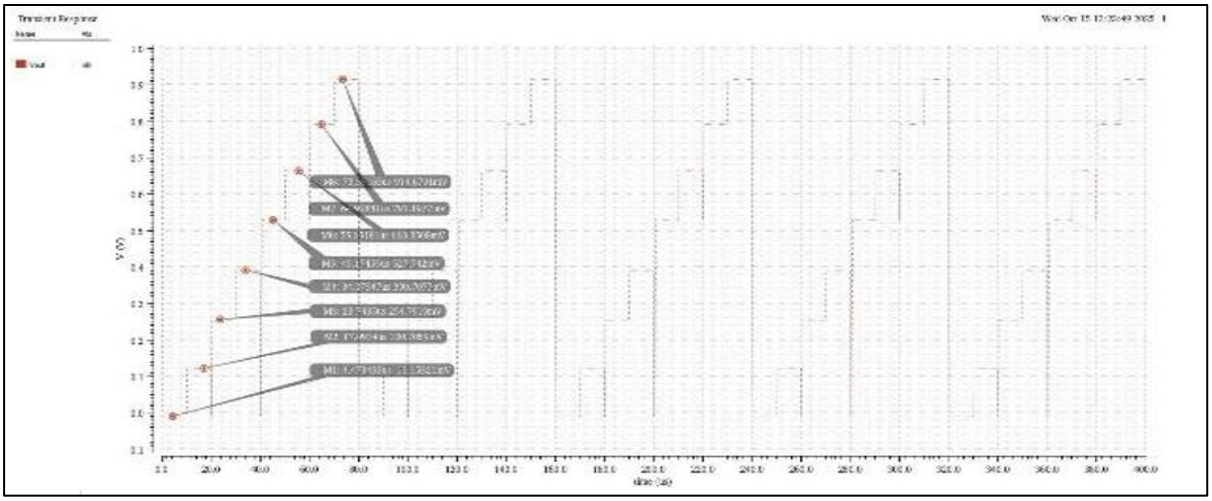

Fig 5 Simulation Result of 3-bit R–2R DAC.

Figure 5 shows the simulated output waveform of the 3-bit R–2R ladder DAC. The transient analysis illustrates a well-defined staircase response, where each step corresponds to a unique digital input code, indicating good linearity and predictable voltage increments between successive level.

- *R–2R 5-bit Resolution*

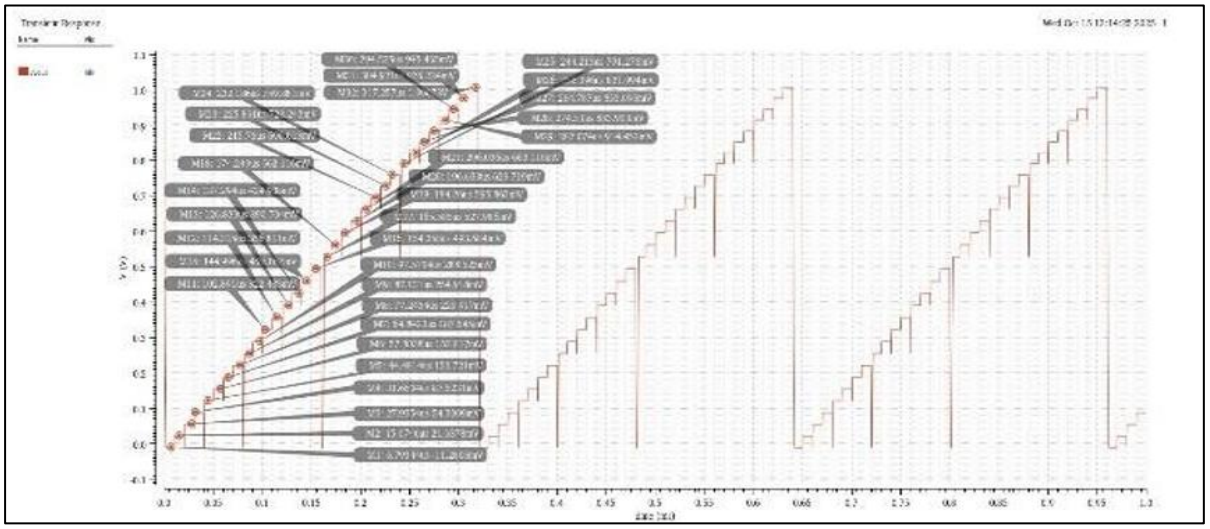

Fig 6 Simulation Result of 5-bit R–2R DAC

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Figure 6 illustrates the simulation result of the 5-bit R–2R Ladder DAC implemented in Cadence Virtuoso. The transient analysis shows a smooth and uniform staircase waveform with 32 distinct output voltage levels, corresponding to the 5-bit digital input combinations ranging from 00000 to 11111. Each step represents an equal voltage increment, confirming accurate binary-weighted voltage generation and proper functioning of the R–2R resistor network. The waveform demonstrates good linearity, monotonic behavior, and a consistent step size, indicating that the DAC effectively converts digital input codes into proportional analog output voltages.

➢ *Current Steering 3-bit Resolution*

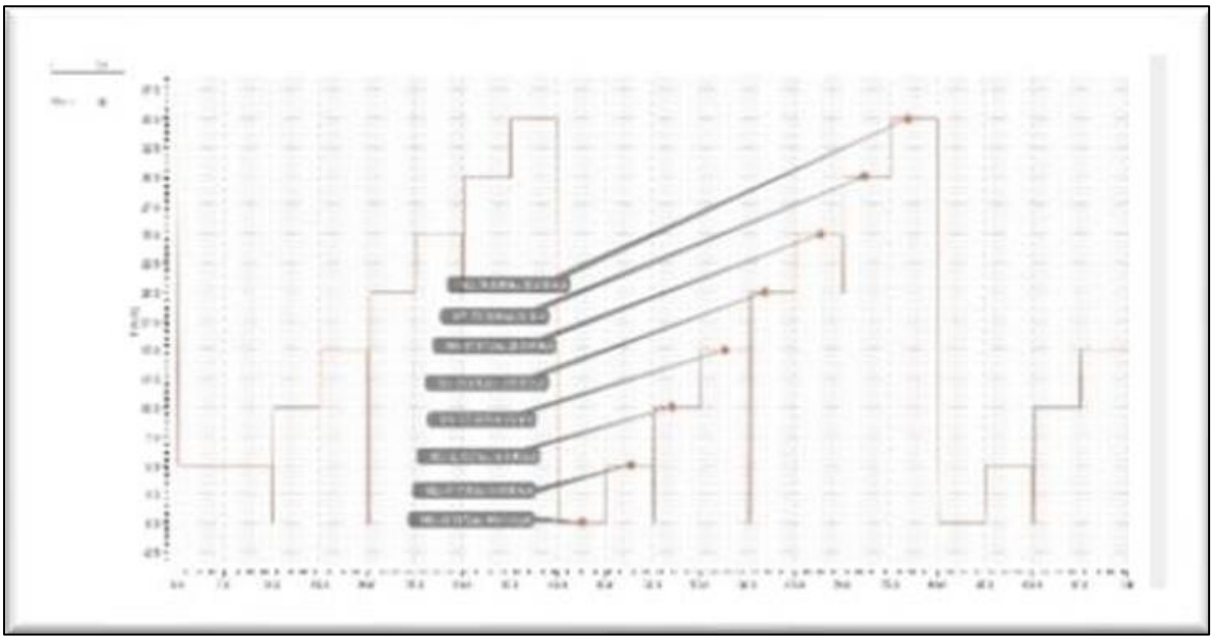

Fig 7 Simulation Result of 3-bit Current Steering DAC

Figure 7 shows the simulation result of the 3-bit Current Steering DAC implemented in Cadence Virtuoso. The circuit was designed using binary-weighted current sources controlled by digital input bits, and simulated using the Spectre tool to observe the transient response. The output waveform exhibits a well-defined staircase current-to-voltage conversion with 8 distinct levels, corresponding to digital input codes from 000 to 111. Each step represents the summed contribution of the active current sources, demonstrating precise current steering and accurate digital-to-analog conversion. The DAC exhibits good linearity, low glitch energy, and a uniform step size, confirming its effective operation and suitability for high-speed mixed-signal applications.

➢ *Current Steering 5-bit Resolution*

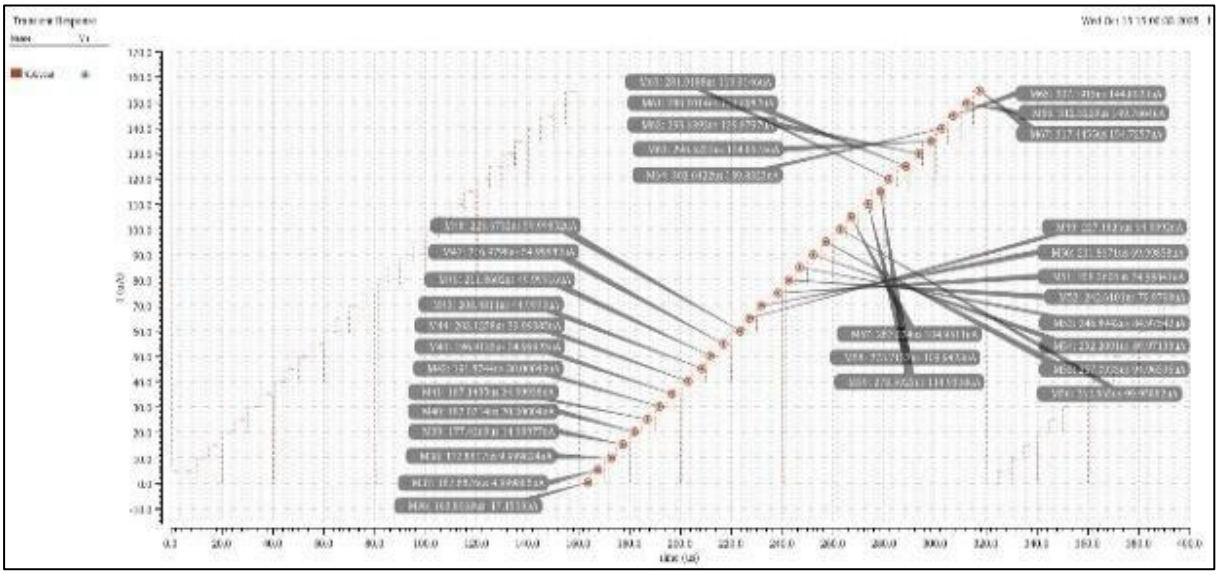

Fig 8 Simulation Result of 5-bit Current Steering DAC

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/26may175

Figure 8 presents the simulation result of the 5-bit Current Steering DAC implemented and analyzed in Cadence Virtuoso using the Spectre simulator. The output waveform clearly demonstrates a uniform staircase response with 32 discrete output levels, corresponding to the 5-bit digital input codes ranging from 00000 to 11111. Each step reflects the contribution of the binary-weighted current sources, where the most significant bit (MSB) provides the largest current and the least significant bit (LSB) provides the smallest. The transient analysis confirms accurate and monotonic digital-to-analog conversion with minimal nonlinearity and glitch distortion. The results validate that the current steering architecture provides high-speed performance, excellent linearity, and stable output transitions, making it highly suitable for precision analog and mixed-signal circuit applications.

IV. ANALYSIS USING DNL AND INL

The Differential Non-Linearity (DNL) and Integral Non- Linearity (INL) analyses were carried out for each DAC configuration to evaluate their accuracy, linearity, and overall performance. The measurements were obtained from transient simulation results in Cadence Virtuoso using the Spectre simulator. The ideal Least Significant Bit (LSB) step size was computed based on the reference voltage range and the number of bits of resolution [1], [3].

DNL represents the deviation of the actual analog step size between two consecutive digital codes from the ideal LSB value. A DNL of ±1 LSB or less ensures monotonicity, meaning the output always increases with increasing input code [9], [12]. INL, on the other hand, measures the deviation of the actual transfer function from a straight line connecting the ideal end points, thereby indicating cumulative errors in linearity. Ideally, both DNL and INL should be as close to zero as possible for accurate digital-to-analog conversion.

The following tables summarize the calculated DNL and INL values for all DAC architectures and resolutions. The results confirm that both the R–2R Ladder DAC and the Current Steering DAC exhibit acceptable levels of linearity and monotonicity, with slight differences depending on design topology and resolution [6], [7].

$$DNL(i) = \frac{Vout(i+1) - Vout(i)}{Vlsb} - 1$$

$$INL(i) = \frac{Vout(i) - Videal(i)}{Vlsb}$$

- *R–2R 3-bit DAC*

Table 1 INL - DNL Analysis of 3bit R-2R DAC

Code	Code(bin)	DNL (LSB)	INL (LSB)
0	0		0
1	1	0.9976	-0.003
2	10	0.0135	0.0028
3	11	0.0168	0.0184
4	100	0.0357	0.0522
5	101	0.0255	0.0694
6	110	-0.0341	0.0291
7	111	-0.0668	-0.0761

The 3-bit R–2R DAC demonstrates near-ideal performance with minimal DNL and INL deviations. Small variations at higher input codes are attributed to resistor mismatches, layout parasitic, and finite switch resistance in the simulation model. The DNL remains within ±0.1 LSB, ensuring monotonic operation. The INL also remains below 0.1 LSB, confirming that the DAC output follows the ideal linear transfer function closely. The results validate that the R–2R structure provides accurate binary-weighted voltage generation for low-bit resolutions.

- *R–2R 5-bit DAC*

Table 2 INL - DNL Analysis of 5bit R-2R DAC

Code	Code(bin)	DNL (LSB)	INL (LSB)
0	0		0
1	1	0.0029	0.0046
2	10	-0.009	0.0914
3	11	0.012	0.1609
4	100	0.0143	0.2354
5	101	0.0069	0.3003
6	110	0.0275	0.3766
7	111	0.0157	0.4449
8	1000	0.0369	0.5606
9	1001	0.0193	0.6396

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10	1010	0.0339	0.7986
11	1011	0.0448	1.0586
12	1100	0.0315	1.3628
13	1101	0.0415	1.6352
14	1110	-0.2319	0.8866
15	1111	0.3242	3.5959
16	10000	0.0445	3.7612
17	10001	0.0397	3.9262
18	10010	0.0304	4.0793
19	10011	0.0329	4.2001
20	10100	0.0173	4.1412
21	10101	0.0018	3.9727
22	10110	-0.0213	3.6907
23	10111	-0.0388	3.5311
24	11000	-0.0474	3.3571
25	11001	-0.064	2.9299
26	11010	-0.0532	2.7479
27	11011	-0.0631	2.5526
28	11100	-0.0704	2.3543
29	11101	-0.057	2.1367
30	11110	-0.066	1.9141
31	11111	-0.0772	1.7147

For the 5-bit R–2R DAC, the number of output levels increases to 32, resulting in more potential for cumulative nonlinearity. As seen from the table, the INL gradually increases with code progression, reaching up to 1.7 LSB at the full-scale output. This nonlinearity primarily arises from mismatch between R and 2R resistors, limited precision in resistor fabrication, and parasitic capacitances at each node. Despite these effects, the DNL values remain within the acceptable range of ±0.1 LSB, ensuring a monotonic output response. The DAC therefore maintains good performance and accuracy for moderate-resolution applications.

- *Current Steering 3-bit DAC*

Table 3 INL - DNL Analysis of 3bit Current Steering DAC

Code (bin)	Code (dec)	DNL (LSB)	INL (LSB)
000	0		0
001	1	0.006917	0.006917
010	2	0.006917	0.006917
011	3	0.006917	0.006917
100	4	0.0000059	0.000033
101	5	-0.00112	0.00223
110	6	-0.00114	0.001085
111	7	-0.00108	0

The 3-bit Current Steering DAC exhibits excellent linearity and very low DNL/INL values, all within ±0.01 LSB. The near-zero deviations indicate precise current source matching, stable transistor operation, and minimal switching glitches. The INL trend remains nearly flat across all input codes, showing that the output current increases linearly with the digital input. This confirms the high accuracy and robustness of the current steering technique, especially for low-bit, high-speed DAC applications.

- *Current Steering 5-bit DAC.*

Table 4 INL - DNL Analysis of 5bit Current Steering DAC

Code	Code(bin)	DNL (LSB)	INL (LSB)
0	0	0	0
1	1	0.002	0.002
2	10	0	0.002
3	11	–0.000	0.002
4	100	0.001	0.003
5	101	–0.000	0.003
6	110	0.001	0.004

ISSN No:-2456-2165 https://doi.org/10.38124/ijisrt/26may175

7	111	–0.000	0.004
8	1000	0	0.004
9	1001	–0.000	0.004
10	1010	–0.000	0.004
11	1011	–0.000	0.004
12	1100	–0.000	0.004
13	1101	0	0.004
14	1110	0	0.004
15	1111	–0.000	0.004
16	10000	–0.004	0
17	10001	–0.001	–0.001
18	10010	–0.001	–0.002
19	10011	–0.001	–0.003
20	10100	–0.001	–0.004
21	10101	–0.002	–0.006
22	10110	–0.002	–0.008
23	10111	–0.002	–0.010
24	11000	–0.002	–0.012
25	11001	–0.002	–0.014
26	11010	–0.002	–0.016
27	11011	–0.003	–0.019
28	11100	–0.003	–0.022
29	11101	–0.003	–0.025
30	11110	–0.004	–0.028
31	11111	–0.001	–0.029

The 5-bit Current Steering DAC maintains outstanding linearity across its entire 32-step range, with both DNL and INL values remaining extremely small—well below ±0.05 LSB. These results highlight the superior matching accuracy of the current sources, which are less affected by parasitic variations compared to resistor-based architectures. The monotonic output behavior and near-ideal transfer curve make this DAC highly suitable for high-speed and precision applications where low distortion and fast settling time are required. From the comparative DNL and INL results, it is evident that both architectures achieve satisfactory linearity for their respective bit resolutions. However, the Current Steering DAC exhibits superior performance due to its better current source matching, lower sensitivity to process variations, and faster switching response. The R–2R DAC, while simpler and easier to implement, shows slightly higher INL deviations at higher resolutions due to resistor mismatches. Nonetheless, both designs are fully functional and demonstrate accurate digital-to-analog conversion characteristics, validating their implementation and simulation in Cadence Virtuoso.

V. COMPARATIVE ANALYSIS OF IMPLEMENTED ARCHITECTURES

To evaluate the overall performance and efficiency of the designed digital-to-analog converters (DACs), a comparative analysis was conducted between the R–2R Ladder DAC and the Current Steering DAC, each implemented for 3-bit and 5-bit resolutions in *Cadence Virtuoso*. The evaluation considered key parameters such as linearity (DNL and INL), speed, area efficiency, power consumption, and integration suitability in mixed-signal systems [1].

The R–2R Ladder DAC, based on resistive voltage division, offers a compact and predictable design for low-resolution applications. However, as the resolution increases, resistor mismatches, temperature variations, and parasitic effects cause noticeable deviations in INL and reduced conversion speed. Consequently, this structure is less effective for high-frequency operations [5], [8], [11].

In contrast, the Current Steering DAC utilizes matched current sources and switching transistors, achieving superior linearity, speed, and dynamic performance. Simulation results confirm near-ideal DNL and INL values, with faster settling and improved stability across both resolutions [3].

Overall, while the R–2R Ladder DAC remains suitable for low-power and moderate-precision systems, the Current Steering DAC demonstrates enhanced performance, scalability, and accuracy, making it the preferred choice for high-speed mixed-signal and communication circuits [5], [8], [11].

VI. CONCLUSION

In this work, R–2R Ladder and Current Steering Digital-to-Analog Converters (DACs) with 3-bit and 5-bit resolutions were successfully designed and simulated in *Cadence Virtuoso* using the *Spectre* simulator. The simulation results demonstrated accurate and monotonic digital-to-analog conversion for both architectures, validating their functionality and design accuracy. The R–2R Ladder DAC exhibited excellent linearity, simplicity in implementation, and low power consumption, making it well-suited for low-to-

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medium speed applications where compactness and design predictability are desired. Conversely, the Current Steering DAC achieved higher operating speed, improved dynamic performance, and lower glitch energy due to its current-mode operation [1], [2], [3].

The DNL and INL analyses confirmed that both architectures-maintained deviations within acceptable limits, ensuring reliable linear behavior. The comparative evaluation highlighted that while the R–2R structure provides an efficient solution for moderate-resolution systems, the Current Steering approach is more effective for high-speed, high-frequency, and precision mixed-signal applications. Overall, both DAC architectures achieved their intended design goals and demonstrated robustness in performance, confirming their reliability, scalability, and suitability for integration in modern CMOS-based VLSI systems and future mixed-signal integrated circuits requiring optimized accuracy and speed.

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