REDUCE POWER CONSUMPTION OF SHIFT REGISTER BY GDI TECHNIQUE

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Abstract :- **In the previous paper, present an application of a 4-bit SISO shift register by making use of a combination of ADOC schema & RTPG. They have also suggested Activity-Driven Fine-Grained CG & RTPG integration. Initially, an ADOC (Activity Driven Optimized Clock Gating Schema) is presented for enhancing the conventional CG based over XOR logic gate. It selects a sub group of flip flops that are gated over a selective basis. Further we incorporate RTPG that is implemented to each of the flip flop. The ADOC schema produces clock enable signals that are applied like sleep signal to each of the PG cell. This assessment is conducted by making use of Tanner EDA by implementing 250 nm methodology. The outcomes of simulation express that SISO shift registers along the RTPG & ADOC technology is 72.03% more efficient than the SISO shift register. In this paper, the XOR logic gate is replaced by NAND logic gate & the GDI methodology is also applied for minimization of consumption of power in the circuitry. The OR gate is replaced by OR gate based over GDI technique. This GDI methodology has the ability of minimizing the consumption of power in the circuitry.**

Keywords— Power Gating; Clock Gating; Activity-Driven Optimized Clock-gating; Run Time Power Gating; Serial Input Serial Output Shift Register.

I. INTRODUCTION

In the digitized circuitry, a shift registers is considered to be cascade of flip flops having a single clock, where outcome of every Flip Flop is linked to 'data' input of the succeeding the flip flop in the chain, that will lead to formation of a circuitry of chain, that results for production of a circuitry that get shifted by one place in the 'bit array' accumulated in it, that shifts the present data over the input & shifting out of the last bit in array, that shifts in the data provided in input & shifting the data from last bit in an array on every transition of clock input.

Basically, a shift register can be of multidimensional form, so that the 'data in' & stage outcomes are bit arrays by themselves. It is applied by implementing various shift registers of same type of bit length in parallel form.

Shift registers may be comprised of both of the serial & parallel form of inputs & outcomes. These are generally referred as SIPO or PISO. There are some forms that are comprised of both of the parallel & serial input forms with parallel & serial outcome. They are also termed as 'bidirectional' shift registers that helps for shifting in both of the directions: L→R or R→L. The serial form input & last outcome of shift register can be linked to produce a 'circular shift register'.

Shift registers are the form of sequential logical circuitry precisely for accumulating the digitized data. They are considered to be a set of flip flops that are linked in form of chain where outcome from one FF becomes the input for succeeding flip flop. Many of the registers are comprised of no attributable internal sequence of states. Every flip flop is triggered by the same clock & all the data lines are reset or set simultaneously.

In some of the lectures, some general shift registers are examined, like SISO (serial in- serial out), SIPO (serial in- parallel out), PISO (parallel in- serial out), PIPO (parallel in- parallel out) & bidirectional shift registers. A specialized form of counter – shift register is also provided.

A. Register

- A group of n flip-flops
- Every flip-flop accumulates one bit
- Two general functionalities: data movement & data storage.

B. Shift Register

- A register that permits every FF to pass the accumulated data to adjoining associates.
- The diagram presents a general movement of data in shift registers.

C. Counter

A register that pass through predetermined state sequence

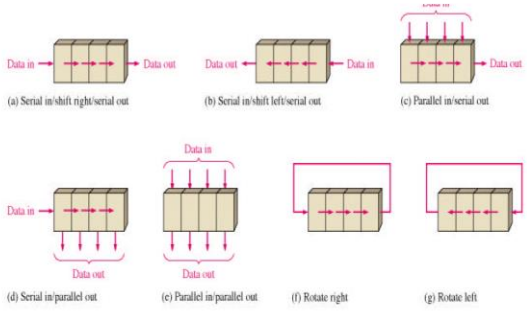

Fig 1:- Basic data movement in shift registers

D. Storage Capacity

The storage capacity of the register is aggregated number of bits (either 1 or 0) of the digitized data it is able to accumulate. Every state (in Flip Flop) is shift register that presents one bit of storage capacity. Hence, the number of stages in the register obtains its storage capacity.

E. Serial In And Serial Out

These are the basic shift registers. The data string is provided over 'Data In' & is shifted to one place on right side on every instance when 'Data Advance' is kept high. On every advance, bit on the far left side (i.e. Data In) is shifted over the outcome of first flip flop. The bit over extreme right side (i.e. Data Out) is shifted & lost.

The data accumulated after every flip flop on the 'Q' outcome. Hence, there are four slots of storage provided in the design. Therefore it is termed as 4-bit register. So, to obtain an idea related to pattern of shifting, it is presumed that the register accumulates the value of 0000 (hence all the slots of storage remain empty). As the order of 1,0,1,1,0,0,0,0 is presented by Data In (the order having a pulse at 'Data Advance' for every instance it is termed as storbing or clocking) to register, it is the outcome. The column at left hand side leads to left-most FFs output pin & so on.

Hence, the serial form of outcome from complete register is 10110000. It is observed that if data is continued towards input, exactly the same value will be obtained as outcome, though offset is through the four 'Data Advance' cycles.

This design is equivalence to hardware of queue. Even at an instance, we can set the complete register to zero by raising the reset (R) pins to high.

This design executes a destructive readout- every datum gets lost as it is been transmitted out from right-most bit.

The SISO (serial in serial out) register intakes the data in serial form, which is a single bit on an instance over single line. It generates the accumulated data on the outcome side in serial format.

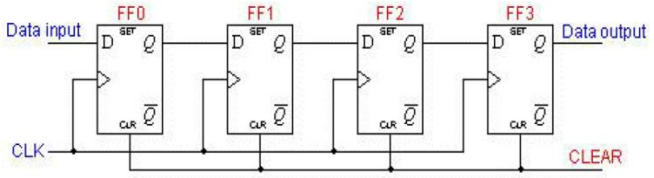

Fig 2 :- Serial In Serial Out

A general 4-bit shift register is produced by making use of four D-FFs as presented in figure. The working of the circuitry is presented as below:

- Initially, the register is cleared that forces all of the four outcomes to zero.
- The input data is implemented in a sequential manner to D input of initial flip flop in the left side (FF0).
- In every clock pulse, a bit gets shifted from left side to right.
- The data word to be presumed as 1001.
- The least significant bit of data must be shifted by register from FF0-FF3.

For obtaining the extracted data from register, their shifting must be performed serially. This can be performed either in a destructive or non-destructive manner. For the destructive form of readout, the actual data gets lost & on the end of read cycle, every FF gets reset to zero.

FF0	FF1	FF2	FF3	
0	0	0	0	1001

Fig 3 :- Bit Transfer in SISO

The data is stacked over the register as the control line is HIGH (i.e. WRITE). The data might be transferred out from the register when value of control line is LOW (i.e. READ).

Clear	FF0	FF1	FF2	FF3
1001	0	0	0	0
WRITE:				
FF0	FF1	FF2	FF3	
1	0	0	1	0000
READ:				
FF0	FF1	FF2	FF3	
1	0	0	1	1001

Fig 4 :- illustrates entry of the four bits 1010 into the register

Figure 4 presents the 4-bits (1010) that is serially shifted out of the resister & it is replaced by the zeros.

F. Serial In Parallel Out (SIPO)

This architecture helps in transformation of serial to parallel data format. The data is provided in serial form as presented in the portion of SISO described above. As the data has been clocked, it can be read over every outcome simultaneously or it can be placed out.

For such registers, the bits of data are invaded in serial form in the same way as described above. The difference is computed in a way the bits are extracted from the register. As the data gets accumulated completely, every bit is presented on the associated outcome line & all the bits are provided simultaneously. The production of 4-bit SIPO registered is presented below.

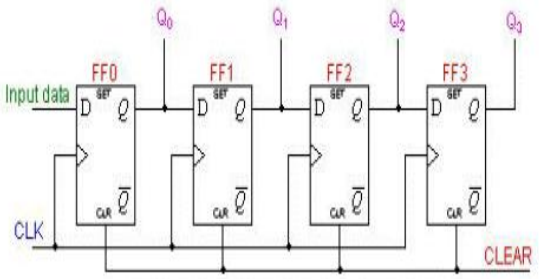

Fig 5 :- Serial in Parallel Out

In the provided table, the shifting of 4-bit binary number 1001 to Q outcome of the register is presented.

Clear	FF0	FF1	FF2	FF3
1001	0	0	0	0
	1	0	0	0
	0	1	0	0
	0	0	1	0
	1	0	0	1

Fig 6 :- Bit transfer in SIPO

G. Structure And Design Of Shift Register Using Integration Of ADOC & RTPG

The D-FF generates the transitions that go in accordance to the input 'D' after identifying the input. This FF is responsible for accumulation

of values present on the data line. It can be considered as a general memory cell. The presented diagram illustrates the internal schema of D-FF by making use of NAND logic gates [3].

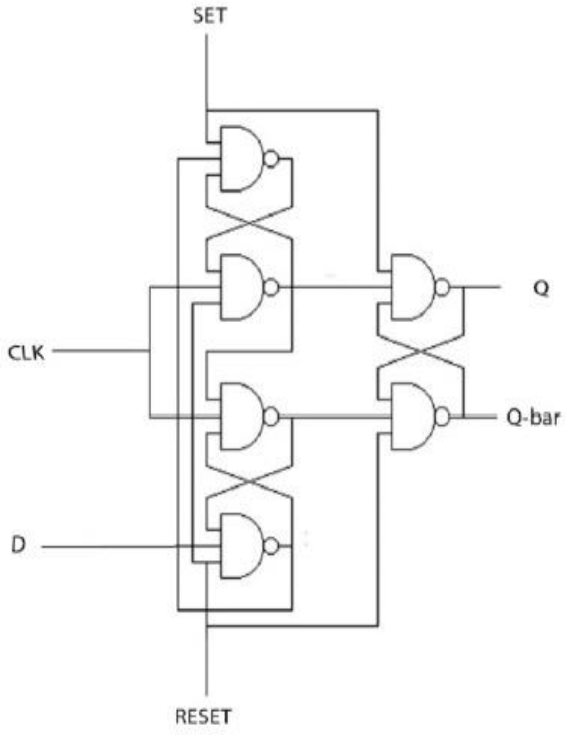

Fig. 7 :- Schematic of D Flip-Flop using NAND Gate

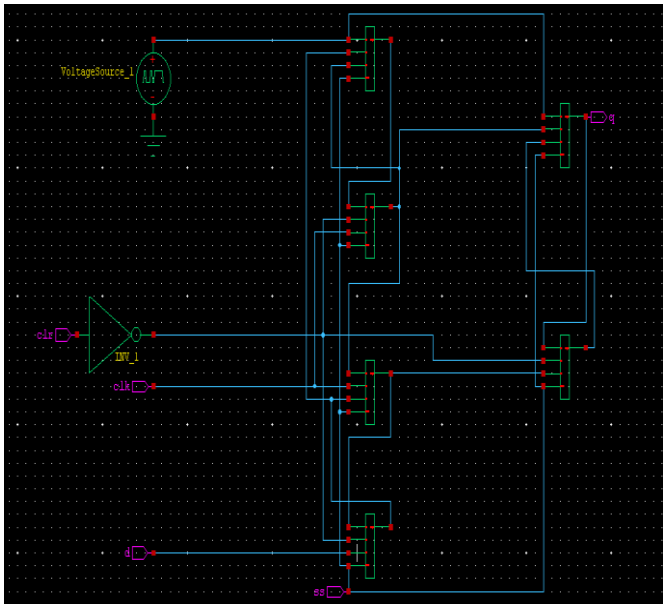

Fig 8 :- Schematic of D Flip-Flop using NAND Gate tanner design

The provided diagram presents several internal architectures of CMOS NAND gate that are applied during implementation of D-FF.

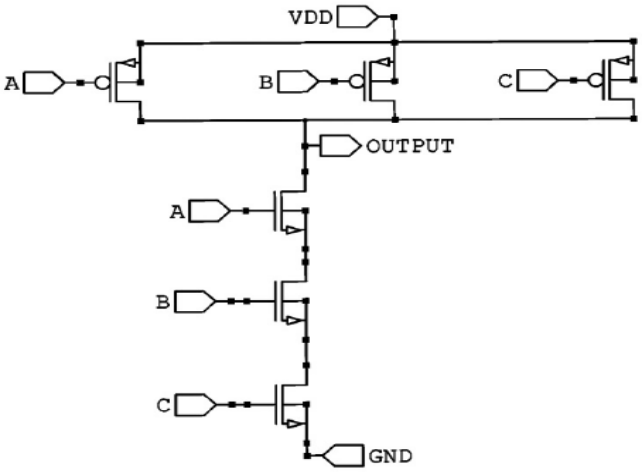

Fig. 9 :- CMOS NAND Schematic

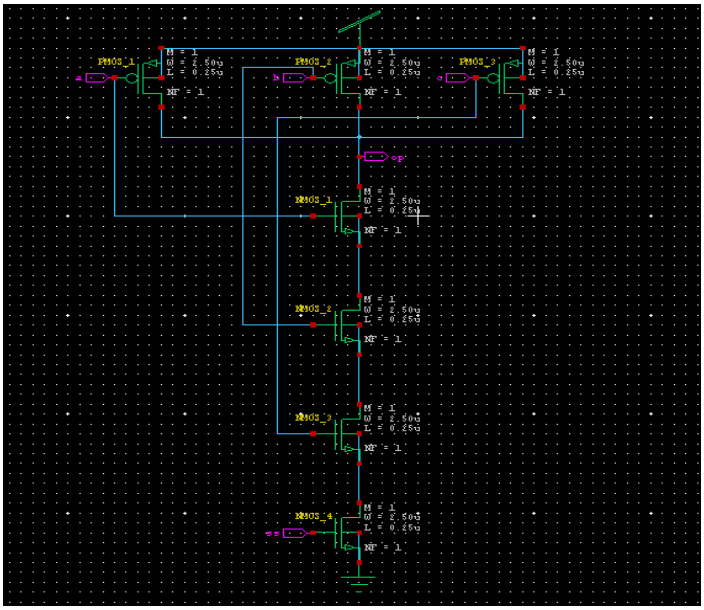

Fig 10 :- CMOS NAND gate design by tanner tool

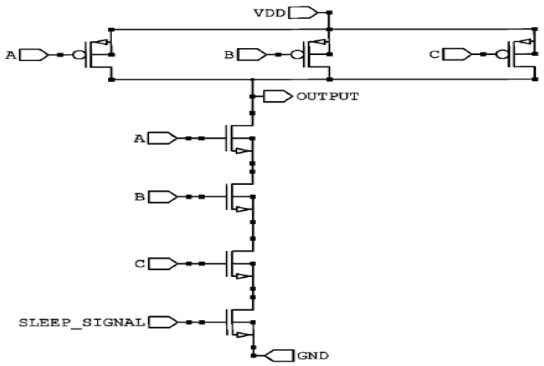

Fig. 11 :- CMOS NAND Schematic with Single footer PG scheme

H. Double Footer PG Scheme

A D-FF is applied through the NAND logic gates that follow up thr presented schema of the diagram & the single & double footer PG schemas are also incorporated in it.

I . 4 Bit Serial Input Serial Output Shift Register

A shift register is produced by cascading the FFs that share a single clock & the outcome of one flip flop is considered to be the input for the succeeding flip flop in a chain like structure. This leads to formulation of a circuitry which shifts the bit array accumulated in it by one place, shifting the data located on the input side & shifting of last bit in the array on every transition of clock input.

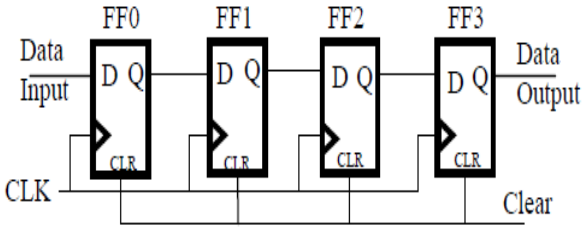

Fig. 12 :- Four bit SISO Shift Register

On the initial basis, CG is applied to each of the FF which is a SCG circuitry. We evaluate the consumption of power by SISO Shift Register, SCG circuitry of Shift Register, with the PG schema & without single & double footer PG schema. The produced clock enable signal act like sleep signal to each PG cells.

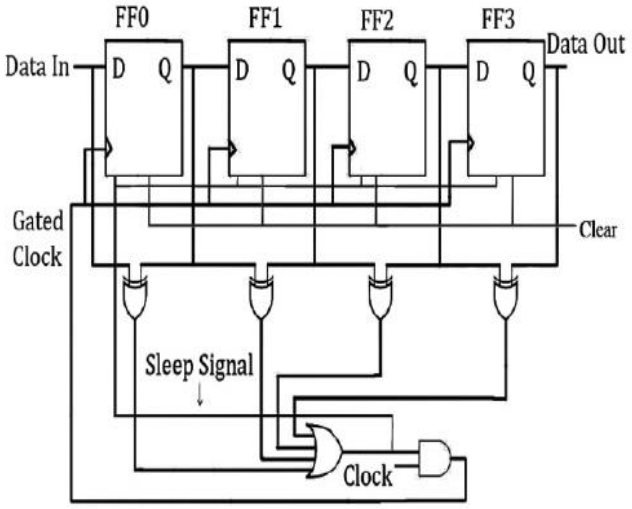

Fig. 13 :- Four bit SISO Shift Register with SCG & RTPG

In order to obtain better results for minimizing the dynamic power, the suggested PSCG circuitry is applied after implementation of SCG circuitry. On the starting basis, a single FF is selected & CG is implemented over it. RTPG is integrated into it later on. This procedure is repeated by selection of two FFs that are further made to three in number. Both of the PG schemas (i.e. single & double footer) were implemented over the given circuitries.

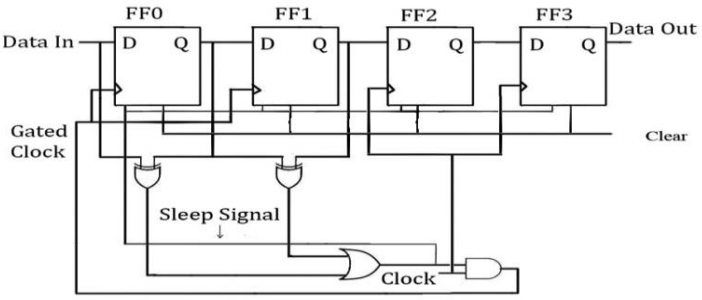

Fig. 14 :- Four bit SISO Shift Register with ADOC & RTPG applied to only two FFs

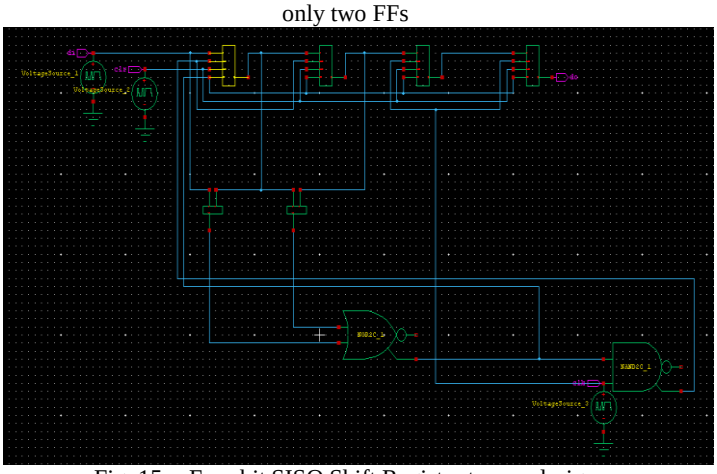

Fig. 15 :- Four bit SISO Shift Register tanner design

II. PROBLEM STATEMENT

In the previous paper[23], implementation of 4-bit SISO designed shift register is presented through a combination of ADOC (Activity Driven Optimized Clock-Gating) schema & RTPG (Run Time Power Gating). An integration of RTPG & Activity-Driven Fine-Grained CG is also displayed. Initially for achieving the job of enhancing the conventional CG based over XOR logic gate is suggested by applying ADOC schema. It makes selection of sub-groups of flip flops on the selection basis, and then RTPG is applied to each of the FF. Further, clock enable signal is applied in the form of sleep signal that is produced by ADOC schema to each of the PG cells. In the base document, we work over a basic XOR gate that absorbs more amount of power. As observed from the diagram, a basic XOR gate is used that is implemented in both of the SISO circuitries along the RTPG & ADOC. The power of outcome is improvised if the consumption of power by XOR logic gate is reduced.

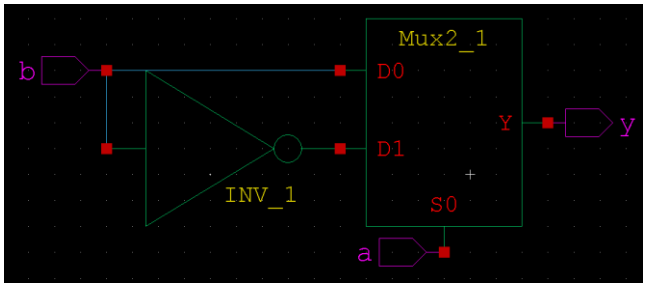

Fig 16:- XOR gate design in TANNER

III. PROPOSED METHODLOGHY

A. Methodology 1

In this suggested design, the OR gate circuitry is replaced by the OR gate based over GDI in order to minimize the consumption of power. This GDI (Gate Diffusion Input) methodology is suggested in [2] & [3], that is some sort of PTL (pass transistor logic) circuitry that makes use of two-transistor cells for implementation of logical function with minimized complicacy. The swing in voltage of internal nodes is very less that minimize the consumption of dynamic power. The OR gate circuitry is replaced by the OR gate based over GDI. As observed from the diagram, applied Or gate is emphasized by the red mark. This marked circle Or gate is replaced by the OR gate based over GDI.

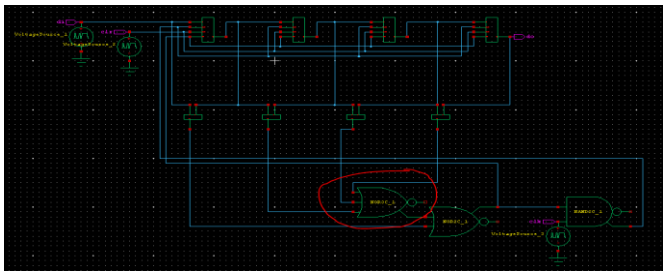

Figure 17 :- SISO normal design

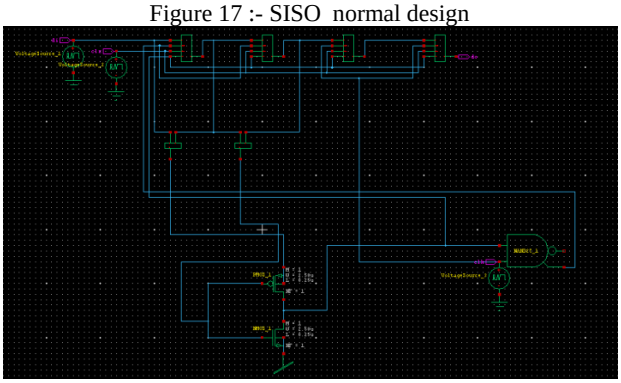

Figure 18:- Proposed Design of SISO

As observed from the picture, a general OR gate is replaced by OR gate based over GDI. With the help of this we can minimize the aggregated consumption of power.

B. Methodology 2

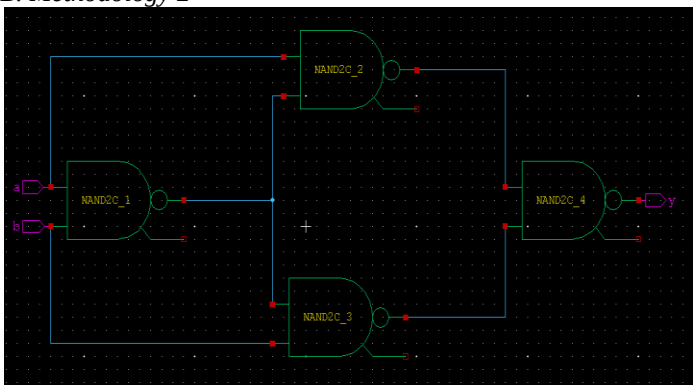

Fig 19 :- XOR gate design by NAND gate

In this structure, four NAND gate transistors are applied where a & b are considered to be inputs. The outcome is obtained from y. It is the XOR gate that is used with help of NAND gate. It will absorb less amount of power.

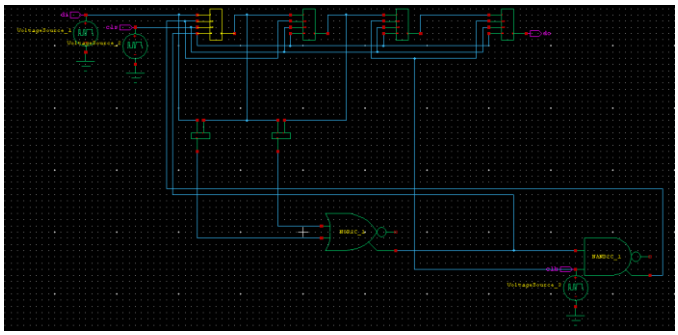

Fig 20 :- Proposed SISO with NAND gate based design XOR gate

A latest design of SISO is produced with the help of XOR logic gate that is based over NAND gate. Here the XOR gate is applied for two times. In this circuitry di & clear are taken as inputs of SISO structure while do is the outcome.

In the earlier designs [23] a 4-bit SISO design is produced. In this circuitry we design a XOR logic gate that absorbs more amount of power. as per the outcomes of power, the value of power is obtained as 1.656598e-004 W as per the outcomes of T-Spice, XOR gate is absorbing more amount of power.

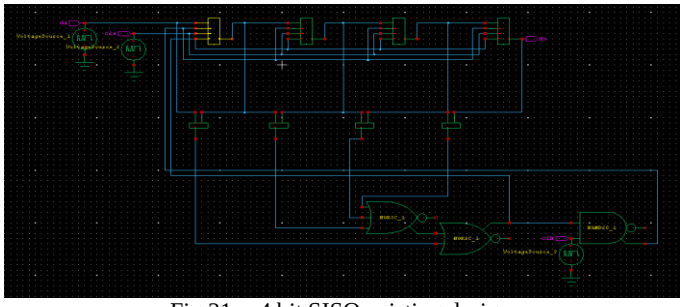

Fig 21 :- 4 bit SISO existing design

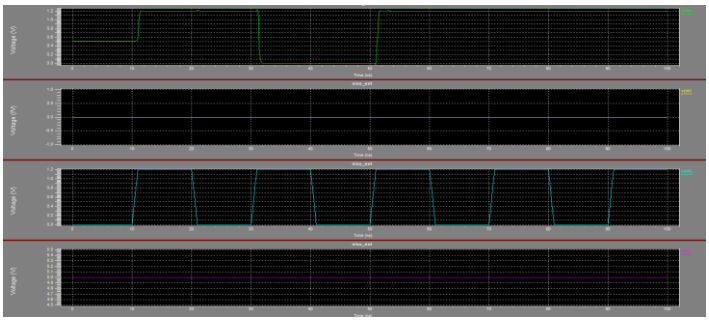

Fig 22 :- Output waveform of the existing SISO circuit

As observed from the images of outcome waveform, there are three values of input di, clk & clr. As from the image, we see that input value is 5V which means that logic is 1. Over the ‘do’ outcome from picture of waveform, it is provided that outcome of logic 1 is obtained after every three cycles.

IV. PROPOSED DESIGN

In the suggested design, a 4-bit SISO design is produced with the help of XOR gates constituted over NAND logic gate that absorbs low amount of power than the current implemented design. As per the outcomes, the obtained power is 1.231972e-004 W from the outcomes of T-Spice. The XOR gate based over NAND gate requires low power.

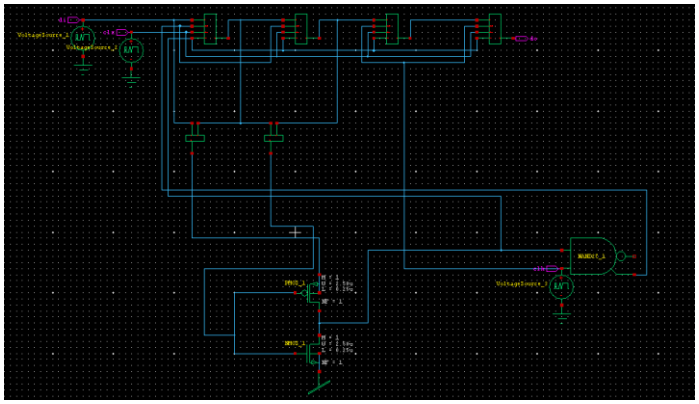

Fig 23 :- Proposed 4 bit SISO design with NAND gate based XOR gate

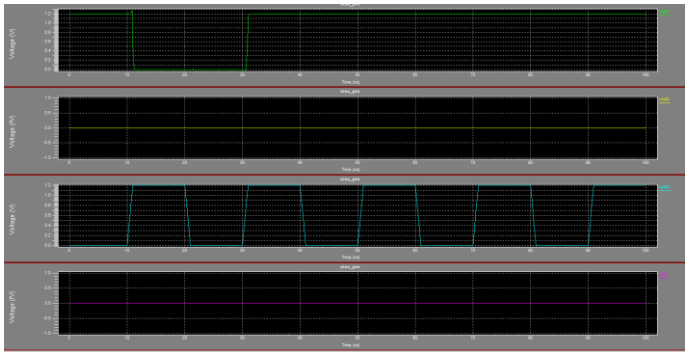

Fig 24 :- Proposed design SISO output waveform

As observed from the images of outcome waveform, there are three values of input di, clk & clr. As from the image, we see that input value is 5V which means that logic is 1. Over the 'do' outcome from picture of waveform, it is provided that outcome of logic 1 is obtained.

	Power(W)
Existing Design	1.656598e-004
Reference paper [1]	5.62 e-003
Reference paper [2]	4.40010 e-004
Proposed Design	1.231972e-004

Table 1 :- Comparison Table

V. CONCLUSION AND FUTURE SCOPE

We suggested a RTPG & fine-grained CG that is constituted over 4-bit SISO by implementation of enhanced XOR along the NAND gate which further choose sub-group of FFs for gating. Even, the enable signals of clock produced in an ADOC circuitry can be applied like sleep signal in RTPG. We implement a NAND gate structure based over low amount of power for a XOR gate design. As from the outcomes, it is observed that from a general XOR gate, the outcome obtained is 1.656598e-004W. Further, we enhance the performance of ar-bit SISO and a NAND logic gate based over XOR logic gate is applied for this purpose. As from the outcomes, we observe that the suggested methodology minimize the consumption of power. the power given as outcome is 1.231972e-004 W for the suggested technology.

With furtherance, we work over enhancing the produced outcomes by implementing the GDI technique with the help of clock gating. This GDI (Gate Diffusion Input) is a latest methodology of a digitized circuit design with less power. This methodology helps to deduct the consumption of power, area complicacy of digital circuitries. We are working over improvising the performance of digitized system by using the technique of clock gating. Clock gating technology will help us in minimizing the consumption of output power. Hence, by this technique, we will be able to minimize the quantity of embedded transistors & power.

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