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Improve Performance of ZTCAM Architecture

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Abstract :- **The requirement for the storage has raised day by day. The searching mechanism of data in the memory is mainly faced by the users these days. It also increases consumption of power, access time & cost. The designs of TCAM constituted over SRAM are referred as ZTCAM is a special memory type that takes search word as input & out-produces address of that word that is stored over data bank. The traditional TCAM table is logically split by ZTCAM through columns & rows and performs it over to associated memory blocks. In the searching process, memory blocks are evaluated by the associated sub words of input word & match address is generated. As compared to the RAM, TCAM has to deal with some limitations like we put the RAM, TCAM in contrast to each other that have some limitations like slower access time, less storage density, complicated design & high cost. In this paper, we have proposed a low costing & area effective novel design for TCAM based over SRAM called ZTCAM that imitates working of TCAM. The traditional TCAM table is split into rows & columns in hybrid TCAM sub parts & their mapping is done as per related memory blocks, in search operation memory blocks are assessed through their related sub words of input words & a match address is provided. In modified design like OATAM table is eliminated and a mapping is performed from VMs to OATs. This minimizes utilization of resources by usage of memory & therefore improves speed & performance. It is a tough job to design & map OATAM tables as the number of bits in input word increase the size of OATAM table. Therefore as OATAM table is eliminated, VMS is mapped to OAT & therefore TCAM functionality is achieved.**

Keywords: *TCAM, Hybrid partitioning, Application-specific integrated circuit, memory architecture, priority encoder.*

I. INTRODUCTION

CAM signifies Content Addressable Memory that is considered as a special memory implemented in Cisco switches. In a case of standard RAM, IOS requires memory address for obtaining the data stored over this location of memory, where IOS & CAM produces an inverse. It makes use of data while CAM returns those addresses over which information is accumulated. Also, CAM works at a faster speed than the RAM as CAM search whole of the memory in one state. CAM tables produces only two outcomes: 0 (true) & 1 (false). [8]

Ternary Content Addressable Memory is abbreviated as TCAM that is considered as expansion of CAM that can get in accordance to a third state that is any value. Hence, TCAM becomes a major constituent of Cisco Layer3 switches & latest routers, as they are capable of storing routing table in TCAMs while permitting for faster lookups that works in a better manner than routing tables accumulated in general RAM. TCAM is a specialized form of CAM that is designed for table lookups in fast manner [8].

TCAM is a cell comprising two SRAM cells & comparison circuitry & also furnish three states called as: 0, 1 & x in which x are referred as don't care state. The x is referred as match that is not linked to an input bit. TCAM produces a single clock lookup having persistent searching time that make it appropriate as per applications like network routers, real time pattern matching, data compression in virus recognition & image processing.

A TCAM that is designed with help of SRAM is inferred as ZTCAM as even though the table creates a lookup for whole of the table in single clock, it is having various drawbacks when it is put in contrast to SRAM. TCAM cells & comparator circuitry adds complexity to the TCAM design. The access time for a TCAM us 3.3 time more than SRAM because of huge parallelism [5]. Complicated integration of logic & memory also increase the time of testing in TCAM [3]. The costing of TCAM is 30 times higher for every bit than SRAM [6]. Even though the attributes like delay, area & power can be minimized through STT RAMM apart from SRAM [1] that is demonstrated in this project.

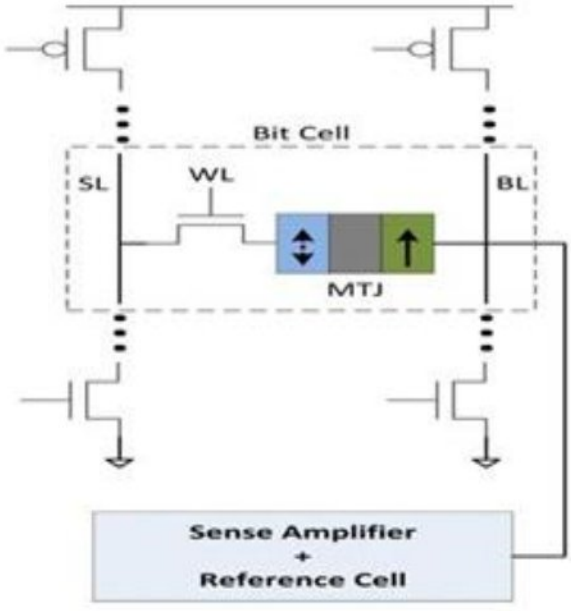

Fig 1:- Circuit diagram of STT RAM

ADDR	SW1	SW2	Layer
0	00	11	1
1	01	01	1
2	0X	11	2
3	11	1X	2

Table 1:- Traditional TCAM table and its hybrid parameters

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ADD	0	1	2	3
VM11	1	1	0	0
VM12	0	1	0	1
VM21	1	1	0	1
VM22	0	0	1	1
OATAM1	0	0	-	-
OATAM1	-	0	-	1
OATAM2	0	1	-	2
OATAM2	-	-	0	1

Table 2:- Z-TCAM example: Data Mapping

ADDR	OAT11 01	OAT12 01	OAT21 23	OAT22 23
0	10	01	10	01
1	01	10	10	11
2	00	00	01	00
3	00	00	00	00

Table 3. Z-TCAM Original Address Mapping

A. Hybrid Partitioning Of TCAM

HP (Hybrid portioning) is considered as a combination of vertical & horizontal portioning of traditional TCAM table. An illustration for HP is provided in Table 3.1 [1]. The conventional table is portioned by HP in vertical & horizontal manner to TCAM sub tables which are further processed to be stored in the associated memory units [34].

VP (vertical portioning) implicates that portioning is performed over TCAM word of C bits to N sub words for every sub word of w bits. The VP is applied for minimizing the size of memory to possible extent. HP (horizontal portioning) splits every vertical partition through range of real addresses in a conventional TCAM table to L number of horizontal partitions. HP cannot be used as a sole as it consumes much power, area & cost while it can be used for producing layers. HP produces aggregated L x N hybrid partitions.

The dimensions for every hybrid partition are obtained as K x w in which K is considered to be a subset of real addresses & w is number of bits in every sub word. The hybrid partitions presenting similar addresses are considered under same layer. As an illustration, HP21 & HP22 span similar address range & are considered under layer 2.

B. Architecture Of Z-TCAM

The aggregated design of Z-TCAM is presented in Figure 3.1 in which every layer demonstrates the layout as presented by Figure 3.2. It comprises L layers & CPE (CAM priority encoder). Every layer produces PMA (potential match address) as output. The PMAs are given as input to CPE that chooses MA (match address) between PMAs.

C. Layer Architecture

This theory explains the layout with two layers: Layer 1 & Layer2. Figure 2 demonstrates architecture of Layer 1. It is comprised of 2 VMs (validation memories), 1-bit AND operation, 2 OATAMs (original table address memories), 2 OATs (original address tables), K-bit AND operation & LPE (layer priority encoder).

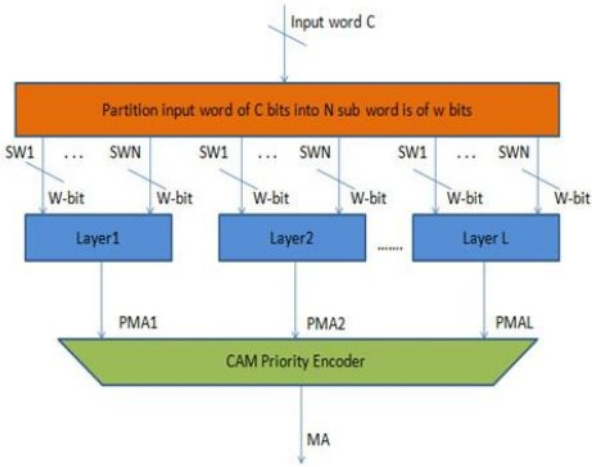

Fig 2: Architecture of Z-TCAM.

D. Validation Memory

Size of every VM is computed as 2w x 1 bits in which w stands for number of bits in every sub word & 2w signifies number of rows. The sub word w demonstrates that it possess aggregated 2w combinations where every combination express a sub word. As per an example, is w is having 4 bits, then it signifies that there are 2^4 = 16 number of combinations. This definition is linked to OAT & OATAM. Every sub word works like an address for VM. If the location of memory invaded by sub word is in high state then input sub word exists or else it is not present [34].

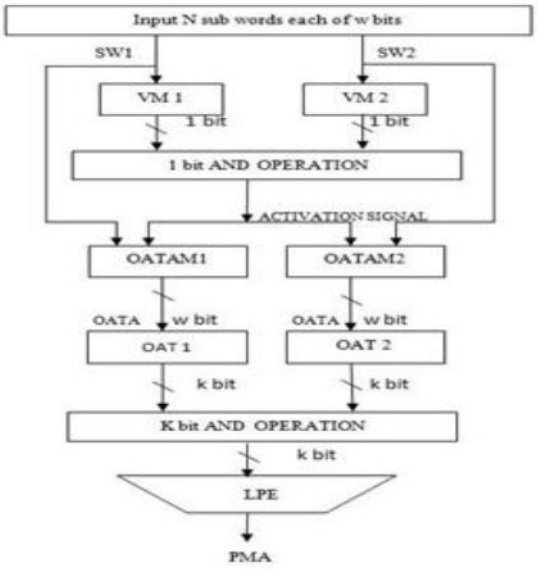

Fig 3: Architecture of a layer of Z-TCAM

Hence, the input sub word is validated by the VM if it is located there. As per table 3.2, VM11 & VM12 are linked to Layer 1 whereas VM21 & VM22 are associated with Layer 2. As an illustration, mapping of sub words 00 & 01 is performed in VM 11while mapping of sub words 01 & 11 is performed over VM12 etc. This also express than memory locations 00 & 01 must be high in VM11 whereas remaining memory locations are set as low as their associated sub words are not present.

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E. 1-bit AND Operation

It perform AND operation over all VMs. The outcome produced by 1-bit AND function determines continuity of search action. In a case where outcome of 1-bit AND operation is high, then it allows continuity of search operation, or else there will be a mismatch in correspondence layers.

F. Original Address Table Address Memory

Each OATAM is of 2w × w bits where 2w is the number of rows and each row has w bits. In OATAM, an address is stored at the memory location indexed by a sub word and that address is then used to invoke a row from its corresponding OAT. If a sub word in VM is mapped, then a corresponding address is also stored in OATAM at a memory location accessed by the sub word. For example, Table 3 shows OATAM21 where addresses are stored at the memory locations 00, 01, and 11.

The outcome of OATAM is referred as OATA. Hyphen "-"signifies that the associated memory location is containing no information as this corresponding sub word for memory location is not provided in VM. The STTRAM is applied for realization of OAT & OATAM [34].

G. Original Address Table

The dimensions of OAT are considered as2w x k where w is considered as number of bits in sub word, 2w signifies number of rows & K presents number of bits in every row where every bit presents an actual address. Here K is considered as subset of actual address obtained from TCAM table. This is OAT that stores the real addresses. As an illustration, OAT is demonstrated in Table 3 where 1 signifies that a ub word is present over mentioned real address.

H. K-bit AND Operation

It performs AND over every bit over read out K-bit rows from every OAT & the outcome is fed to LPE.

I. Layer Priority Encoder

As we are emulating TCAM & several matches can exist in TCAM [17], LPE chooses PMA from outcomes of K-bit AND operation.

J.. Z-TCAM Operations 4.1 Data Mapping

Conventional TCAM table is logically portioned into hybrid partitions. Every hybrid partition is expanded to a binary version. Therefore, firstly x is expanded into 0 & 1 states that are accumulated in SRAM. As an illustration, if we are having TCAM word of 010x, then it is presented into 0100 & 0101. Every sub word, working in form as address, is applied to its associated VM & logic "1" is written over memory location. This similar sub word is implemented over associated OATAM & w data bits are written over those memory locations. In the searching process, the w bits work like an address for OAT. The K bits are also written over memory location in the OAT that is presented by the associated OATA. Therefore by this, mapping of each hybrid partition is performed. A sub word can be assumed as hybrid partition which is located over several locations. Hence, it is mapped over associated VM & its actual address is mapped to its respective bit with respect to OAT [40].

As a single bit in OAT refers to actual address, the memory locations in which VMs & address positioning actual addresses in OATs are high are mapped whereas remaining memory locations & address positions are set as low in OATs & VMs. As an illustration, data mapping is demonstrated in Table 2. Table 1 is used for mapping Z-TCAM. We have considered N = 2, L =2, K = 2 & w = 2. After the required processing, HP11, HP12, HP21 &HP22 are mapped over their associated memory units. In the given example, we have mapped hybrid partitions of layer 2 to the associated memory units. It is easy to map hybrid partitions of layer 1 in the similar manner.

Steps	Activity
1	Sub-word 1 =00 Sub-Word2 = 11
2	Sub-word1 is applied to VM21 Sub-word1 is applied to VM22
3	Read -Out bit from VM21=1 Read Out bit from VM22 = 1
4	Have all VMs Validate their Corresponding sub - words ?
5	Yes , so sustain search operation
6	Read Out Data from OATAM21 = 0 Read out Data from OATAM22=1
7	Read Out Data From OAT21 =10 Read Out Data from OAT 22 =11
8	K-Bit And operation Result =10
9	PMA= 2

Table 4.Example of a Search Operation in Layer 2 of Z-TCAM

II. PROBLEM STATEMENT

The demand for memory has been increased tremendously day by day. The searching operation of data in memory and area are the main problem that are faced by the user. It increases power consumption, cost and access time. The SRAM based architecture of TCAM known as ZTCAM is a special type of memory, which receives an input search word and returns the address of that word which it is stored on its data bank. ZTCAM logically divides the classical TCAM table along columns and rows into hybrid TCAM sub tables and then maps them to their corresponding memory blocks. When compared to RAM, Ternary Content Addressable Memories (TCAMs) suffer from certain limitations such as low storage density, relatively slow access time, low scalability, complex circuitry, and higher cost. A low cost and an area efficient novel architecture for SRAM based TCAM known as ZTCAM which emulates the functionality of TCAM.

During search operation, the memory blocks are accessed by their corresponding sub words of the input word and a match address is produced. In the previous circuit , OATAM (Original Address Table Address Memory) block was using .That is a main issue for hogh circuit complexity and delay. We can further reduce the delay and LUT from the existing design delay and LUTs.

A. ISSUE 1 :- High Circuit Complexity of ZTCAM

As we have been mention , that in the previous design OATAM layer is using for address the memory . The use of OATAM is just to provide the memory address for the OAT table . OATAM layer is producing high complexity for the ZTCAM design . That can be further reduce .

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B.ISSUE 2 :- High delay of ZTCAM

OATAM layer is producing the delay which is cause of high delay . The delay can be further reduce after remove OATAM layer from the ZTCAM circuit .

III. PROPOSED METHODOLOGY

Modification to existing TCAM architecture using SRAM is done by bypassing OATAM. The modified architecture connects the VMs directly to corresponding OATs and thus achieve the TCAM operations through correct data mapping. The main advantages of this modified structure is that less resources thus less memory usage and resource utilization. Speed of operation is increased.

In the modified architecture the OATAM table is eliminated and direct mapping from VMs to OATs is done. This helps in reducing much resource utilization to be reduced and by reducing memory usage the performance and speed is improved. The OATAM tables are very difficult to design and map, and as the number of bits in the input search word increases the OATAM table size also increase enormously. So by eliminating the OATAM table we mapped the VMS directly with OATs and thus achieved the TCAM functionality.

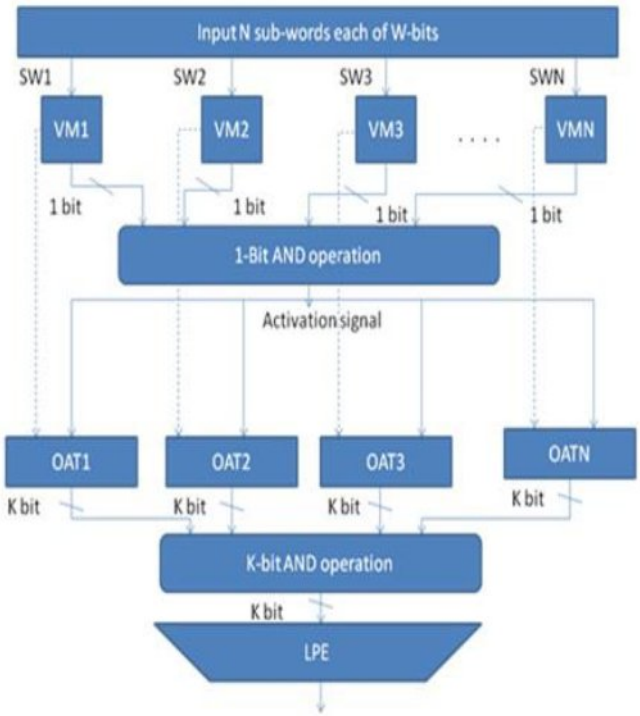

Figure 4:- Modified architecture for TCAM

IV. RESULTS

Propose ZTCAM is design in Xilinx ISE 6.1 for FPGA device Spartan 3 with device XC3S50 and Package is PQ208. As fig 5 is showing the RTL schematic for the propose ZTCAM . In the propose ZTCAM OATAM layer is remove and the address is transferring in the OAT layer Directly .

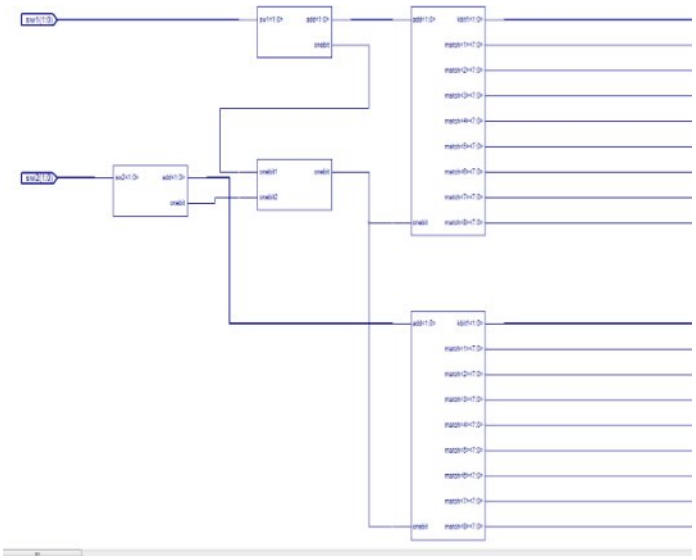

Fig 5 :- RTL design for Propose ZTCAM

```
Timing constraint: Default path analysis
Delay:              8.329ns (Levels of Logic = 3)
  Source:           sw1<0> (PAD)
  Destination:      add<1> (PAD)

  Data Path: sw1<0> to add<1>
                                Gate     Net
    Cell:in->out      fanout    Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2    1.492    0.465  sw1_0_IBUF (sw1_0_IBUF)
     LUT3:I0->O            1    0.720    0.240  p5_c<1>1 (add_1_OBUF)
     OBUF:I->O                  5.412           add_1_OBUF (add<1>)
    ----------------------------------------
    Total                      8.329ns (7.624ns logic, 0.705ns route)
                                       (91.5% logic, 8.5% route)
```

Fig 6:- Delay report for the Propose ZTCAM Design

As fig 6 is showing the delay report for the Propose ZTCAM . In the delay report delay is coming 8.329 ns in which 7.624ns delay is for logic and 0.705 ns delay is for route . That means 91.5 % delay is for logic and 8.5% delay is for route .

```
Number of Slices:                        1  out of    768     0%
Number of 4 input LUTs:                  2  out of   1536     0%
Number of bonded IOBs:                   6  out of    124     4%
```

Fig 7 :- Number of Slices for the Propose ZTCAM

As fig 7 is showing that the number of slices for the Existing ZTCAM is 1 out of 768 . It is 0% of the total number of Slices .Number of slices is showing the occupying area of the system .

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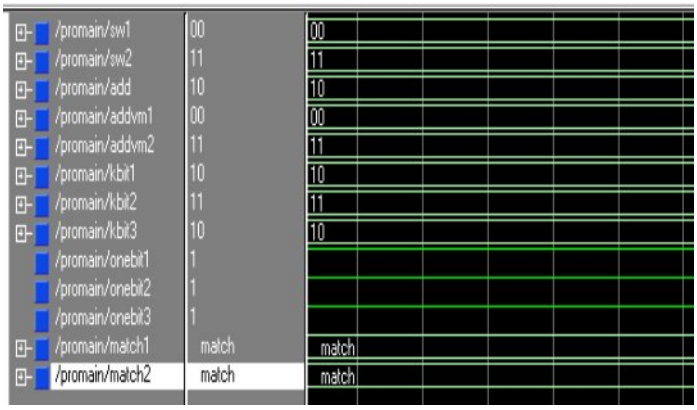

Fig 8 :- Output Waveform of the Propose ZTCAM

As we can see from the Fig 8 , for search the words we give the input of the sw1 and sw2 which is 00 and 11. Match1 and Match2 is showing that the given words are matching or not in the memory address . Add is showing the final memory address of the search words .

6.3 COMPARISON TABLE

	Delay	Number of Slices
Normal ZTCAM(with OATAM layer)	9.408 ns	2
Proposed ZTCAM(Without OATAM layer)	8.329 ns	1

Table 4 :- Comparison Table for the Existing Design and Proposed Design

V. CONCLUSION & FUTURE SCOPE

A. Conclusion

We have designed both TCAM architecture basic using SRAM and a modified version of it. After the simulation in ISE design suite and implementation on the Spartan3 XC3S50 package PQ207 board, we could conclude that modified architecture works better than the current one in terms of resource utilization, power consumption and latency. From the timing analysis it is evident that delay is reduced in the modified architecture for TCAM. As we can see in the results session delay is 9.408ns for the existing ZTCAM design and 8.329 ns for the Proposed ZTCAM design. Delay is getting reduce for the proposed ZTCAM design in which we remove the OATAM layer for the ZTCAM design . So upon considering the above facts we conclude that an efficient structure for TCAM using SRAM is being implemented with certain improvement factors.

B. Future Scope

The future work will be based on designing IP filters based on TCAM. Future work aims to implement TCAM in ASIC and FPGA and to investigate the TCAM field in depth and achieve more designs for SRAM-based TCAM.

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