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A Review for QSD Number Addition / Subtraction

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Abstract:- The need for high speed digital circuits became more prominent as portable multimedia and communication applications incorporating information processing and computing. The drawback of modern computers lead to the deterioration in performance of arithmetic operations such as addition, subtraction, division, multiplication on the aspects of carry propagation time delay, high power consumption and large circuit complexity. This system explores the carry free n digits addition/subtraction as the carry propagation delay is most important factor regarding the speed of any digital system. In this paper ,we are giving the review of papers for the QSD Adder / Subtractor .

Keyword :- *Carry free addition, Fast computing, FPGA, Quaternary Signed Digit, VHDL, VLSI.*

I. INTRODUCTION

In various computers & other processors, adders are implemented in ALUs and also in other portions of processors for calculating the address, table indices & same kind of operations. Even though adders can be generated for various numerical presentations like excess-3 or binary-coded decimal, most of the basic adders work over binary digits. In the cases were negative numbers are presented through two's or one's complement, it is necessary to transform an adder to adder-Subtractor. Some other signed number presentations need a more complicated structurized adder.

A. Quaternary Signed Digit Numbers

QSD digits are present by making use of 3-bit 2's complement notation. Each digit is presented by:

$$D = \sum_i^n x_i 4^i \qquad (1)$$

Here x_i can be taken as any of the value from the set of {3, 2, 1, 0, 1, 2, 3} for generating a suitable decimal representation. A QSD negative number is obtained by complementing a QSD positive number which means the 3 = -3, 2 = -2, and 1 = -1. For digitized implementation, bigger sized digits like 64, 128 and more can be utilized trough a consistent delay. A signed digit number system constituted over higher radix value like QSD helps in more information storage density, low complicacy, less system constituents & low cascading gates & operations. This methodology helps in implementation of area effective & high speed adders & multipliers.

For Example ,

$$(1\bar{2}\bar{3}3)_{QSD} = (23)_{10}$$
$$= 1*4^3 + \bar{2} * 4^2 + \bar{3} * 4^1 + 3 * 4^0$$
$$= 64-32-12+3 = 23$$
$$= (\bar{1}\,2\,3\,\bar{3})_{QSD} = (-23)_{10}$$

B. Adder Design

A faster Arithmetic set helps in elaboration of application domain for faster multipliers in processing of digitized signals, modular exponential, matrix inversion, calculation of Eigen values, digit filters etc. Square roots, calculation of reciprocals, inverse square toots & other elementary functions through implementation of small sized tables, small multipliers & for few functions, a final multiplication is obtained. Addition is taken as a cardinal operation in the field of digital computing. As the size of digits become large, a need of carry free addition is there. This carry free addition can be obtained by exploitation of redundancy in QSD numbers & QSD addition.

$$(6)_{10} = (12)_{QSD} = (2\bar{2}) \qquad (2)$$

Two steps are involved in the carry free addition. In the first step, an intermediate carry & sun from augends & addend is produced. In the next step, intermediate sum of present digit & carry from lower significant digit is combined [3] [6]. There are two rules defined for prevention of carry from rippling. As per the first rule, value of magnitude of intermediate sum must be equal to or less than 2. As per the 2nd rule, value of magnitude of carry should be equal or less that 1. Further, magnitude of outcome obtained in the second step must not be higher than 3 that is presented by a single digit QSD number. Thus, no additional carry is needed. In the 1st step, the possible input pairs of augends & added are taken into account.

Sum	QSD representation	QSD coded number
-6	$\bar{2}\,2\,,\bar{1}\bar{2}$	$\bar{1}\bar{2}$
-5	$\bar{2}3,\bar{1}\bar{1}$	$\bar{1}\bar{1}$
-4	$\bar{1}0$	$\bar{1}0$
-3	$\bar{1}1,0\bar{3}$	$\bar{1}1$
-2	$\bar{1}2,0\bar{2}$	$0\bar{2}$
-1	$\bar{1}3,0\bar{1}$	$0\bar{1}$
0	00	00
1	$01,1\bar{3}$	01
2	$02,1\bar{2}$	02
3	$03,1\bar{1}$	$1\bar{1}$
4	10	10

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5	$11,2\bar{3}$	11
6	$12,2\bar{3}$	12

Table 1 :- The Intermediate Carry And Sum Between -6 To 6

Both of the inputs & outcomes can be encoded in 3-bit 2's complement binary number type. Mapping in the addend, augends, inputs & outputs, sum & intermediate carry are presented in binary form Table 1. As the value of intermediate carry remains in between -1 & 1, only 2-bot binary presentation is needed. At last, five 6-variable Boolean expressions can be extracted.

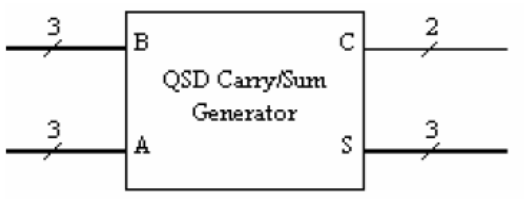

Figure 1. The intermediate carry and sum generator

In the 2nd step, sum generator & intermediate carry from lower significant digit is added to sum of current digit for generating the last final outcome no carry is produced by the addition in this step as carry-in coming from lower digit s absorbed by present digit. All the possible sets of summation generated in between sum & intermediate carry are presented.

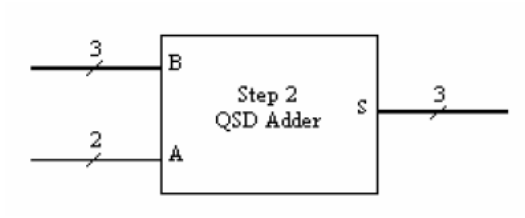

Figure 2. The second step QSD added.

It is possible to extract three 5-variable Boolean expressions. N-QSD carry & sum generators along the n-1 second step adders is needed for implementing an n-digit QSD adder that is presented in the outcomes which comes out to be an n+1 digit number. The outcome obtained by this addition lie in between -3 to 3. As taking a carry is not permitted in this step, the outcome is a single digit QSD output. The inputs are, intermediate carry & sum that are 2-bit & 3-bit binary respectively. The outcome obtained is 3-bit binary representation of QSD number [4] [5].

It is possible to extract three 5-variable Boolean expressions. the implementation of the Boolean equations is done with the help of FPGA tools. The compilation & simulation of Modelism and Leonardo spectrum design is performed. There are two steps in the addition for design of adders. The 2nd step adder is presented in figure 2. N-QSD carry & sum generators along the n-1 second step adders is needed for implementing an n-digit QSD adder that is presented in figure 3. The outcome obtained is n+1 digit number.

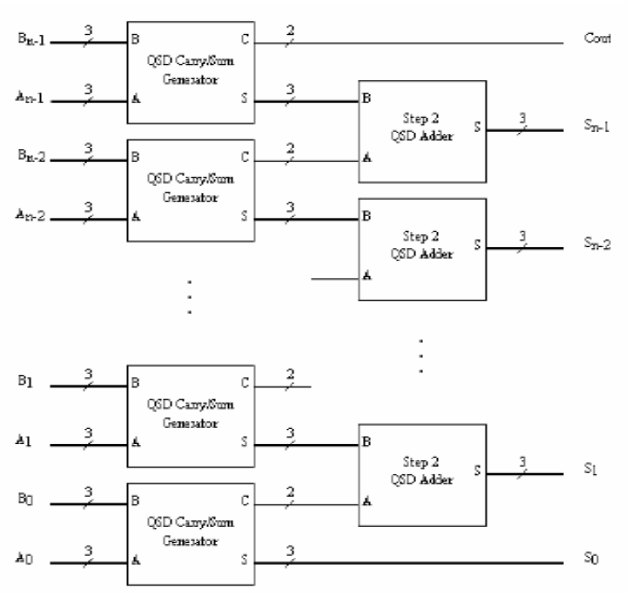

Figure 3 :- n-digit QSD adder

II. LITERATURE REVIEW

In 2011 Kothuru.Ram Kumar[et.al] presented a paper for the speed of computation which is restricted by generation & propagation of carry particularly with increment in quantity of bits. The processes like borrow free subtraction carry free addition & multiplication can be performed through implementation of QSD. Even though, some other logical components based over prime modules are needed for execution of arithmetic functions. An arithmetic function which is carry free is attained through higher radix number system like QSD. In QSD, every digit is presented in range of -3 to 3. This also helps in implementation of complex functions like carry free addition over large bit numbers like 64, 128 or more with persistent delay & low complicacy. Microwind, Modelsim6.0 & Leonardo Spectrum are used in synthesis & simulation of design.

In 2013 Prashant Y. Shende[et.al] presented a paper for the development emerged in electronic circuitries which has taken place of analog circuitries in various fields. The quaternary system has got many advantages when compared to binary logic system. A higher radix number system can help in performing arithmetic functions that are carry free like QSD. A fast multiplier constituted over QSD number system is proposed in this paper in which chain of carry propagation is removed and so it minimizes time of propagation in contrast to radix 2 number system. In a QSD system with n digits, every figure is presented by selecting a number from set of digits [-3, -2, -1, 0, 1, 2, 3]. This carry propagation chain is removed from QSD number system that also minimizes time of computation and so improvising speed of machine.

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The process for simulation & synthesizing quaternary multiplier is executed. The fine performance is obtained through the outcomes with help of quaternary multiplier & quaternary adder implemented over other types of adders because of addition schema which is carry free and leads to persistent delay that is not linked to quantity of input bits. The quaternary multiplier applied along the persistent delay adder generates same value of constant delay through compromise in area. This system can be applied through quaternary adder as the main component.

In 2014 Vadathya Mohan[et.al] presented a paper for the speed of computation which is restricted by generation & propagation of carry particularly with increment in quantity of bits. The processes like borrow free subtraction carry free addition & multiplication can be performed through implementation of QSD. Even though, some other logical components based over prime modules are needed for execution of arithmetic functions. An arithmetic function which is carry free is attained through higher radix number system like QSD. In QSD, every digit is presented in range of -3 to 3. This also helps in implementation of complex functions like carry free addition over large bit numbers like 64, 128 or more with persistent delay & low complicacy [2].

The QSD adder proposed here is superior to various binary adders counted in terms of addition of higher bits & number of gates along the consistent time. The operational speed will also be increased through an efficient layout for performing multiplication & addition operations. QSD number system requires low space than the BSD for accumulation of number; more gates can be deployed for enhancing the QSD adder.

In 2014 Ch.Vishali [et.al] presented a paper for QSD adder with minimal propagation delay. It is more easy to apply binary number system but is comprises some restrictions in terms of complexity, area that gives a hike to propagation delay in the circuitry. QSD number system is applied to deal with these drawbacks. The size of chip gets decreased by ¼ through this system. This research is focused over quaternary addition. Range defined for these numbers will be -3 to 3. Quaternary addition also incorporates carry free addition that minimizes propagation delay.

At last, this research draws a conclusion that QSD adder formulated for addition of single digit is generated with features like optimization of power, less latency & accuracy. The dissipation of dynamic power for project will be 35.6781 over 13 GHz frequencies. The delay of single digit adder is 0.73 ns. This Xilinx 14.7 performs simulation of design & Synopsis Design Compiler synthesizes the design.

In 2013 Prashant Y. Shende[et.al] presented a paper for digital circuitries which operated over high speed are cardinally require with invaded computations & information processing. Arithmetic circuit also has an important role in application specified & general purpose computational circuitries. The latest computers guides towards distortion in performance of arithmetic functions like addition, subtraction, division & multiplication on the basis of carry propagation delay, higher complexity in circuits & higher consumption of power. While producing such adder with help of QSD number leads to faster addition & subtraction that has the ability of carry free addition & borrows free subtraction as carry propagation chain is removed & therefore it also minimizes propagation timing contrasting radix 2 systems. In QSD number system constituted over quaternary system, every digit can be presented through a number picked from the range of -3 to 3. It also helps in implementing operations over larger digits like 64, 128 having consistent delay & complexity.

This proposed QSD adder works in a better manner than other standard binary adders considering the factors like number of gates & higher bit addition through consistent time. The operational speed will also be increased by an optimal design of an adder block for performing addition & multiplication. QSD numbers require low space than the BSD for retaining numbers & further improvisation to QSD adder can also tolerate higher number of gates.

In 2009 Reena Rani[et.al] presented a paper for executing the functions like addition, subtraction & multiplication with propagation delay. A higher radix number system like QSD helps in attaining carry free operation. Some fast speed adders constituted over QSD umber system are proposed in this paper. Every figure is presented through a number from range of -3 to 3 in the QSD. Operations like carry free addition & various others can be implemented over large number of digits like 64 & 128 or more with consistent delay & lessen complexity. The design in such circuitries is generated through FPGA tools. Modelism software is used for simulation of design while Leonardo Spectrum is used for its synthesis.

This proposed QSD adder works in a better manner than standard binary adders while considering the factors like higher number of bits addition & number of gates in a consistent time period. The operational speed will be increased through an efficient design of adder block while performing operations like addition & multiplication. There is around ¼ less space acquired by QSD numbers than the BSD while QSD adder can support more number of gates with further enhancement.

In 2014 Shrikesh A. Dakhane[et.al] presented a paper for design the binary logic circuitries in an easy manner where there are less number of interlinks. These interlinks become a hefty work with increased number of inputs. The area of chip needs to be lessening with increase in complexity. The QSD numbers also helps to enhance the logical level. The logical circuitries based over such number systems provide less amount of delay while compared to binary circuitries. In this paper we are focused over designing an arithmetic system that produces better outcomes than standard binary circuitries. The addition performed through QSD also eliminates the condition of rippling of carry. This also eliminates the substantial carry handling circuitry that produces faster adders that are

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incorporated in other types of processors to generate faster outcomes. Such adders provide consistent delay which doesn't change as per number of inputs. Multipliers produced through such adder generate faster outcomes & possess lower complexity. The designing & evaluation of such circuitries is performed through Xilinx 13.2 software. Modelism software is used for simulation of outcomes.

In 2015 Jyoti R Hallikhed, [et.al] presented a paper for the speed execution of arithmetic operation in a binary system is restricted by generation & propagation of carry. The functions like carry free addition & borrow free subtraction are achieved through QSD number system. The QSD number system needs a specialized set of prime modules constituted over logical arithmetic functions. A higher radix number system like QSD is used for implementing the carry free addition process. It also supports the operations or higher numbers such as 64 & 128 without any carry propagation. Xilinx 13.2 ISE simulator is used for simulation & analysis of design. The verilog code is used for designing the proposed adder whilst Xilinx 13.2 ISE simulator is used for simulation & synthesis of the design. In this QSD addition & subtraction are entrenched & evaluated. The QSD ALU performs in a better manner in contrast to ordinary designs. The complexity in a QSD adder is directly proportional to number of bits that are having similar order like a standard BCD & other adders like ripple carry adder. Such QSD adders can act as main building component for other types of arithmetic & logical operations like multiplication & division. Through the QSD schema, some sounded arithmetic operations can be applied straight manner.

In 2014 M Naveen krishna [et.al] presented a paper for a higher radix number system such as QSD is applied for fast & more efficient arithmetic operation. In a binary system, speed of performing computation is restricted by generation & propagation of carry as there is hike in number of bits. There is an opportunity for performing carry free addition, multiplication & borrow free subtraction through implementation of QSD number system. a digit in a QSD's number system is presented by selecting a digit out of -3 to 3. This also enables to perform carry free addition & borrow free subtraction with consistent delay & lower complexity. Xilinx 12.2 is used for synthesis & simulation of design.

In the proposed layout of QSD, operations like addition, subtraction & multiplication for a single digit are designed through verilog HDL & its simulation is done by Xilinx 12.2. Such circuitries consume lower amount of power & energy and also performs in a better way. These designs also encounter fewer delays. Xilinx is used for simulation & synthesis of these designs. Simultaneously this layout is suitable for generating multiprocessors with high performance that is comprised of several processing units.

In 2015 Bhavya Sree Kotte,et.al[et.al] presented a paper for These days adders are mainly implemented in electronic components like computational devices & digital signal processors. Adders are able to implementing several algorithms such as IIR, FIR etc. In the present electronic components, digital systems have got an important place in routine. The arithmetic functions like addition, subtraction & multiplication has to still deal with some issues like restricted number of bits, complexity of circuit, time delay in propagation. The speed of operation by adders determines the speed of digital processors which have some constraints such as power, speed & area. The carry chain moulds the path of delay incorporated in adder. Binary signed digit numbers implemented in adders help to limit the propagation of carry with more complicated process of addition. Fewer such limitations applied over the system are related to speed of computation that also confines generation & propagation of carry particularly with a hike in number of bits. Hence, it leads to higher complexity & less density of storage. Carry free arithmetic operations are attained through high radix number system like QSD. In provided research, carry propagation chain is eliminated by QSD number system that also lessens the time of computation & also improving speed. QSD adder or Multiplier is the logic circuitries that are designed for implementing high speed arithmetic functions. A high radix based signed digit number system like QSD helps in high information storage density & lower complexity. A high speed & area effective adders & multipliers are applied through this technology. Carry free addition & similar operations are applied over larger digits like 64, 128 or more that can be applied through consistent delay & lower complexity. Xilinx 10.1 is used for simulation & synthesis of design.
In this proposed research QSD adder is used through NAND-NAND implementation for a single digit addition is formed. Performance of such adders is assessed through minimizing the complexity of circuit & computations. These designed adders that use QSD number presentation helps in faster addition or subtraction and has the ability of carry free addition & borrow free subtraction. The carry propagation chain is removed & therefore minimizes the time of propagation in contrast to radix 2 systems & further improvising speed of machine. These circuitries absorb fewer amounts of energy & power that also demonstrates higher level of performance in design analysis. The proposed QSD adder works in a better manner than standard binary adders in terms of gates & higher bit addition in consistent time.

In 2014 G.Manasa[et.al] presented a paper for the binary number system which restricts the speed of propagation & generation of carry. This QSD number system supports in attain borrow free subtraction & carry free addition simultaneously. A particular set of prime modulo based over logic for arithmetic functions is needed by the QSD number system. a high radix number system like QSD is implemented to perform carry free arithmetic function. Arithmetic functions like subtraction & addition can be implemented over bigger numbers such as 64 & 128 that can be calculated through without any propagation in carry through QSD number system. The Xilinx 13.2ISE simulator is used for simulation & analysis of design.

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Here in the paper, method for converting the binary to quaternary number system is demonstrated through some examples. Some different types of methods are used for adding up of quaternary numbers such as adding up of two QSD numbers, intermediate carry & sum are produced at initial level & the intermediate carry & sum are added to one another through full adders. The outcome generated from this addition will be free from carry. In this as performing conversion for binary to QSD, bits are splinted for LSB to MSB for each of the odd bit. This splitting must be halted over odd bit & splitting of MSB bits can't be done as it is considered as sign bit. This paper helps in implementing QSD addition for 65-bit number. This procedure for producing a quaternary number system & addition of QSD numbers through quaternary addition generates a delay of 72.616ns, 74 CLB's, 1294-input LUT's, 196 IO's & 65 XOR logic gates. This adder does not generate any carry that minimizes complicacy & interlinks. The function of addition performed through QSD number system is put in contrast to the addition performed through binary number system & further outcomes are evaluated.

In 2013 Sachin Dubey[et.al] presented a paper for the speed of computation which is restricted by generation & propagation of carry particularly with increment in quantity of bits. The processes like borrow free subtraction carry free addition & multiplication can be performed through implementation of QSD. Even though, some other logical components based over prime modules are needed for execution of arithmetic functions. An arithmetic function which is carry free is attained through higher radix number system like QSD. In QSD, every digit is presented in range of -3 to 3. This also helps in implementation of complex functions like carry free addition over large bit numbers like 64, 128 or more with persistent delay & low complicacy. The Modelism6.0, Microwind & Leonardo Spectrum are used for simulation & synthesis of design.
The dissipation of dynamic power in proposed layout comprising QSD adder built over NAND-NAND implementation for adding a single digit is obtained to be 36.255W over 5GHz frequency. Such circuitries consume low amount of power & energy & also presents a higher level of performance. The delay encountered by this proposed design is 2ns. Modelism 6.0 is used for simulation of design & Leonardo Spectrum LS2006a_59 is used for its synthesis while Microwind determines dissipation of power. Simultaneously, this design is suitable for producing a high performance multiprocessor that is comprised of several processing components.

In 2013 Aditya Sharma[et.al] presented a paper for Complicacies in circuit design, limiting the propagation delay, number of digits are non-changeable disadvantages that are faced in diversified DSP applications that require variegated functions.QSD (quaternary signed digit) number system works over method of eliminating carry propagation chains by simultaneously minimizing propagation delay to a huge proportion & therefore lead to faster arithmetic computations while comparing to binary number system. This paper demonstrates a VHDL layout of QSD based over adder/ subtractor & logical unit. The proposed VHDL layout will be applied over FPGA & detailed evaluation of performance will be attained. The design constituted over QSD provides better level of productivity over the other type of number systems for superior performance constituted over several different types of attributes like propagation delay, consumption of power, LUT utilization & number of digits. The formed QSD adder in the paper can be implemented for generation of QSD multiplier design. The further developments can constitute towards square-roots & division through representations of QSD. Moreover, this layout can be optimized through multivalve logic realization.

CONCLUSION

In VLSI we implement Reversible logic gates for improvising the performance for power of the circuitry. The delay, power & area get minimized after implementation of reversible logic gates in the QSD. We present the Review for the QSD adder , Subtraction and multiplications .

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