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Implementation of High Speed Vedic Multiplier

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***Abstract*:- Today processor needs high speed multipliers. Multipliers are the essential block to process functions in high speed arithmetic logic units, multiplier and accumulate units, digital signal processing units etc. To enhance speed many modifications over the standard modified booth algorithm, Wallace tree methods for multiplier design have been made and several new techniques are being worked upon. With the increasing constraints on delay, more and more emphasis is being laid on design of faster multiplications. Among these Vedic multipliers based on Vedic mathematics are presently focused due to these being one of the fastest and low power multiplier. Out of sixteen sutras in Vedic mathematics of multiplication "Urdhva Tiryagbhyam" has been selected as a most efficient one in terms of speed. A large number of high speed Vedic multipliers have been proposed with Urdhva Tiryagbhyam sutra. Few of them are presented in this paper giving an insight into their methodology, merits and demerits. Carry save adder, Ripple carry adder based Vedic Multipliers show considerable improvements in speed and area efficiency over the conventional ones.**

***Keywords**: Vedic mathematics, Urdhva Tiryagbhyam, carry save adder, ripple carry adder.*

I. INTRODUCTION

The Sanskrit word Veda is derived from the root Vid, meaning to know Without limit. The word Veda covers all Veda-sakhas known to humanity. Swami Bharati Krishna Tirtha (1884-1960)[1], former Jagadguru Sankaracharya of Puri culled a set of 16 Sutras (aphorisms) and 13 Sub-Sutras (corollaries) from the Atharva Veda. He developed methods and techniques for amplifying the principles contained in the aphorisms and their corollaries, and called it Vedic Mathematics. Vedic Mathematics offers a new and entirely different approach to the study of Mathematics based on pattern recognition. Vedic Mathematics designs used in many applications like ALU, MAC etc.

II. VEDIC MATHEMATICS SUTRAS

These 16 Sutras apply to and cover almost every branch of Mathematics[2]. They apply even to complex problems involving a large number of mathematical operations. Application of the Sutras improves the computational skills of the learners in a wide area of problems, ensuring both speed and accuracy, strictly based on rational and logical reasoning.

1. Anurupye Shunyamanyat-(If one is in ratio, the other is Zero)
2. Chalana-Kalanabyham–(Differences and Similarities)
3. Ekadhikina Purvena–(By one more than the previous one)
4. Ekanyunena Purvena–(By one less than the previous one)
5. Gunakasamuchyah– (The factors of the sum is equal to the sum of the factors)
6. Gunitasamuchyah– (The product of the sum is equal to the sum of the product)
7. Nikhilam Navatashcaramam Dashatah–(All from 9 and the last from 10)
8. Paraavartya Yojayet–(Transpose and adjust)
9. Puranapuranabyham–(By the completion or non completion).
10. Sankalana-vyavakalanabhyam– (By addition and by Subtraction)
11. Shesanyankena Charamena–(The remainders by the last Digit)
12. Shunyam Saamyasamuccaye– (When the sum is the same that sum is zero)
13. Sopaantyadvayamantyam– (The ultimate and twice the Penultimate)
14. Urdhva Tiryagbyham–(Vertically and crosswise.)
15. Vyashtisamanstih–(Part and Whole)
16. Yaavadunam–(Whatever the extent to fits deficiency).

A. Braun's Multiplier

Braun's multiplier[3] is an n × m bit parallel multiplier and generally known as carry save multiplier and is constructed with m × (n-1) address and m × n AND gates. The Braun's multiplier has a glitching problem which is due to the ripple carry adder in the last stage of the multiplier. Vedic multipliers show the considerable improvements in speed and area efficiency over the BRAUN MULTIPLIERS.

B. UT Sutra

The proposed Vedic multiplier depends on the "Urdhva Tiryagbhyam" sutra. These Sutras have been customarily utilized for the increase of two numbers in the decimal number framework. It is a general increase equation relevant to all instances of augmentation. It actually signifies "Vertically and Crosswise". It makes all the numeric calculations quicker and less demanding. The benefit of multiplier in view of this sutra over the others is that with the expansion in number of bits,

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range and postpone increment at a littler rate in contrast with others.

Urdhva – Tiryagbhyam is the general equation material to all instances of augmentation and furthermore in the division of a substantial number by another expansive number.

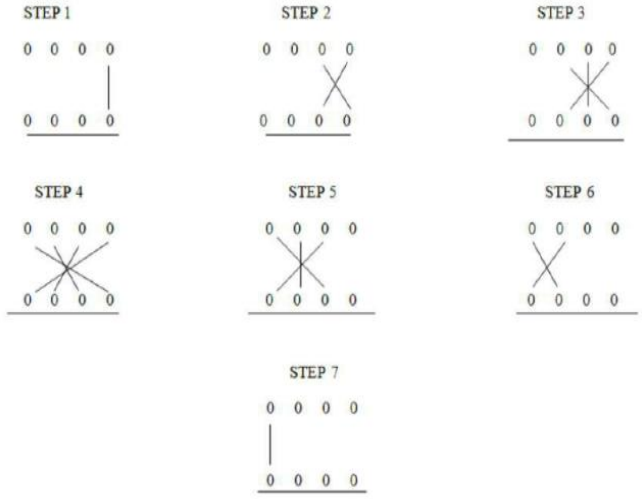

Fig 1. Block diagram of 4-Bit vedic multiplier

The multiplication of two decimal numbers 325 and 738. The numbers of steps in the process depend upon the number of the digits being used. Digits on the two ends of the lines are multiplied and resultant is added to the carry from previous step. When the number of crossing lines in a single step is greater than one then they all are added along with the previous carry. After this, only the least significant digit of the resulting number is taken as product digit and rest are considered as carry digits. Initial carry is taken as zero.[4]

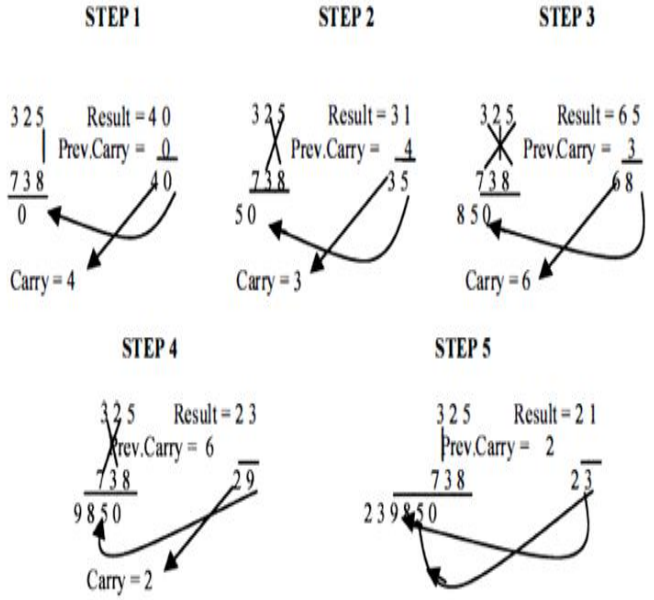

Fig 2. Decimal number multiplication using UT sutra

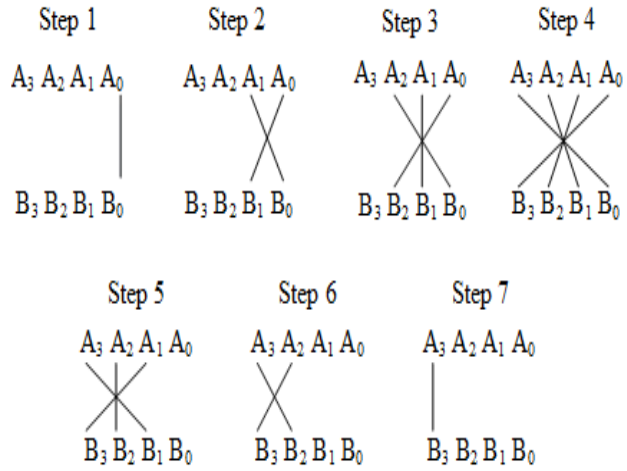

Fig.3. 4X4 vedic multiplication block diagram

Another strategy for the estimation of Urdhva Tiryakbhyam technique is appeared in Figure 2. In this method, the numbers to be duplicated given us a chance to state 5498 and 2314 are composed on the sequential sides of the square table. On apportioning the square into lines and segments, each line/segment has a place with one of the digit of the two numbers to be increased to such an extent that each digit of one number has a little square normal to the digit of other number. These little squares are further partitioned into two equivalent amounts of by transversely lines. Presently the every digit of one number is duplicated with each digit of second number and two digit items are set in their relating square. The digits on transversely line are included with past convey. Digits on dabbed noteworthy digit of the subsequent number are taken as item digit and rest are considered as convey digits. Introductory convey is thought to be zero here moreover. [2] The technique can be reached out for parallel numbers. A basic 1-digit twofold increase is portrayed by AND entryway operation. Utilizing this and UT technique 2X2 duplication for a1a0 and b1b0 is executed by 2 half adders and resultant bits are r2 (2 bits) r1r0 as shown in Fig. 4. The equations regarding this are given below. [5]

$$r0\ (1bit) = a0b0 \quad .....(1)$$
$$r1\ (1bit) = a0b1 + a1b0 \quad .....(2)$$
$$r2\ (2bit) = b1a1 + c1 \quad .....(3)$$
$$Product = r2\&r1\&r0 \quad .....(4)$$

Higher double augmentations can likewise be acquired with the assistance of lower increase units and the snake unit. The individual increase items are acquired by same partitioning technique, at last utilizing the 2X2 piece duplication strategy. For NXN increase unit, we require four N/2 bit multipliers, two N bit full adders, one half adder and N/2 bit full adder to include the aggregate and carry of half adder appeared. Fast of multiplier depends endless supply units utilized.

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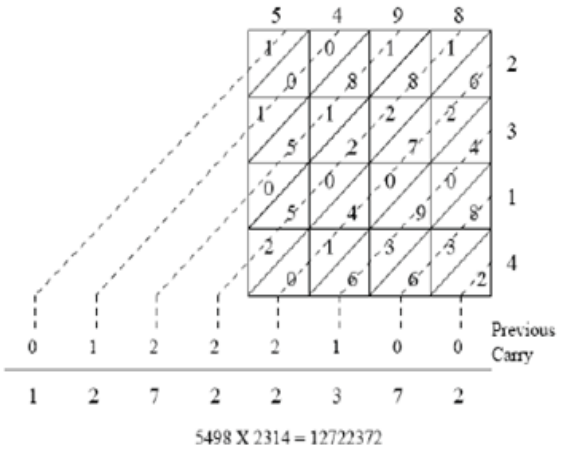

Fig 4. Alternate way to calculate UT sutra

III. 2X2 VEDIC MULTIPLIER

The 2X2 Vedic multiplier module is implemented using four input AND gates & two half-adders which is in its block diagram. It is found that the hardware architecture of 2x2 bit Vedic multiplier is same as the hardware architecture of 2x2 bit conventional Array Multiplier .Hence it is concluded that multiplication of 2 bit binary numbers by Vedic method does not made significant effect in improvement of the multiplier's efficiency.

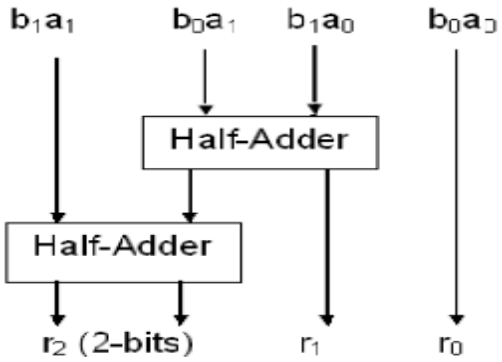

Fig 5. 2X2 Vedic multiplier

VI. 4x4 BIT VEDIC MULTIPLICATION USING RIPPLE CARRY ADDER

A RCA is a coherent circuit in which the complete of each full adder is given as the carry contribution to the following sequence full adder. It is purported in light of the fact that it gets undulated to the following stage. Adders are the primary squares to finish a multiplier outline. The Ripple Carry Adder (RCA) has the littlest area when compared with alternate adders. So it is restricted to applications where the range must be limited. The ripple carry adder is one of the least complex adders. The ripple carry adder is built by combining full adders (FA) obstructs in arrangement. One full adder is in charge of the expansion of two paired digits at any phase of the carry. A carry save circuit actualizes the expansion of two essential and one carry info and produces SUM and CARRY yield. In carry save adder, one piece full adder circuits are organized in course. Carry yield of the each full adder capacity is associated as carry contribution of one twofold piece higher full adders. Bit a0, b0 s to the slightest critical bits to be included and c0 speak to the carry input flag. In these adders, the primary goal is to create last carry and to obtain with better speed and lower control utilization[6].

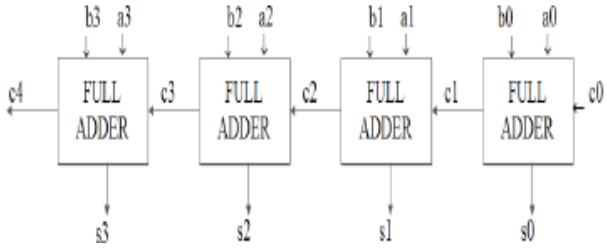

Fig 6. Ripple carry adder

In ripple carry adder, one bit full adder circuits are arranged in cascade. Carry output of the every full adder function is connected as carry input of one binary bit higher full adder . Bit a0, b0 represent the least significant bits to be added and c0 represent the carry input signal. In these adders, the main objective is to produce final carry and sum output with better speed and lower power consumption.

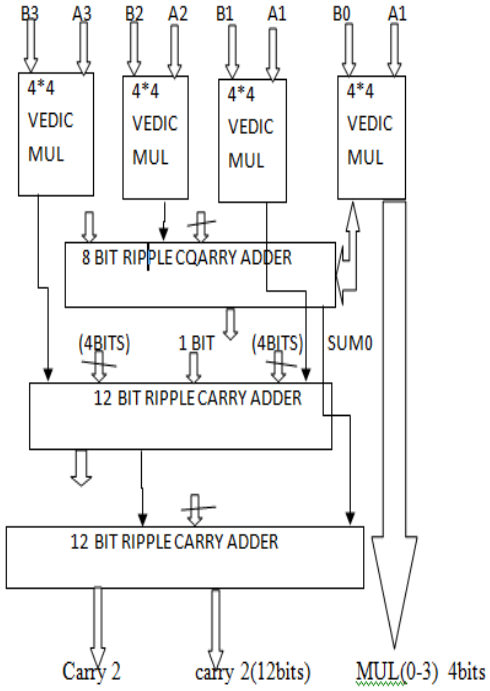

Fig7. Block diagram for 4X4 vedic multiplier using ripple carry adder

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V. MULTIPLICATION USING CARRY SAVE ADDER

A ripple carry adder is a kind of computerized adder, utilized as a part of PC miniaturized scale engineering to figure the aggregate of at least three n-bit numbers in twofold. It varies from other computerized adders in that it yields two quantities of an indistinguishable measurements from the information sources, one which is an arrangement of halfway entirety bits and another which is a succession of bits. The carry save adder is utilized to include at least three N bit operands by creating the yield of two N bit numbers in two sequences. One is having the N bit partial addition results comes about and another is having the arrangement of carry bits. At that point a ripple carry adder, for the most part Ripple carry adder is utilized to include these sets for the generation of final output. Not at all like regular adders like carry ripple, carry look ahead adder ,this adder does not has any carry propagation and has the propagation delay of a single full adder and delay does not change with the quantity of bits (n). Thusly for adequately huge estimation of n, it is quicker and littler in size [7]. For N-bit increase, it requires N-bit carry save adder and N+1 bit Ripple carry adder.

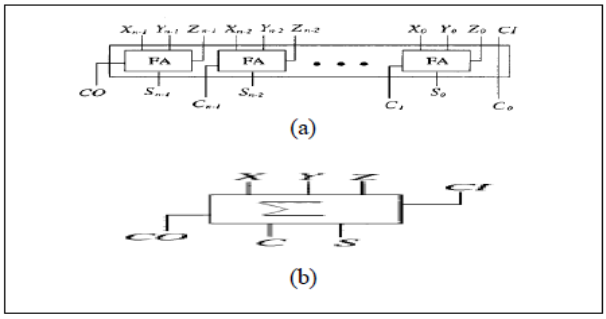

Fig8. Carry save adder

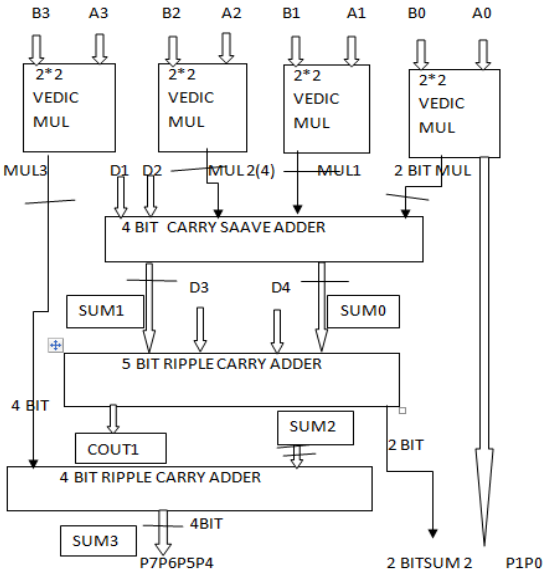

Fig 9. Block diagram for 4X4 vedic multiplier using carry save adder.

VI. CONCLUSION

Vedic Multiplier supposedly is productive in speed, control and zone in computerized plans as for different multipliers. Considering every one of the plans of it examined above, we can say that the Carry save adder based Vedic multiplier with Urdhva Tiryakbhyam sutra is viewed as a promising technique in terms of speed and area. The work can be further extend with the compressor based vedic multiplier and utilization of such multiplier in arithmetic logical unit, increase in accumulator unit designs and comparing at the outcomes with existing same designs.

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