Design and Analysis of 16bit Ripple Carry Adder and Carry Skip Adder Using Graphene Nano Ribbon Field Effect Transistor (GNRFET)

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Abstract: Moore's Law Cannot Be Sustained Since MOSFET's Cannot Be Scaled Below 10nm Due To Its Physical Properties .This Trade-Off Paves A Way For New Material Used In Fetes To Sustain Moore's Law, Various Other Technologies Include Fin-Shaped FET (Finfet), Carbon Nano-Tube FET (CNTFET), Reversible Logic, Reconfigurable Logic And Grapheme Nano-Ribbon FET (GNRFET), Among The Available Alternatives GNRFET's Has Proven To Be A Promising Potential Replacement In Terms Of Design Area, Lower Power Consumption And Faster Operation. Carbon Is An Interesting Element Because Even If Some Material Is Made Up Of Carbon Atoms, It Can Have Various Morphologies And Characteristics Depending On How Carbon Atoms Bind Together. Designing Of RCA And Cska Adders Using GNRFET.

I. INTRODUCTION

Integrated circuits have transformed the environment in which we live. The shrinking size of the transistors that result in smaller, faster and cheaper systems have enabled tremendous use of these chips. It is being evaluated that there are more than 15 billion silicon based chips currently in use. This number many reach a trillion in couple of years from now.

CMOS (Complementary metal-oxide semiconductor) is the semiconductor technology used to produce integrated circuit chips. In the year 1965, Gordon Moore (INTEL Co-founder) predicted that the number of transistors per square inch in an Integrated Circuit doubles every 18 months. This refers to the continued scaling both horizontally and vertically features the size of silicon based CMOS transistor. This effort has helped in producing inventory technologies of electronic devices.

Although the scaling of CMOS transistors has some predictions, there is a believe that it will finally reach the boundary at size of 22 nm as being forecasted in the International Technology and Roadmap for Semiconductors ITRS 2007. They frequently cite that CMOS transistors are approaching end.

Furthermore, the concern is not only about the inability of the devices itself to continue operate steadily but also the constraints from the economic and technology point of view. With the increasing level of device integration and the growth in complexity of microelectronic circuits, power dissipation, delay and area has come the primary design goal.

II. GRAPHENE

Graphene has been a purely theoretical form of carbon for decades. It wasn't until the year 2004 that Andre Geim and Konstantin Novoselov managed to produce Graphene flakes with a technique called mechanical exfoliation. Geim and Novoselov were awarded the Nobel Prize in Physics in 2010 for their discovery of Graphene. It is, therefore, easy to claim that 2010 has been the year of Graphene. In 2010, around 3000 Graphene related articles were published and roughly 400 patent applications filed.

According to a recent news article in Nature, South-Korea is planning to put 300 million US dollars in commercializing Graphene. New Graphene related discoveries are in nanotechnology news almost every other day. Keeping up with the pace of progress in the Grapheme research field is getting quite exhausting, and the pace of new discoveries shows only slight saturation.

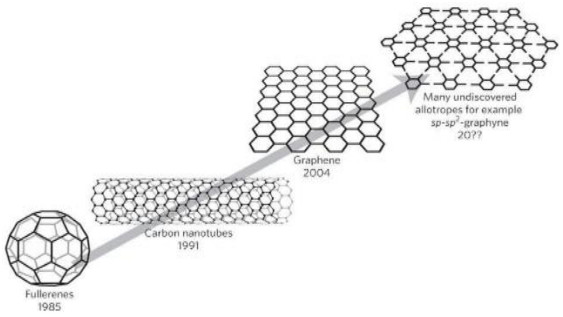

Fig 1: Some carbon allotrope

Grapheme is a single layer of sp2-bonded carbon atoms that are packed in a honeycomb lattice. The name Grapheme is sometimes misleadingly used with multiple layers, even though the variation in properties is quite significant when

going from one layer to several. It should be noted that multilayer Graphene can have up to ten layers, and still be called Grapheme.

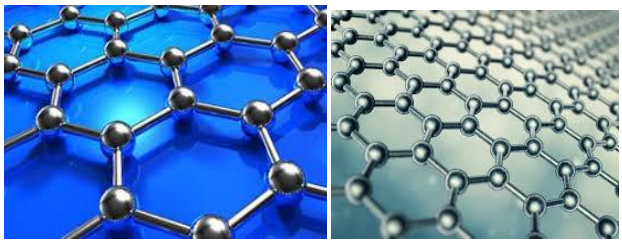

Fig 2: Hexagonal structure of Carbon

The atomic structure of Graphene gives rise to exceptional electrical, optical, mechanical and thermal properties. The most interesting electrical properties are high electron mobility and ballistic transport of charge carriers. However, these properties come with a twist; Graphene is zero-band gap semiconductor, or semimetal. The lack of band gap in intrinsic Graphene is perhaps, together with large scale manufacturing, the most difficult engineering issue. The zero-band gap means that Graphene cannot be switched from conductive state to non-conductive state.

The lack of a band gap is a problem, if Graphene is to be used in logic circuits in much the same way as silicon is used today as the material in complementary metal-oxide semiconductor logic circuits. Nonetheless, the zero band gap of large area Graphene is not an issue in all applications.

A. Electronic Band Structure

Graphene has a honeycomb (hexagonal) structure of sp2-bonded atoms. The electronic band structure of Graphene can be solved with tight binding approximation (TBA) or the similar linear-combination of atomic orbitals (LCAO), which is more commonly used in chemistry.

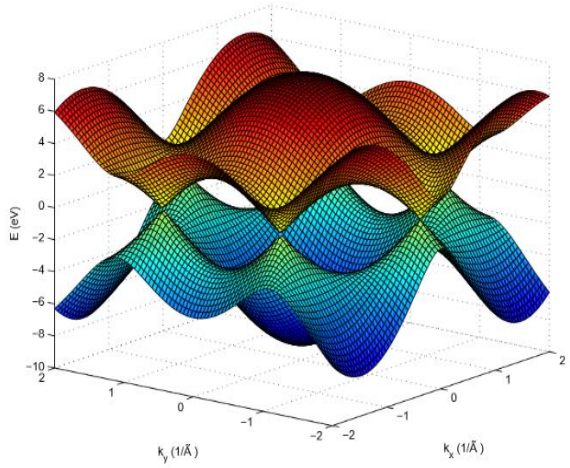

Fig 3: The electronic dispersion in Graphene

Graphene is a 2D material, but distinctions can be made between bi-layer Graphene and few-layer Graphene (FLG). Bilayer Graphene has two layers, but the electronic band structure is already quite different from single layer Graphene. Band gaps of some hundreds of mill electron volts have been achieved with bilayer Graphene by applying a perpendicular electric field to the belayed. The gap in Bernal stacked belayed Graphene arises from the forming of pseudo spins between the layers, thus making it possible to electrically induce a Band gap.

There are still many properties of Graphene that have not been thoroughly investigated. Even the existence of a band gap in large area Graphene is controversial. In addition to band gap opening in bilayer Graphene by applying an electric field, it is possible to create band gap by quantum confinement, i.e. by fabricating Graphene Nano ribbons. Edges may have significant influence on electrical properties, especially with GNRs.

B. Gnrfet

In one GNRFET, multiple ribbons are connected in parallel to increase drive strength and to form wide, conducting contacts. Two-dimensional Graphene is a semi-metal without a band-gap. A band-gap can be obtained by using a narrow Graphene Nano ribbon (GNR) which show distinct electronic properties and can be classified as either A-GNRs or Z-GNRs (armchair and zigzag Graphene Nano ribbons. A-GNRs are either semiconducting or metallic depending on their width, however, Z-GNRs are found to be metallic for all the widths.

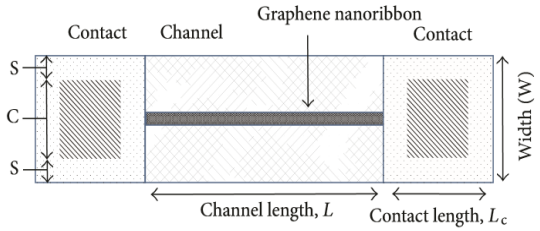

Fig 4: The structure of GNR with Nano Ribbon placed between source and drain

If Graphene is patterned into Nano ribbons, using planar technologies such as electron beam lithography and etching, a sizeable band gap opens. Son et. al. have shown that the band gap of an armchair GNR (AGNR) arises from both the quantum confinement and the edge effects. As a consequence, FETs with AGNR channels (AGNR-FETs), showing complete switch off and improved on-off current ratios, can be considered as building blocks for future digital circuits. Numerical modeling of GNR-FETs is usually based on a 'top-of-the barrier' approach under ballistic transport.

Graphene Nano Ribbons (GNRs) are one-dimensional (1D) nanostructures restricting carrier motion in only one direction, reducing scattering for enhanced mobility. The transistor current is quite high as electrons are injected from the source and transit to the drain terminal. A narrow width semiconducting GNR is utilized as a channel in a top-gated transistor. This pushes the limits of complementary metal-oxide semiconductor (CMOS) type of technology beyond its limits in a GNR.

The GNRFET device structure is very similar to MOSFET and is shown in figure 5 above. The 2D Graphene sheets are patterned to 1D ribbons to induce necessary band-gap. These 1D ribbons are called Graphene Nano Ribbon (GNR) and are semiconducting in nature owing to the fact that the band gap is inversely related to the ribbon width.

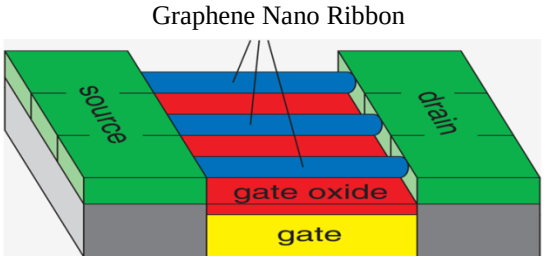

Figure 5 : view of a Graphene Nano Ribbon FET structure.

The GNR-FET operation under the condition that the electron gas in the channel is non-degenerate. Such a consideration is valid in the voltage range which is saliently wide in terms of practical applications. Thus, the back gate voltage is assumed to be not excessively high, so that the electron density is moderate, the electron gas in the channel is non-degenerate, and the electrons occupy only the lowest (n = 1) sub band in the conduction band Nano ribbons. Not with standing this, it is suggested that the channel sections adjacent to the source and drain contacts are highly conducting, so that these section are equipotential.

III. DESIGN METHODOLOGY

Adders are the most fundamental component in any of the digital computational units like ALU's, CPU's. As we know adders produce sum and carry as a result. If we want to compute addition of multiple bits which usually occurs in microcontrollers, microprocessors etc., we need to use multi-bit adders. So, to achieve this we go for 16-bit adders. Considering the parameters to enhance performance of adders various topologies are available.

Several adder topologies are

- Ripple Carry Adder (RCA)
- Carry Skip Adder (CSkA)
- Carry Look Ahead Adder (CLA)
- Carry Select Adder (CSlA)
- Carry Bypass Adder (CBA)

The advancement in IC technology is primarily attributed to the MOSFET scaling theory. As the transistor size reduced, power consumption also reduced. As the process technology reached nano-meter regime, silicon CMOS started developing Short Channel Effects which led to increased power dissipation. A trade-off arose between power-dissipation and area. Alternatives to CMOS were found to avoid the trade-off. Graphene based transistor proved to be a potential replacement to CMOS.

The Arithmetic and Logic Unit is the basic computing unit of all microprocessors or microcontrollers. The parallel adder forms the critical path in the ALU. The proposed work designs GNRFET based 16bit RCA and CSkA architectures. The architecture contains 28TFA The Adders are implemented first with 4 blocks of 1bit full adder to get the 16bit structure.

A. Ripple Carry Adders (RCA)

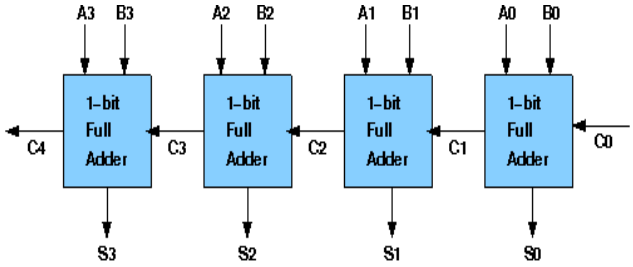

Figure 6: 4 bit Block diagram of RCA

The ripple carry adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage.

A number of full adders may be added to the ripple carry adder or ripple carry adders of different sizes may be cascaded in order to accommodate binary vector strings of larger sizes. For an n-bit parallel adder, it requires computational elements (FA). Figure 6 shows an example of a parallel adder: a 4-bit ripple-carry adder. It is composed of four full adders. The augends' bits of x are added to the addend bits of y respectfully of their binary position. Each bit addition creates a sum and a carry out. The carry out is then transmitted of the carry in of the next higher-order bit. The final result creates a sum of four bits plus a carry out (C4).

B. Carry Skip Adder (CSKA)

The carry skip adder provides a compromise between a ripple carry adder and a CLA adder. It consists of a speed up carry

chain called skip chain. This chain defines the distribution of ripple carry blocks, which compose the skip carry blocks, constituting skip adder. It consists of a special circuit which quickly detects if all bits to be added are different. CSA divides the words to be added into blocks.

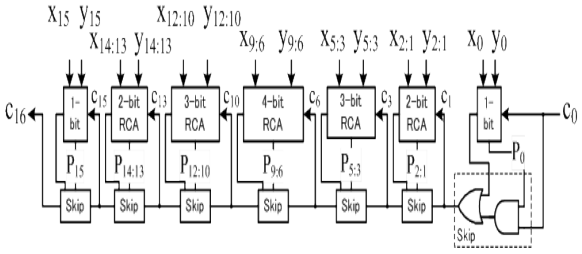

Fig 7: 16-bit Carry Skip Adder

The signal produced by this circuit will be called block propagation signal. If carry is propagated at all positions in block, the carry signal entering into the block can directly bypass it and so be transmitted through a multiplexer of the next block.

C. Hspice Tool

A circuit net list describes the basic functionality of an electronic circuit that you are designing. In HSPICE format, a net list consists of a series of elements that define the individual components of the overall circuit. You can use your HSPICE-format net list to help you verify, analyze, and debug your circuit design, before you turn that design into actual electronic circuitry.

H-Spice transient analysis computes the circuit solution as a function of time over a time range specified in the TRAN statement. Since transient analysis is dependent on time, it uses different analysis algorithms, control options with different convergence-related issues and different initialization parameters than DC analysis.

Here Predictive Technology Model (PTM) files and GNRFET libraries are used which contain all the defined parameters required for the simulation in H-Spice tool. The main focus is into the analysis of efficiency of various adder topologies based on the parameters such as Propagation Delay, Average Power Consumption and Power Dissipation.

IV. RESULT AND DISCUSSION

RCA and CSKA addition of 16 bits needs 33 inputs, like Input A with 16 bits, Input B with 6 bits followed by a Carry input of 1 bit. The resulting output is a 17 bits output with 16 bits Sum output and a 1 bit Carry output with logic high as 0.5 Volts and logic low as zero volts.

Parameter	RCA	CSkA
Power dissipation(nW)	0.3173	0.4842
Average power Consumption(nW)	0.65309	0.4977
Delay (ns)	100.08	0.0062

From the performance comparison based on various parameters GNRFET for 22 nm technology we conclude that, in case of Average Power Consumption, delay and power dissipation GNRFET did produce satisfactory results. By taking into account all the performance comparison parameters GNRFET based 16 bit Cask provides best performance as it needs less Average Power Consumption i.e., 49.77 nW, dissipates 48.42 new of power and has 0.00615 ns of propagation delay. Thus GNRFET can be the future of technology.

V. FUTURE WORK

Our work can be further continued by designing and optimizing remaining adder topologies i.e., Carry Save Adder (CSA), Carry Increment Adder (CIA) and Carry Look Ahead Adder (CLA) and their respective Arithmetic Units consisting of operations such as Addition, 2's Complement Addition, Increment and Decrement. This work can be further improved by clubbing these operations into a single Unit i.e., Combined Unit. The Arithmetic Unit can be combined with the Logic Unit to form ALU thereby also including the Memory Unit designed using SRAM Cells and DRAM Cells and their respective individual units and can be combined to form complete System Unit.

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