Reduce Power Consumption and Area of JK and SR Flip Flop by use Gate Diffusion Input

Ankit Fogat
M.Tech Scholar
Jaipur National University, Jagatpura Jaipur

Lokesh Lodha
Assistant Professor
Jaipur National University, Jagatpura Jaipur

Abstract:- This article is presenting a very fast, minimum power simultaneously timed NOR / NAND gate founded JK flip-flop by adjusted Gate Diffusion Input or GDI process in 130 nm technology. We introduce two kinds of flip-flop, NAND gate founded and NOR gate founded. We encounter the two kinds of problems; firstly, the significant power usage, and secondly, the great quantities of transistor using power. To additionally improve the implementation of the JK flip-flop, we utilize the Modified Gate Diffusion Input or M-GDI method. In this case, a reduced quantity of transistors will be employed, and the power usage will additionally be less. M-GDI is a method for reduced power conjunctional computerized circuit where logic gates are devised by utilizing reduced quantity of transistor. This method allows the lowering of the power usage, diffusion setback, and surface of the circuits having minimum intricacy of logic model.

Keywords-Modified Gate Diffusion Input (GDI) procedure, low power, high speed, power delay product (PDP), transistor count, area.

I. INTRODUCTION

A flip-flop or latch in electronics is a circuit that contains two balanced states and may be utilized to safeguard state data. A flip-flop is in fact a bistable multivibrator. The circuit may be manipulated to switch state through signals administered to at least one control contributor and will get one or two results. It is the essential storage unit in sequential logic. Latches or flip-flops are basic construction blocks of computerized electronics frameworks utilized in communications, computers, as well as numerous alternative kinds of frameworks.

Latches and flip-flops are utilized as information safeguarding units. A flip-flop safeguards a solitary bit (twofold digit) of information; of its two states, one denotes a "one" while the second denotes a "zero". This type of information storage may be employed to safeguard state, and this type of circuit is depicted as successive logic. When utilized in a finite-state device, the result and subsequent state rely not just on its actual contribution, but on its actual state as well (and thus, past contributions). It may further be utilized for the addition of pulses, and for coordinating changeably-clocked contribution signals to some standard clocking signal.

Flip-flops may be either basic (clear or opaque) or timed (synchronous or border-triggered). Even though the expression flip-flop is traditionally indicated universally to both basic and timed circuits, in contemporary application, it is typical to retain the expression flip-flop uniquely for speaking about timed circuits; the basic ones are typically termed latches.

A latch is stage-sensitive according to this wording, while a flip-flop is border-sensitive. In other words, when a latch is on, it turns clear, whereas the result of a flip-flop just changes on a solitary kind (positive direction or negative direction) of clock border.

The flip-flop is built in such a manner that the result Q is AND with CP and K. This setting is created so as to clear the flip-flop during a timed pulse just in case Q was 1 before. Likewise, Q is AND with CP and J, so as to clear the flip-flop during a timed pulse just in case Q was 1 before.
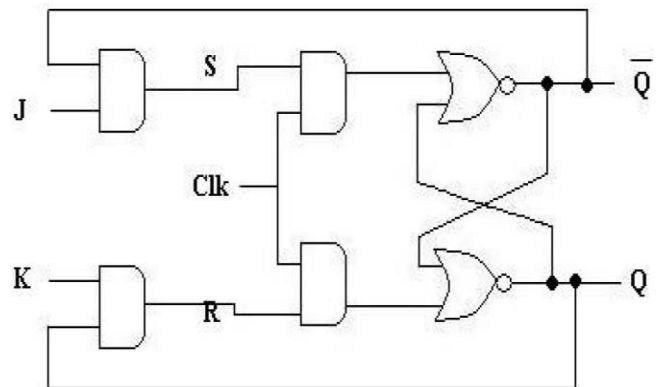

Fig 1 :- JK flip flop by AND , NOR gate

J	K	Function
0	0	Hold
0	1	0
1	0	1
1	1	Toggle

Table 1 :- Truth table of JK flip flop

A. JK Flip Flop By AND, NOR Gate In Tanner Tool

Like we may observe in Fig 2, we devise the JK flip-flop with the aid of AND, NOR gate. We provide the three contributions clk, J, K, and results Q and Q_ bar. Here, we utilize four AND gates as well as two NOR gates for devising the JK flip-flop.
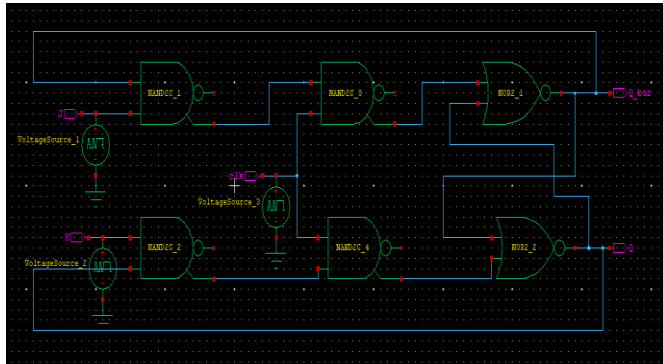
Fig 2:- JK flip flop by AND, NOR gate

B. JK Flip Flop By NAND Gate

Like we may observe in Fig 3, JK flip-flop is devised by utilizing eight NAND gate. We are using three contributions, J, K and Clk. In the model provided, two levels are displayed for the ultimate results that are Save Latch and Master Latch. Fig 4 is displaying the model of Tanner device for JK flip-flop using NAND gate.
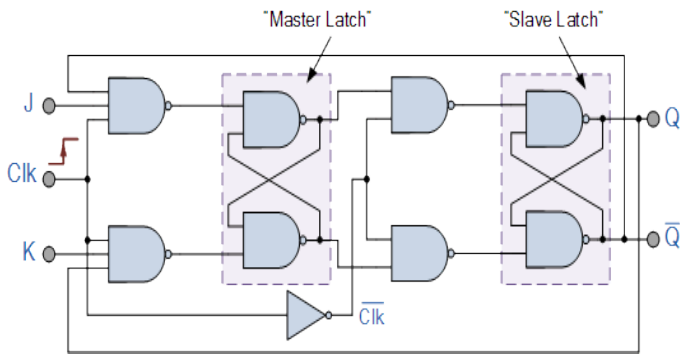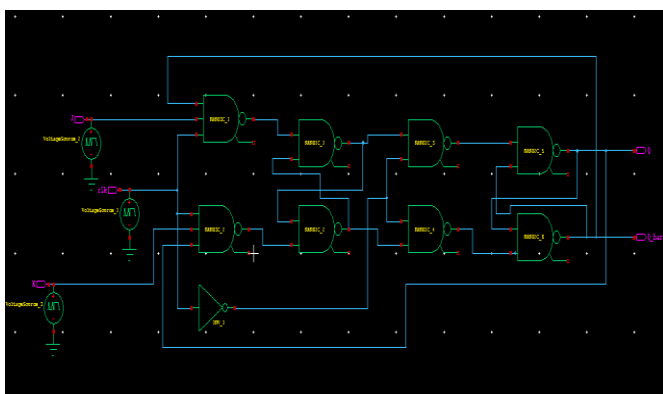

Fig 3:- JK Flip Flop by NAND Gate

Fig 4:- JK flip flop design by TANNER tool.

We utilize voltage origin of bits to provide the contributions J, K, and clk in Fig 4. We may provide 10 bits in a solitary moment here.

II. PROBLEM STATEMENT

The major problem in VLSI is power usage and surface size. In this dissertation, we are attempting to solve the two major issues, which are:

A .Power Consumption

Power usage in VLSI is the major problem which arises in the CMOS model. Like we may observe, figures 2 and 4 are utilizing many logic gates, which are in turn amplifying the power usage. We need to lower the power usage of the JK flip-flop by implementing the recommended process. The power usage is 8.680838e-003 watts in Fig 2 and 5.736606e-003 watts in Fig 4. We need to lower the power usage from the current power usage outcomes.

B. Number Of Transistor

Like we may observe from figures 2 and 4, many transistors and gates are employed. The surface size increase with the quantity of transistors, and because of this the power usage is augmented as well. In our dissertation, we are attempting to solve the quantity of transistors issue. In Fig 2, the entire quantity of transistors used is 32 for the JK flip-flop model which we devised with AND, NOR gate. The entire quantity of transistors is 54 for the JK flip-flop model where we used NAND gate. Therefore, in this article, our first issue is lower the quantity of transistors for the two models.

III. PROPOSED METHODOLOGY

To lower the power usage and quantity of transistors, we are using the M-GDI process. Morgenshtein *et al.* (2002) researched a very rapid and multipurpose logic model for minimum power electronics devising, called Gate Diffusion Input or GDI process [7] having diminished surface size and power requirements, and efficient in performing a wide range of logic applications. Fig 5 illustrates a fundamental M-GDI logic cell, utilized for performing a range of logic applications and circuits at minimum power and very rapid model where G, P, and N are three contributions and the result is obtained from the D terminal. Table 1 denotes the logic applications which may be performed with the aid of this fundamental M-GDI cell [1,2]. However, this essential Modified GDI logic model has some realistic constraints such as swing deterioration, manufacturing intricacy in regular CMOS methodology and mass links. Such constraints may be surmounted by M-GDI logic model [4, 5].
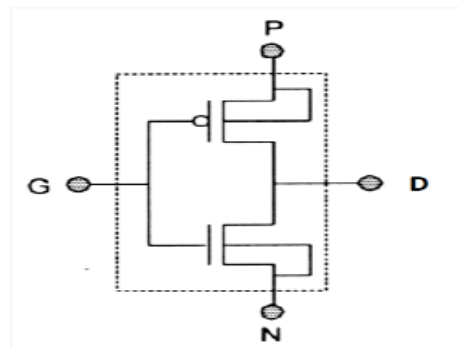

Fig 5:- Basic M-GDI Cell

Further to this, physical performance of core M-GDI cell is not feasible in customary p-well progression. Moreover, the implementation through twin well / triple well scheme will require the basic M-GDI cell to have a better surface size because of the discrete wells for each transistor. This essential assumption is not precise as the origin, together with drain module, depends on the values of logic given at the contribution. So, in the principal M-GDI cell, the impact of the substrate was eliminated in situations where the body was connected to the origin, though an amelioration in minimum voltage occurred on linking the bulk to the drain. Additionally, as the fundamental M-GDI cell forces twin-well CMOS or SO1 process to understand, realization of a basic M-GDI chip will be an important one. The Modified Gate Diffusion Input cell as shown in Fig 4.1 surmounts the disadvantages incurred by the primary M-GDI cell and is tremendously similar to the fundamental M-GDI cell, apart from the issue that the PMOS and NMOS transistors' bulks in an altered GDI cell are constantly attached to V DD and GND correspondingly. This eases natural implementation of the M-GDI gates in common CMOS processes. The result of the body impact on circuit performance is tremendously similar to that of rudimentary M-GDI cell.

A. NOT gate using Modified GDI technique

Fig. 6 shows the NOT gate made by utilizing M-GDI method and is nearly alike to that of a regular CMOS inverter.
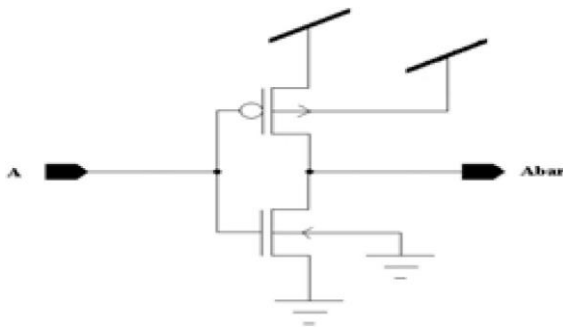

Figure 6: NOT gate using modified GDI technique

Fig 7 displays the contribution and the resultant waveform of a NOT gate using M-GDI methodology in 130nm technology.
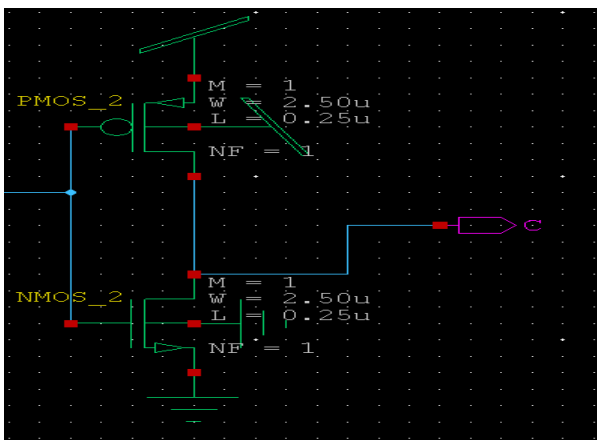

Fig 7:- NOT gate design in Tanner By M-GDI Technique

Figure 8: Input and output waveform of a NOT gate using modified GDI

B. NOR gate using Modified GDI technique

Fig 9 shows the NOR gate created by utilizing M-GDI method. It consists of two M-GDI cells, in which the port 'P' of the initial cell is taken as the contribution 'B' and the port 'G' of the initial cell is taken as a contribution 'A'. Port 'N' of the initial cell is equipped with Vdd and the result 'nl' is linked to port 'G' of the other cell which functions as an essential inverter, completing the result acquired from the initial cell.
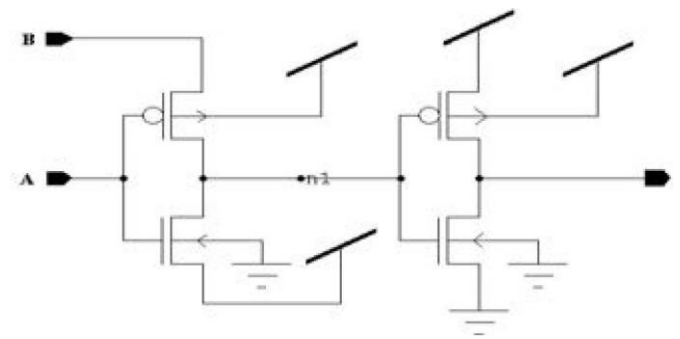

Figure 9: NOR gate using modified GDI technique

Fig. 10 displays the contribution and result waveforms of a NOR gate devised by utilizing M-GDI method in 130nm technology.
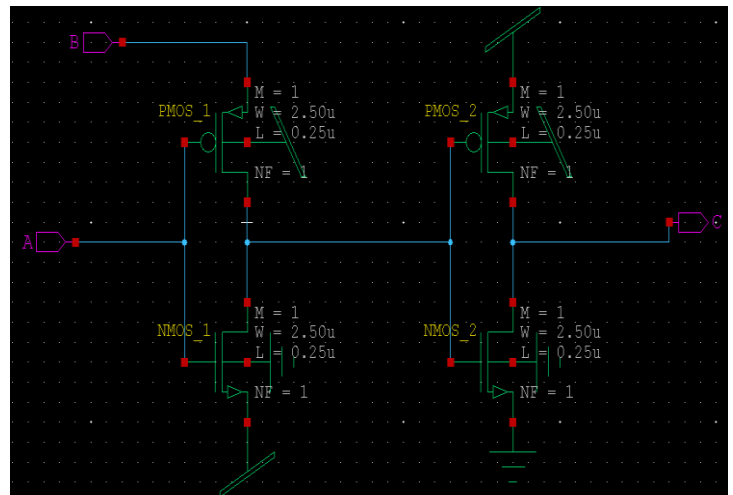

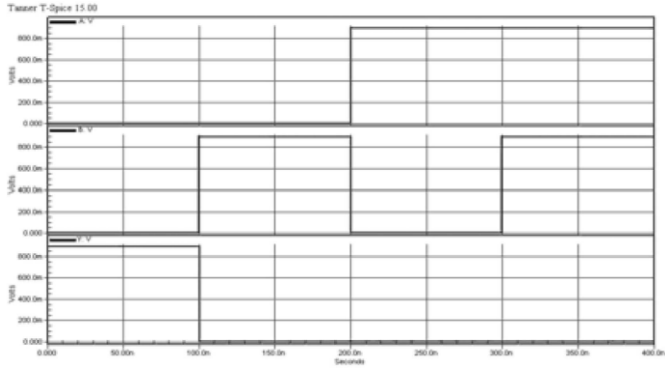Fig 10:- NOR gate Design by Tanner M-GDI Technique

Figure 11:- : Input and output waveform of a NOR gate using modified GDI technique

C. AND gate using Modified GDI technique

Fig 12 illustrates an AND gate designed utilizing M-GDI method, in which port 'P' is linked to GND and port 'N' is given a contribution 'B'. Port '0' is provided a contribution 'A'.
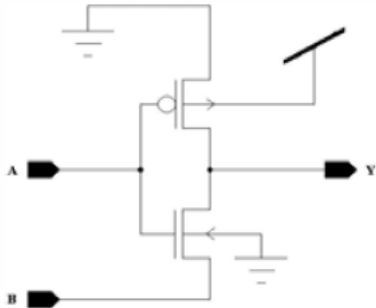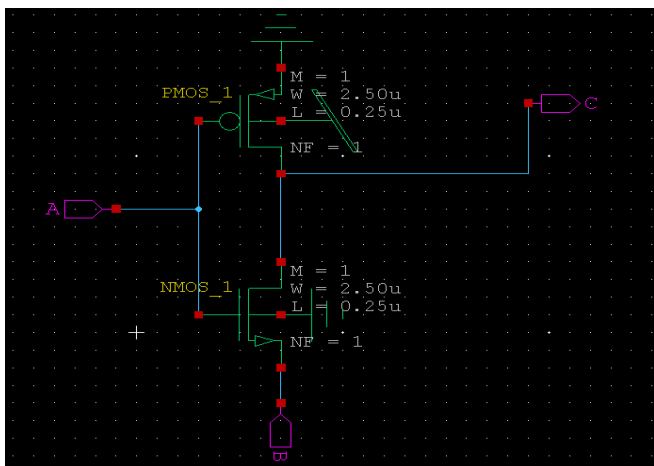

Figure 12: AND gate using Modified GDI technique

Fig 13 displays the contribution and result waveforms of an AND gate, created utilizing M-GDI method in 130nm technology.

Figure 13: AND gate using Modified GDI technique by Tanner
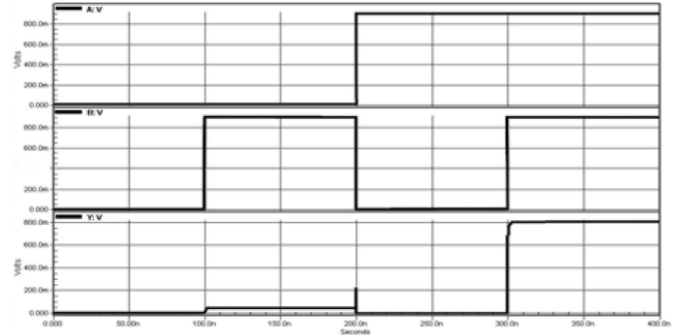
Figure 14: Input and output waveform of an AND gate using modified GDI

In Fig 15, we present the JK flip-flop by utilizing AND, NOR gate. Like we may observe in the figure, four AND gates, two NOR gates are employed in devising the JK flip-flop. To provide the contribution to the J, K, and CLK, we utilize voltage supply.
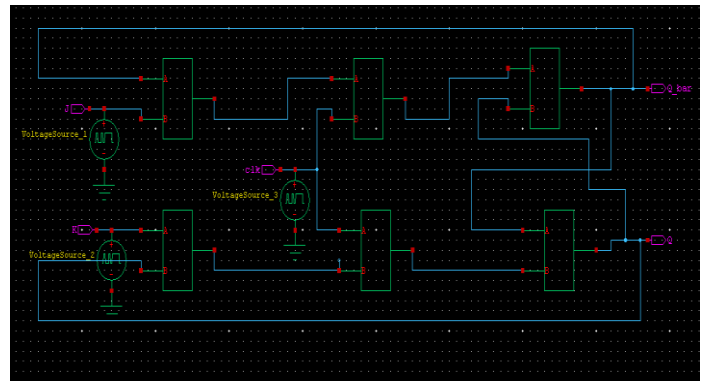

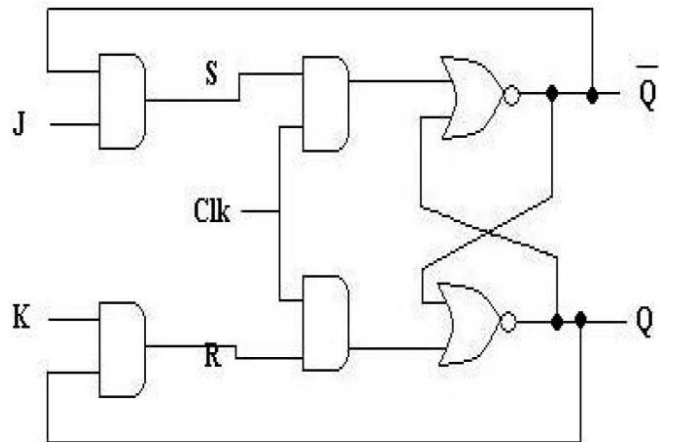Fig 15:- JK flip flop by use AND, NOR Gate

Fig 16 :- JK flip flop by AND , NOR gate

Fig 16 shows the JK flip-flop by utilizing NAND gate. M-GDI method is used to devise the NAND gate in this module.

IV.   RESULTS

A. JK Flip Flop By And, Nor Gate

Like we may observe in Fig 20, JK flip-flop is devised by utilizing AND, NOR gate. To provide the contributions, voltage supplies are linked to the J, K, and clk contribution. Q and Q_ bar are the results of the JK flip-flop.
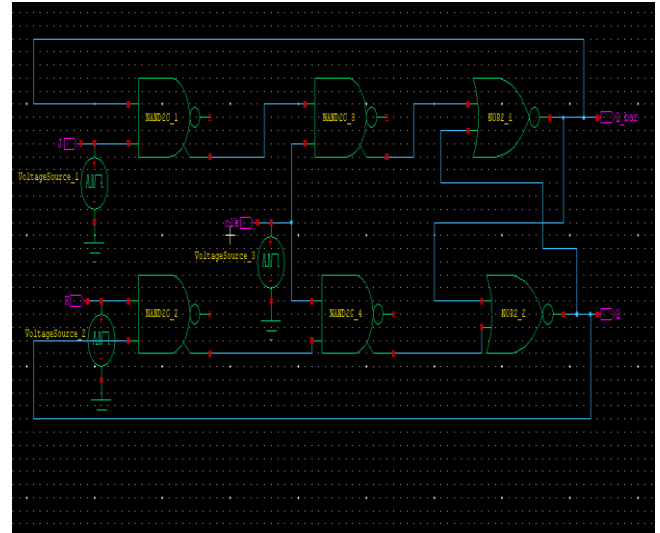

Fig 17:- NAND gate design by M-GDI Technique

In Fig 17, we devise the NAND gate by applying M-GDI methodology. With the aid of NAND gate with M-GDI method, we devise the JK flip-flop as depicted in Fig 18.

Fig 18 :- JK flip flop

D. SR Flip Flop

Figure 19 is showing the proposed design of SR Flip Flop. SR Flip Flop is the combination of NAND gate . So in the proposed design , use M-GDI based NAND gate . M-GDI is able to reduce the Power Consumption and Transistors of the circuit.

Fig 19. Proposed SR Flip Flop Design by use M-GDI
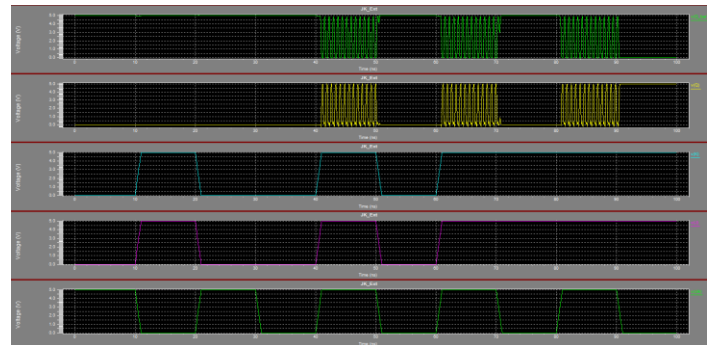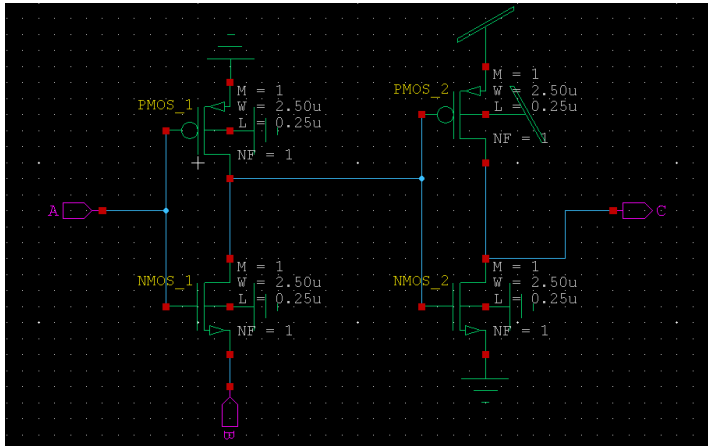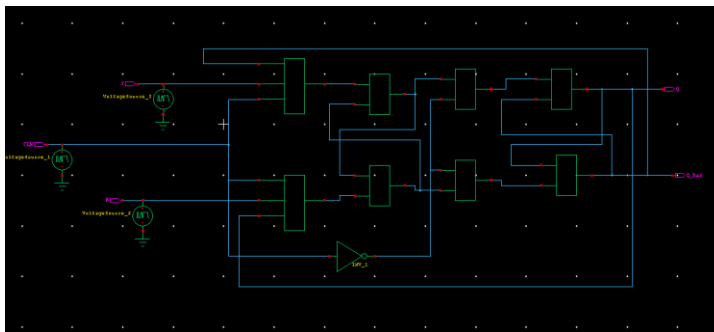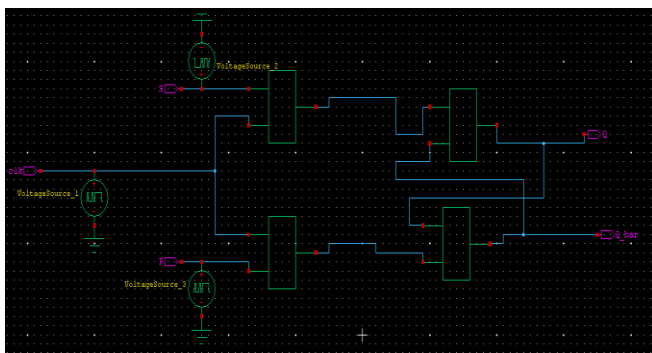

Fig 20:- JK flip flop by use AND, NOR gate

Fig 21:- Output Waveform of JK flip flop by AND, NOR gate

Like we may observe in Fig 21, clk, J, and K are the contributions, while Q and Q_bar are the results of the JK flip-flop. The power usage for the JK flip-flop with AND, NOR gate is $1.356195*10^{002}$ watts and the quantity of transistors is 32.

B. JK Flip Flop By NAND Gate

Like we may observe from Fig 22, JK flip-flop is devised by utilizing NAND gate. To provide the contributions, voltage supplies are linked to the J, K, and clk contribution. Q and Q_bar are the results of the JK flip-flop.
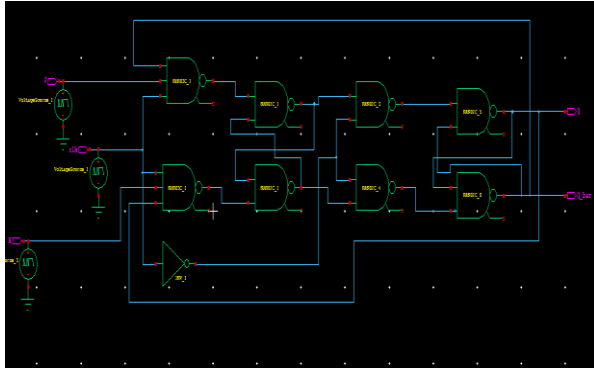
Fig 22:- JK flip flop by use NAND gate.

Like we may observe in Fig 22, clk, J, and K are the contributions and Q, Q_bar are the results of the JK flip-flop. With NAND gate, the power usage for the JK flip-flop is 5.736606e-003 watts and the quantity of transistors is 54.
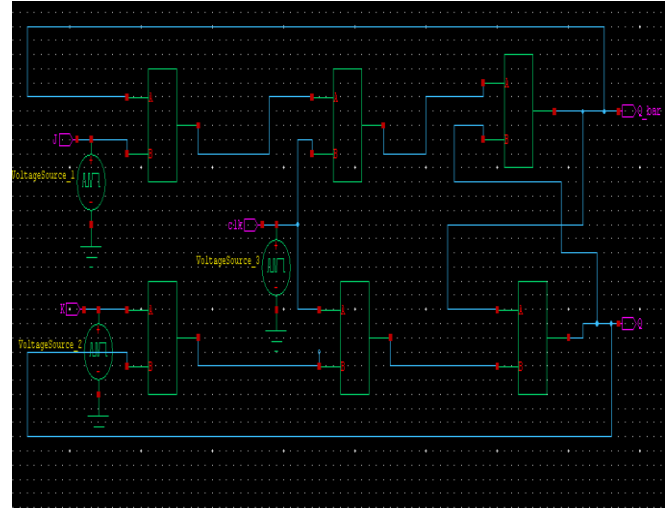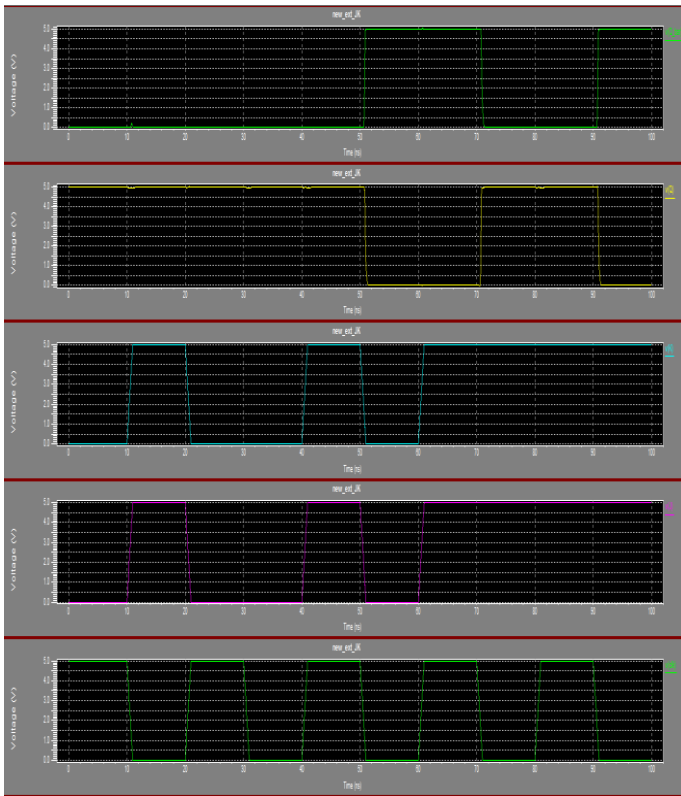

Fig 23:- Output Waveform of JK flip flop by NAND gate

C. Proposed JK Flip Flop By AND, NOR Gate With M-GDI Technique

Like we may observe in Fig 24, JK flip-flop is devised by using AND, NOR gate. To provide the contributions, voltage supplies are linked to the J, K and clk contributions. Q and Q_bar are the results of the JK flio-flop. To devise the AND, NOR gate, the M-GDI method is applied.

Fig 24:- JK flip flop by use AND, NOR gate with M-GDI technique

Like we may observe in Fig 25, clk, J, and K are the contributions while Q and Q_bar are the results of the JK flip-flop. The power usage for the JK flip-flop using AND, NOR gate through M-GDI method is $1.091241*10^{002}$ watts and the quantity of transistors is 16.
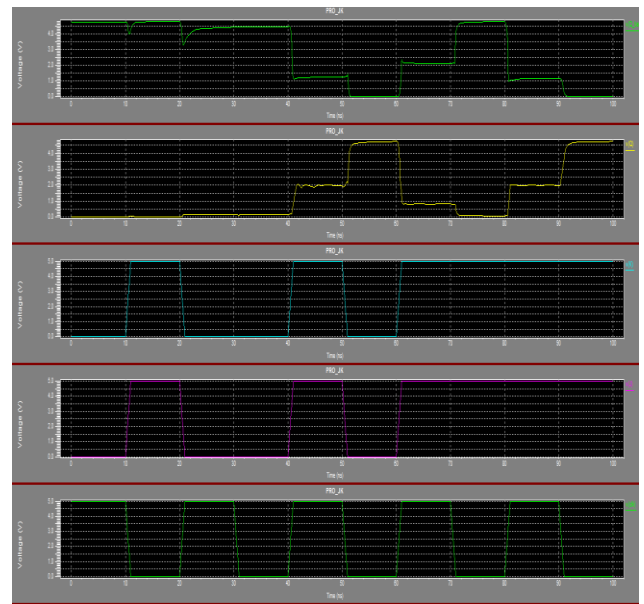

Fig 25:- Output Waveform of JK flip flop by AND, NOR gate with M-GDI technique

D. Proposed JK Flip Flop By NAND Gate With M-GDI Technique

Like we may observe in Fig 26, JK flip-flop is devised by utilizing NAND gate. To provide the contributions, voltage supplies are linked to the J, K and clk contribution. Q and Q_bar are the results of the JK flip-flop. To devise the NAND gate, we apply the M-GDI method.
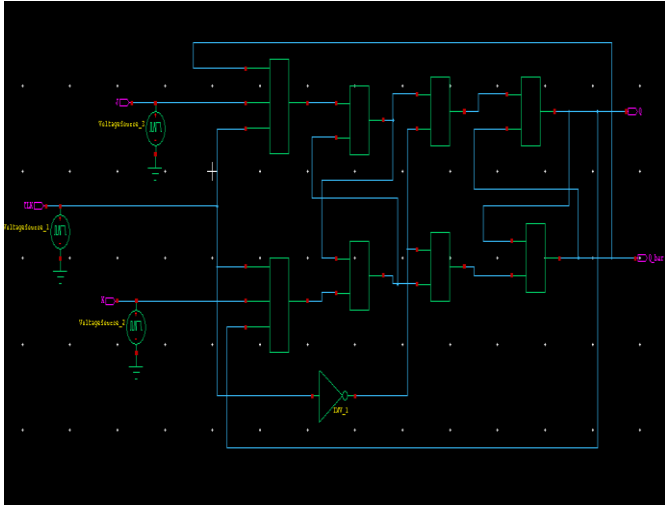
Fig 26:- JK flip flop by use NAND gate with M-GDI technique

Like we may observe in Fig 26, clk, J, and K are the contributions while Q and Q_bar are the results of the JK flip-flop. The power usage for the JK flip-flop using NAND gate through M-GDI methodology is 2.603563e-003 watts and the quantity of transistors is 42.
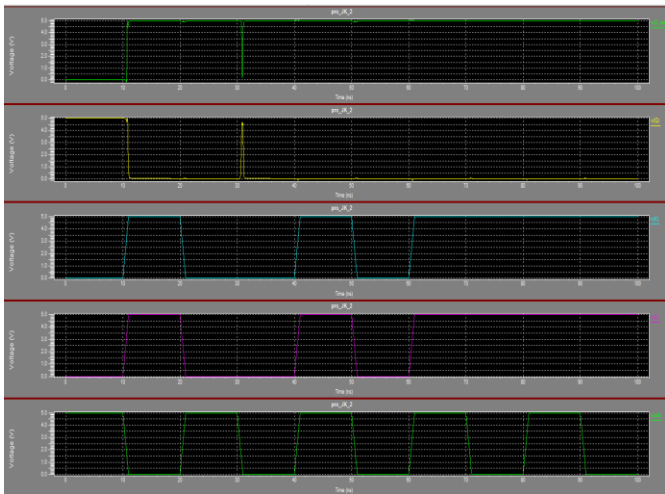

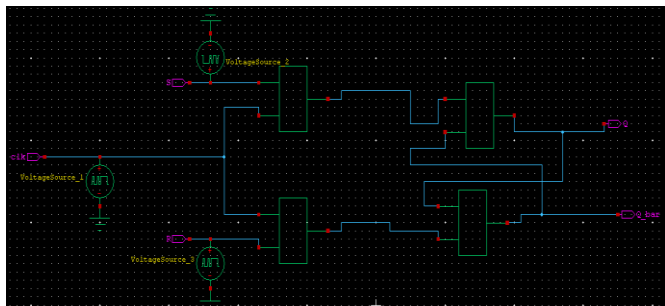Fig 27:- Output Waveform of JK flip flop by NAND gate with M-GDI technique

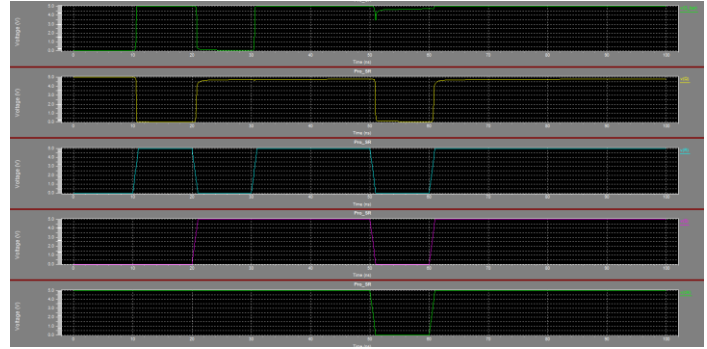Fig 28. Proposed SR Flip Flop by use M-GDI

Fig 29. Output Waveform for Proposed SR Flip Flop

Figure 28 is showing the proposed SR Flip Flop by use M-GDI based NAND Gate. For design the SR Flip Flop use 4 NAND Gate. Figure 29 is showing the output waveform of the SR Flip Flop.

5.5 COMPARISON TABLE

	Power	Transistor
J-K Flip flop (JK-Ext)	1.356195*10^002 watts	32
Proposed JK Flip Flop(pro_jk)	1.091241*10^002 watts	16
S-R flip flop (SR_FF)	6.86710*10^003 watts	24
S-R proposed (Pro_sr)	3.28069*10^003 watts	16

Table 1:- Comparison Table

V.   CONCLUSION AND FUTURE SCOPE

In this dissertation, we devise the JK flip-flop by utilizing two kinds of model. In the initial model, we utilize AND, NOR gate and in the other model, we utilize NAND gate founded plan. The major problem in the VLSI is high power usage and surface size. Therefore, in this dissertation, we lower the power usage and quantity of transistors for the JK flip-flop for the two models. We recommended M-GDI method through which the quantity of transistors and surface size is diminished. Without MGDI technique the power consumption of JK Flip flop is 1.356195*10^002 watts and 32 number of transistor. NAND Gate Based SR Flip flop Power Consumption is 6.86710*10^003 watts while number of transistor are 24.

After apply MGDI the power consumption for the AND, NOR gate based JK flip flop is 1.091241*10^002 watts. MGDI based SR Flip flop Power Consumption is 3.280698*10^003 watts while number of transistors are using 16.

Prospectively, we may administer the recommended altered JK flip-flop in Johnson counter. The power usage and quantity of transistors may be diminished by using the altered JK flip-flop in the Johnson counter.

REFERENCES

[1]. Reto Zimmermann and Wolfgang Fichtner. "Low-Power Logic Styles: CMOS versus Pass Transistor Logic_" IEEE Journal of solid-state circuits, 32(7), pp.1079-1090.

[2]. Chinnarao , Francis and Apparao, 2012. Design of a low power flip-flop using CMOS deep submicron technology, International Journal of Electronics Signals and Systems (IJESS) ISSN: 2231- 5969, 2(1), pp. 99-103.

[3]. Soheil Ziabakhsh and Meysam Zoghi, 2009. Design of a Low-Power High-Speed T-Flip-Flop Using the Gate-Diffusion Input Technique, 17th Telecommunications forum TELFOR 2009, Serbia, Belgrade, November 24-26, pp.1470- 1473.

[4]. Geetha Rani, Praveen Kumar, Stephen Charles, Chandrasekhar Reddy, S.Md.Imran Ali, 2012.

[5]. Design of Near- Threshold CMOS Logic Gates, International Journal of VLSI design & Communication Systems, 3(2), pp. 193-201.

[6]. Subodh Wairya, Rajendra Kumar Nagaria and Sudarshan Tiwari, 2012. Comparative Performance Analysis of XOR-XNOR Function Based High-Speed CMOS Full Adder Circuits for Low Voltage VLSI Design" International Journal of VLSI design and Communication Systems, 3(2), pp. 221-242.

[7]. Kharate G. K., Digital Electronics, Oxford university press, 2010, 1sh Edition, ISBN 13:978-0-19-806183-0.

[8]. Morris Mano M. 1979. Digital Logic and Computer Design" Prentice-Hall of India, Easter Economy Edition, 1th Edition, ISBN 81-203-0417-9

[9]. Priyanka Sharma1 , Himanshu Joshi," High Speed, Low Power NAND Gate-based JK Flip-Flop using Modified GDI Technique in 130 nm Technology", International Journal of Engineering Science and Computing, June 2016.