

Design, Modelling and Implementation of Interleaved Boost DC-DC Converter

Divya M₁

PG Student [Power Electronics], Dept. of Electrical Engg, UVCE, Bengaluru, Karnataka, India

Guruswamy K P₂

Assistant professor, Dept. of Electrical Engg, UVCE, Bengaluru, Karnataka, India

Abstract:- Multiphase converter topologies for use in high performance and low voltage applications have received increasing interest in recent years. The project report compares a 2-phase interleaved boost converter with the conventional Boost converter. In this research, a 2-phase structure with interleaved control is studied which is said to reduce the input current ripples, the output voltage ripples, and the size of passive components with high efficiency compared with the conventional topology. Furthermore, a state space averaging technique is performed there by steady state and small signal models are derived for these dc/dc converters. A closed loop control is achieved by designing a digital PID controller to achieve the proper regulator for the converters. The design and investigation of PID controller is made for the parameters and designed values of the DC-DC converter using MATLAB Simulink. The hardware implementation of the conventional boost converter and 2-phase interleaved boost converter is performed using Arduino Microcontroller and performance of the two converters is studied. The Simulation and experimental results thus obtained concludes that 2-phase IBC satisfies the objectives of reducing the size of passive elements and reducing the input current ripple.

Keywords: Interleaved boost DC-DC converter (two phase IBC), continuous conduction mode (CCM), Transfer function (TF), Proportional-Integral-Derivative (PID) Pulse Width Modulation (PWM), Small Signal Model (SSM), ARDUINO micro controller, SISO tool.

I. INTRODUCTION

All the new apparatus working on low voltage and high current needs Power converters that can supply regulated voltages from a constant power source. The parameters of the apparatus cannot be achieved only with the existing converters and hence there is a need for newer topologies. The apparatus require a constant output voltage even during varying loads and varying sources, also for the better switching of gates, closed loop control is required which can be implemented using different control techniques. Interleaving is an approach to minimize the input current ripple and also its affects the efficiency on the converter The optimal selection of the number of phases and the switching frequency results in a better efficient converter operation. The result can be gauged by several parameters such as cost, weight, volume, conduction losses of the switches, volume index of the inductor, input current and voltage ripples. The major benefit of interleaving topology is achievement of

higher power quality needs, reduced input current and reduced cost the power inductor with increase in phase number[1][2].Soft-switching type of converter is used for reducing the switching losses and hence improving the efficiency. But it also holds a disadvantage which is rise of voltage across the switch during the resonance It is also seen that increase in efficiency using this type of converter is a mere 1.5% than the conventional interleaved boost converter [3].The use of coupled inductors to increase the ripple current of each cell. A positive coupling coefficient will only yield the desired result based on output characteristic plot of each cell [4][5].

A control method in pulse width-modulated (PWM) dc–dc converters because of its quick reaction, precision, and overburden protection is peak current mode control (PCM).Utilizing control hypothesis, a transfer function from the error voltage to the duty cycle that captures the behaviour can be derived. This transfer function has a pole that can be in either the left-half plane or right-half plane, which catches the sample and-hold impact precisely, empowering the portrayal of the current-loop gain and closed-current loop for PWM dc–dc converters with PCM [6]. It is very unstable when duty ratio exceeds 0.5 in the peak current mode- control and there is presence of Sub harmonic oscillations in this type of control. Voltage Loop of Boost PWM DC–DC Converters with Peak Current-Mode Control is used to arrive at the gain of the voltage loop , transfer function consisting of reference voltage to output voltage and closed loop output impedance using small-signal averaging technique. The line regulation, load regulation and control voltage level can be found. It concludes that the instability of the Peak current mode control method is eliminated using this proposed method[7].There are various troubles associated with the SM controllers when compared to PWM controllers, SM controllers is not an IC for power electronics application, high switching frequency and the consequent power losses being the significant ones. It concludes on feasible solution of using a PWM based sliding mode controller gives a more reliable transient response for a more wider working range[8][12].

In this paper, a comparative analysis of conventional boost converter and Interleaved boost converter is made to study the performance so as to replace the conventional boost converter with the IBC. Interleaving also called multi-phasing, is a technique that is useful for reducing the size of filter components [9].The input to these converters is an unregulated and low DC voltage, which is obtained by photovoltaic (PV) array output or low voltage battery.

Interleaved boost converter is used to convert the unregulated DC input into a controlled DC output at a desired voltage level. IBC topologies have received increasing attention in recent years for high power applications. The benefits of interleaving include high power capability, modularity and improved reliability. Therefore an IBC has been proposed as a suitable interface. IBC is a complex converter due to a number of parallel connections. However it has the following advantages as compared to conventional boost converter.

1. Low input current ripple
2. Low output voltage ripple
3. High efficiency
4. Reduces the size of filter components

As the output current is divided by the number of phases, the current stress in each switch is reduced. Each switch is switched at the same frequency but at a phase difference of $\frac{2\pi}{N}$ where N is the phase number.

In this paper the Two phase Interleaved buck Converter was modelled considering all the parasitic elements of the converter using state space averaging technique [10, 11] and analysed using small signal analysis. Section II, III presents working principle of two phase IBC with duty cycle D ($0 < D < 0.5$) ($0.5 < D < 1$). Section IV, describes the steady state

characteristics and design of two phase IBC converter. Section V presents modeling and analysis two phase IBC. Section VI gives the simulation results. Section VII gives the Experimental results Finally section VIII concludes the paper.

The model is simulated in MATLAB/ Simulation for closed loop with analog PID controller. This paper presents the design of two phase IBC and also modelling and analysis of same.

II. 2-PHASE INTERLEAVED BOOST DC-DC CONVERTER

The two phase interleaved boost converter is as shown in Figure.1. It consists of two conventional boost converters connected in parallel and operates in interleaved fashion. Inductor L1, Switch S1, and Diode D1, forms the first converter while L2, S2 and D2 constitute the second converter. The two phase IBC share the same filter capacitor CO at the output. It is assumed that the parameters of the two converters are identical. The gating signals and the inductor current waveforms of the converter are shown in Figure.2. In case of the two phases, each phase control signal is shifted from each other by 180° as shown in Figure 5. Switching sequences of each phase may overlap depending upon the duty ratio D.

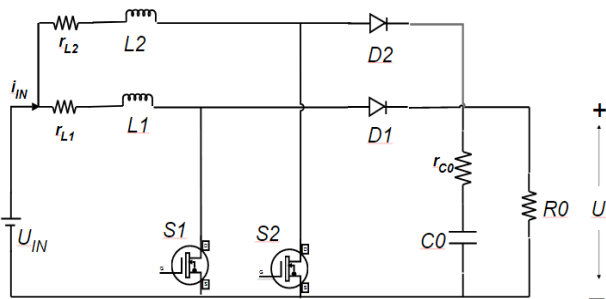


Figure 1: Circuit diagram of 2-phase IBC

The number of switches simultaneously ON is determined by duty cycle D, which is defined by the time that one switch is ON divided by one switching period. The following table 1 gives the 3 region of operation of IBC based on the duty cycle.

Region	Duty cycle	Switches simultaneously ON
R1	($0 < D < 0.5$)	None
R2	($0.5 < D < 1$)	Two

In region R1, no switches are simultaneously ON, which means that this is a forbidden region of operation since a path for the demagnetization of the inductor does not exist when the only switch that is ON turns off. In region R2, 2

switches are ON simultaneously. R2 will be discussed in detail in the following sections for continuous conduction mode (CCM).

A. Working principle

In region R2 and considering CCM operation, the proposed converter has four topological stages per switching period that can be described as follows. Before the first stage, S2 is already conducting.

- Stage 1 ($0 < t < t_1$)

Stage 1 starts when switch S1 and S2 are turned on and the diodes D1 and D2 are reverse biased. Inductor L1 and L2 are magnetized with energy from power source U_IN and current i_L1 and i_L2 increases linearly as shown in the figure 2. The

load receives energy from the output capacitor C_0 . This

topological stage is shown in figure 2.

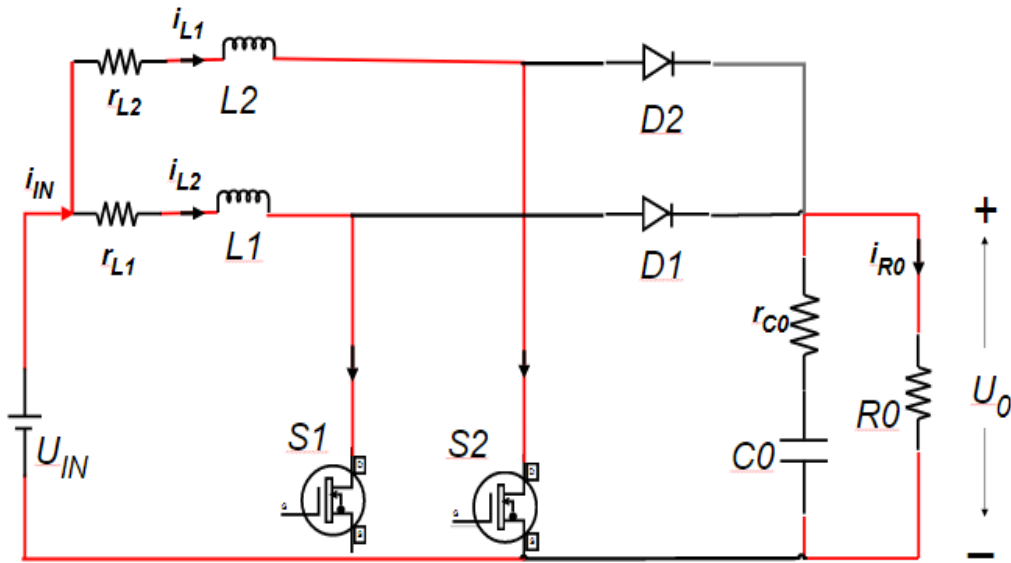


Figure 2 Equivalent circuits of First Third and Fifth stages

- Stage 2 ($t_1 < t < t_2$)

This stage starts when switch S_2 is turned off and hence diode D_2 is reverse biased. Inductor L_2 is demagnetized and current i_{L2} decreases linearly as shown in the figure 2. The load receives energy from

the source and the inductor through diode D_2 . This topological stage is shown in figure 3.

- Stage 3 ($t_2 < t < t_3$)

The third topological stage is same as the first stage.

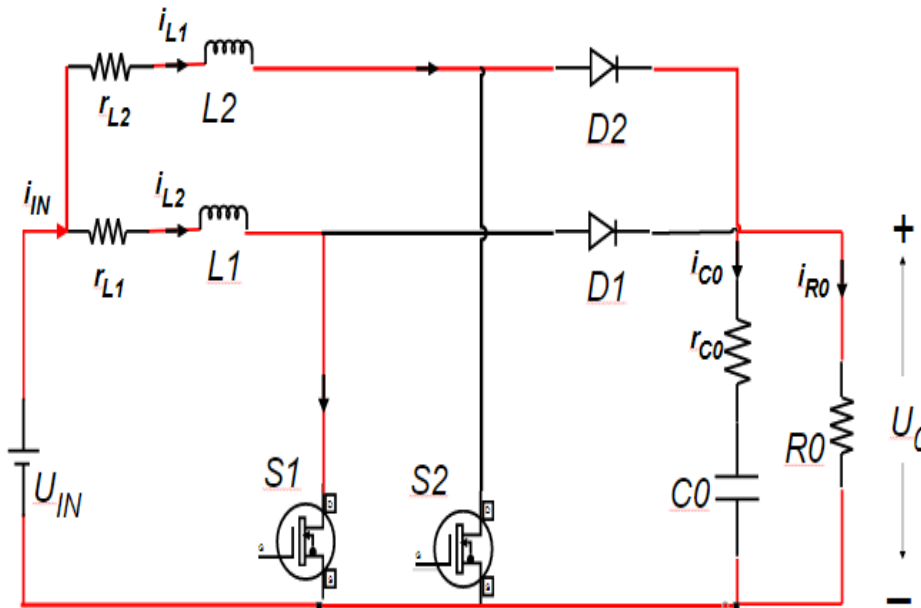


Figure 3. Equivalent circuit of Second stage

- Stage 4 ($t_3 < t < t_4$)

This stage starts when switch S_1 is turned off and hence diode D_1 is reverse biased. Inductor L_1 is demagnetized and current i_{L1} decreases linearly. The load receives energy

from the source and the inductor through diode D_1 . This topological stage is shown in Figure 4. After the fourth stage, the switching period is complete and another period starts with the first stage.

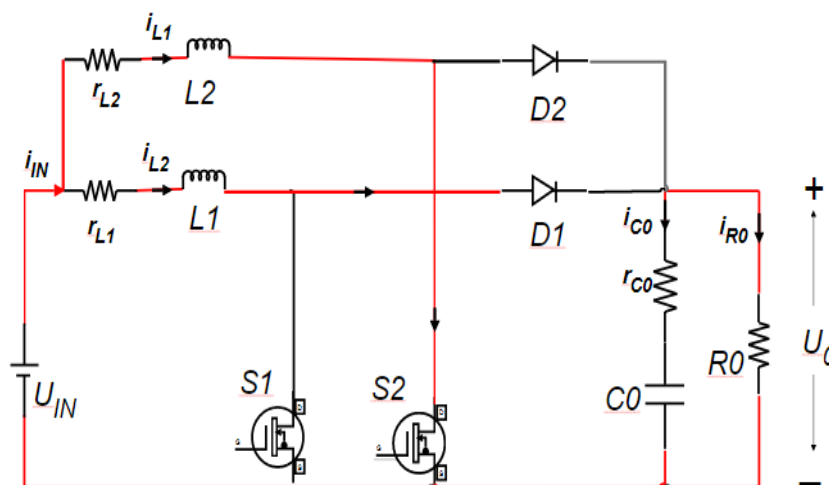


Figure 4 Equivalent circuit of Fourth stage

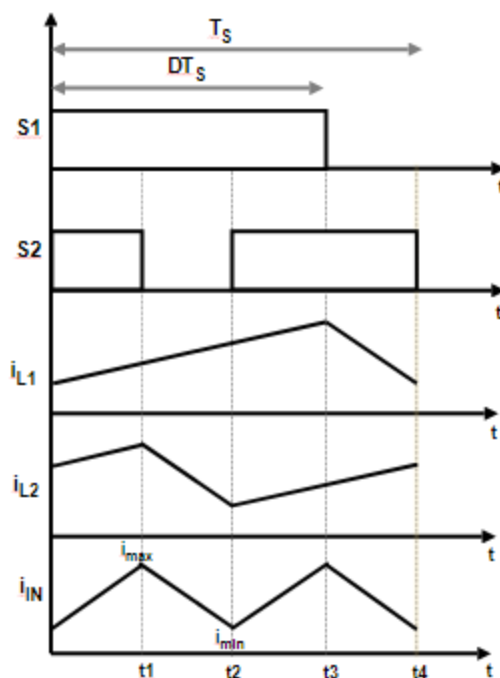


Figure 5 Ideal steady-state waveforms of dc-dc boost converter

Symbol	Description	Units
U_{IN}	Input voltage	Volts
U_0	Output voltage	Volts
U_{C0}	Capacitor voltage	Volts
D	Duty ratio	Unit-less
f_s	Switching frequency	Hz
T_s	Switching period	Seconds
T_{ON}	ON time	Seconds
i_{IN}	Inductor current/Input current	Amperes
i_{L1}	Current across first inductor	Amperes
i_{L2}	Current across first inductor	Amperes
I_o	Output Current	Amperes
i_{min}	Minimum Inductor current	Amperes

i_{max}	Maximum Inductor current	Amperes
i_{R0}	Load current	Amperes
$C0$	Output capacitance	Farad
$R0$	Load Resistance	Ohms
L_b	boundary value of Inductance	Henry
C_{min}	Minimum filter capacitance	Farad
ΔI_{IN}	Input ripple current	Amperes
ΔU_o	Ripple voltage	Volts
N	Number of phases	
P_{Output}	Output Power	Watt
P_{Input}	Input Power	Watt
η	Efficiency	
V_{DS}	Drain to source voltage	Volts
V_{GS}	Gate to source voltage	Volts
$R_{DS(on)}$	On time Drain to source resistance	Ohms

III. DESIGN AND COMPARATIVE ANALYSIS OF 1-PHASE BOOST CONVERTER AND 2-PHASE IBC

Table 2. Design specification

Input Voltage U_{IN}	10V
Output Voltage U_0	20V
Output power P_{Output}	25 Watts
Switching frequency f_s	31 kHz
Input current ripple ΔI_{IN}	5%
Output voltage ripple ΔU_o	2%

A. Calculations

Duty ratio

$$D = 1 - \frac{U_{IN}}{U_o} = 1 - \frac{10}{20} = 0.5$$

$$L = \frac{DU_{IN}}{f_s * \Delta I_{IN}} = \frac{0.5 * 10}{31000 * 0.05} = 1.29mH$$

$$R_o = \frac{U_o}{I_o} = \frac{20}{1.25} = 16\Omega$$

$$I_{IN} = \frac{I_o}{(1 - D)} = \frac{1.25}{(1 - 0.5)} = 2.5A$$

$$CO = \frac{DI_o}{f_s * \Delta U_o} = \frac{0.5 * 1.25}{31000 * 0.02} = 50.403\mu F$$

Considering the same specifications, the inductor and capacitor values of two –phase IBC are calculated,

$$L1 = L2 = \frac{DU_{IN}}{f_s * N * \Delta I_{IN}} = \frac{0.5 * 10}{31000 * 2 * 0.05} = 645\mu H$$

$$CO = \frac{DI_o}{f_s * N * \Delta U_o} = \frac{0.5 * 1.25}{31000 * 2 * 0.02} = 25.20\mu F$$

B. Calculation of efficiency for conventional boost converter

The equation for efficiency is calculated considering all the losses due to the parasitic elements i.e., On state drain-source resistance of the MOSFET $R_{DS(on)}$, series resistance of the diode r_D , internal series resistance of the inductor r_L , internal series resistance of the capacitor r_{CO} .

The values of these parasitic elements are obtained from data sheets of the corresponding component.

1) Losses in the switches due to drain-source resistance

$$R_{DS(on)}$$

$$P_{Switch} = 2 * R_{DS(on)} D \left[\frac{I_{OUT}}{2(1-D)} \right]^2 = 2 * 0.077 * 0.5 * \left[\frac{1.25}{2(1-0.5)} \right]^2 = 0.1203W$$

2) Losses in the diode due to diode series resistance r_D

$$P_{Diode} = r_D I_{OUT}^2 + V_F I_{OUT} = 0.3 * 1.25^2 + 0.875 * 1.5 = 1.78125W$$

3) Losses in the inductor due to internal series resistance r_L

$$P_{Inductor} = r_L \left[\frac{I_{OUT}}{(1-D)} \right]^2 = 0.6 \left[\frac{1.25}{0.5} \right]^2 = 3.75W$$

Losses in the capacitor due to internal series resistance r_C

$$P_{Capacitor} = r_C I_{OUT}^2 = 0.05 * 1.25^2 = 0.078125W$$

$$P_{Input} = P_{Switch} + P_{Diode} + P_{Inductor} + P_{Capacitor} + P_{Output} = 30.85W$$

The input power is the sum of the output power and all the above losses.

The efficiency by

$$\eta = \frac{P_{Output}}{P_{Input}} = \frac{25}{30.85} = 81.03\%$$

The Figure 6 shows the graph of efficiency against duty ratio for both conventional boost converter and 2-phase IBC, it can be observed that the efficiency is decreasing as the duty ratio is increased in both converters. The ripple in the input current against duty ratio is shown in figure 7 for the 1-phase boost converter and 2-phase IBC and it is observed that the ripple current is linearly increasing up to 50% of duty ratio and later decrease to 0 at 100% in case of conventional boost converter where as symmetric waveform in which ripple current is reduced to 0 at a duty ratio of 0.5 is seen for the 2-phase IBC meaning a zero ripple current can be achieved when the 2-phase IBC is operated at 50% duty. It can also be seen that the amplitude of ripple current is higher for 1-phase boost converter and significantly low for the 2-phase IBC.

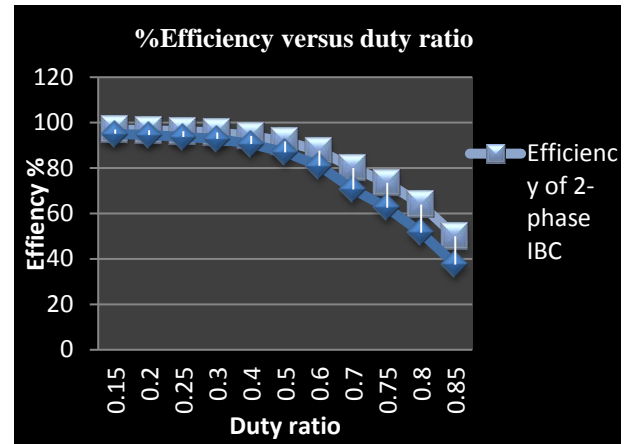


Figure 6. Efficiency versus duty ratio plot

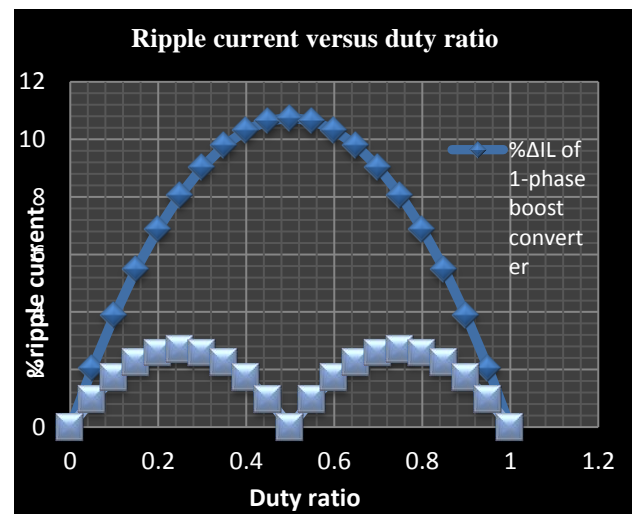


Figure 7. Input Ripple current versus duty ratio plot

IV. MODELING AND ANALYSIS OF TWO-PHASE IBC

A. Modeling

Analysis of two level interleaved boost converter using state space averaging technique. The two phase interleaved boost converter is analysed for duty cycle d ($0.5 < d < 1$). The circuit can be analysed in four modes of operation by considering parasitic elements [6].

The current across the inductors i_{L1} and i_{L2} and the capacitor voltage U_{CO} are considered to be the state variables shown in equation (1) and the state space representation is shown in equation (2).

$$\text{State variables are } \begin{bmatrix} i_{L1} \\ i_{L2} \\ U_{CO} \end{bmatrix} \quad (1)$$

State space representation

$$\begin{aligned} \dot{x} &= Ax + Bv_g \\ y &= Cx \end{aligned} \tag{2}$$

Stage1 (0<t<t1): Switch S1 is closed and S2 is open, in this period inductor current IL1 is rising and IL2 is falling refers figure 2. Analyze the Figure 5 of stage 1 operation, by applying KVL and KCL we get the equation shown below in matrix form.

$$A_1 = \begin{bmatrix} \frac{(r_{L1}+r_{S1})}{L_1} & 0 & 0 \\ 0 & \frac{(r_{L2}+r_{S2})+Rr_c/R+r_c}{L_2} & \frac{R}{(R+r_c)L_2} \\ 0 & \frac{R}{C(R+r_c)} & \frac{1}{C(R+r_c)} \end{bmatrix}$$

$$B_1 = \begin{bmatrix} \frac{1}{L1} & 0 & 0 \\ \frac{1}{L2} & 0 & -\frac{1}{L2} \\ 0 & 0 & 0 \end{bmatrix} \quad C_1 = \begin{bmatrix} 0 & \frac{Rr_c}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix}$$

Stage2 (t1<t<t2): Switch S1 and S2 is closed in this period inductor current IL1 and IL2 is rising refers figure 5. Analyze the Figure 3 of stage 2 operation, by applying KVL and KCL we get the equation as shown below in matrix form.

$$A_2 = \begin{bmatrix} \frac{1}{L1}(r_{L1}+r_{S1}) & 0 & 0 \\ 0 & -(r_{L2}+r_{S2}) & 0 \\ 0 & 0 & -\frac{1}{C(R+r_c)} \end{bmatrix}$$

$$B_2 = \begin{bmatrix} \frac{1}{L1} & 0 & 0 \\ \frac{1}{L2} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad C_2 = \begin{bmatrix} 0 & 0 & \frac{R}{R+r_c} \end{bmatrix}$$

Stage3 (t2<t<t3): Switch S1 is open and S2 is closed in this period inductor current IL1 is falling and IL2 is rising refers figure 5. The KVL and KCL is applied to the circuit in figure 2. to obtain the equation below in matrix form.

$$A_3 = \begin{bmatrix} -\frac{1}{L1} \left(\frac{Rr_c + (R+r_c)(r_{L1}+r_{S1})}{(R+r_c)} \right) & 0 & -\frac{R}{L1(R+r_c)} \\ 0 & -\frac{(r_{L2}+r_{S2})}{L2} & 0 \\ \frac{R}{C(R+r_c)} & 0 & -\frac{1}{C(R+r_c)} \end{bmatrix}$$

$$B_3 = \begin{bmatrix} \frac{1}{L1} & -\frac{1}{L1} & 0 \\ \frac{1}{L2} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

$$C_3 = \begin{bmatrix} \frac{Rr_c}{R+r_c} & 0 & \frac{R}{R+r_c} \end{bmatrix}$$

Stage 4 (t3<t<t4): Switch S1 and S2 is closed in this period inductor current IL1 and IL2 is rising refers figure 5. The KVL and KCL is applied to circuit in figure 4. to obtain the equation shown below in matrix form.

$$A_4 = \begin{bmatrix} -\frac{1}{L1}(r_{L1}+r_{S1}) & 0 & 0 \\ 0 & -\frac{(r_{L2}+r_{S2})}{L2} & 0 \\ 0 & 0 & -\frac{1}{(R+r_c)} \end{bmatrix}$$

$$B_4 = \begin{bmatrix} \frac{1}{L1} & 0 & 0 \\ \frac{1}{L2} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad C_4 = \begin{bmatrix} 0 & 0 & \frac{R}{R+r_c} \end{bmatrix}$$

B. Analysis using small signal modeling

The general, waveforms of inductor currents at steady state in a particular switching cycle of an N-phase interleaved will be shifted by $2\pi/N$ degrees, Based on the assumption that all switching cells carry equal average current and are operated at the same duty ratio in a switching

$$d_{2i-1} = d$$

$$d_{2i} = \frac{1}{N} - d \tag{3}$$

Where $i = 1, 2, \dots, N$, and d is the duty ratio in the switching cycle considered. If d is constant from cycle to cycle, it is defined as the steady-state duty ratio, D . According to the averaged state-space model over one particular cycle can be written as

$$\dot{x} = Ax + Bu_o \tag{4}$$

By applying (4) to the waveforms in figure 5, we obtain

$$A = \sum_{j=1}^{2N} d_j A_j$$

$$B = \sum_{j=1}^{2N} d_j B_j \tag{5}$$

Where A_j and B_j are the state matrix and the control vector of the interval $d_j T_s$ respectively, and $j = 1, 2 \dots 2N$.

We now assume that $d = D$. Using (6.14) in (6.15), we can write

$$A = D \sum_{i=1}^N A_{2i-1} + \left(\frac{1}{N} - D\right) \sum_{i=1}^N A_{2i}$$

$$B = D \sum_{i=1}^N B_{2i-1} + \left(\frac{1}{N} - D\right) \sum_{i=1}^N B_{2i} \tag{6}$$

Substituting number of phases as $N=2$

$$A = D[A_1 + A_3] + [1 - 2D]A_2 \tag{7}$$

$$B = D[B_1 + B_3] + [1 - 2D]B_2 \tag{8}$$

To investigate the small-signal behaviour, we now assume that d varies from cycle to cycle and the perturbations in the input voltage, in the duty ratio and in the states are introduced to (4).

By neglecting the non-linear second-order term, the perturbed state-space equation for an N-phase interleaved converter is obtained as

$$\dot{\tilde{x}} = A\tilde{x} + B\tilde{u}_o + A\tilde{x} + B\tilde{u}_o + \left[\sum_{i=1}^N (A_{2i-1} - A_{2i})\tilde{X} + \sum_{i=1}^N (B_{2i-1} - B_{2i})\tilde{u}_o\right]\tilde{d}$$

(9)

When all perturbations are set to zero, the steady-state model is obtained as

$$X = -A^{-1}BU_o \tag{10}$$

Consequently, the small-signal model (SSM) is found to be

$$\dot{\tilde{x}} = A\tilde{x} + B\tilde{u}_o + \left[\sum_{i=1}^N (A_{2i-1} - A_{2i})\tilde{X} + \sum_{i=1}^N (B_{2i-1} - B_{2i})\tilde{u}_o\right]\tilde{d} \tag{11}$$

Using the Laplace transform in (11) we have the small signal model for N parallel cells as

$$\tilde{x}(s) = (sI - A)^{-1} [Bu_o(s) + \left\{\sum_{i=1}^N (A_{2i-1} - A_{2i})\tilde{X} + \sum_{i=1}^N (B_{2i-1} - B_{2i})\tilde{u}_o\right\}\tilde{d}(s)]$$

(12)

On substituting the corresponding values in the above equation and on simplification the transfer function can be obtained.

$$\frac{\tilde{U}_o(s)}{\tilde{d}(s)} = (sI - A)^{-1} [A_1 + A_3 - 2A_2]X \tag{13}$$

On substituting the matrices derived, in the equation (13), the transfer function is obtained.

$$\frac{\tilde{U}_o(s)}{\tilde{d}(s)} = \frac{U_{IN}}{(1-D)} \frac{2(1-D)^2 / LC_o}{s^2 + \frac{s}{R_o C_o} + \frac{2(1-D)^2}{L_o C_o}} \left(1 - \frac{Ls}{2R_o(1-D)^2}\right) \tag{14}$$

After getting the transfer function of the converter, the same is fed into the SISO design tool command in the MATLAB. Open loop step response is generated Using automated PID tuning in SISOTOOL platform, we can find the K_p and K_i values to feed into PID controller.

IV. SIMULATION RESULTS

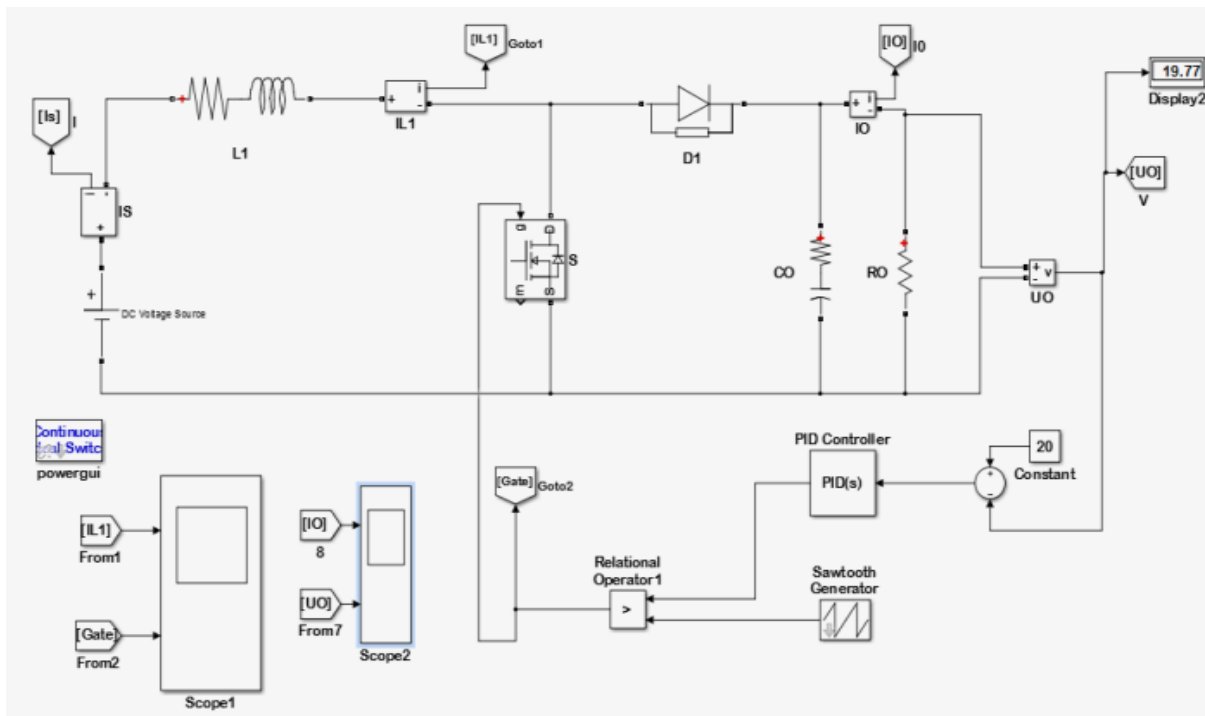


Figure 8. 1-phase Closed loop Boost Converter in Simulink

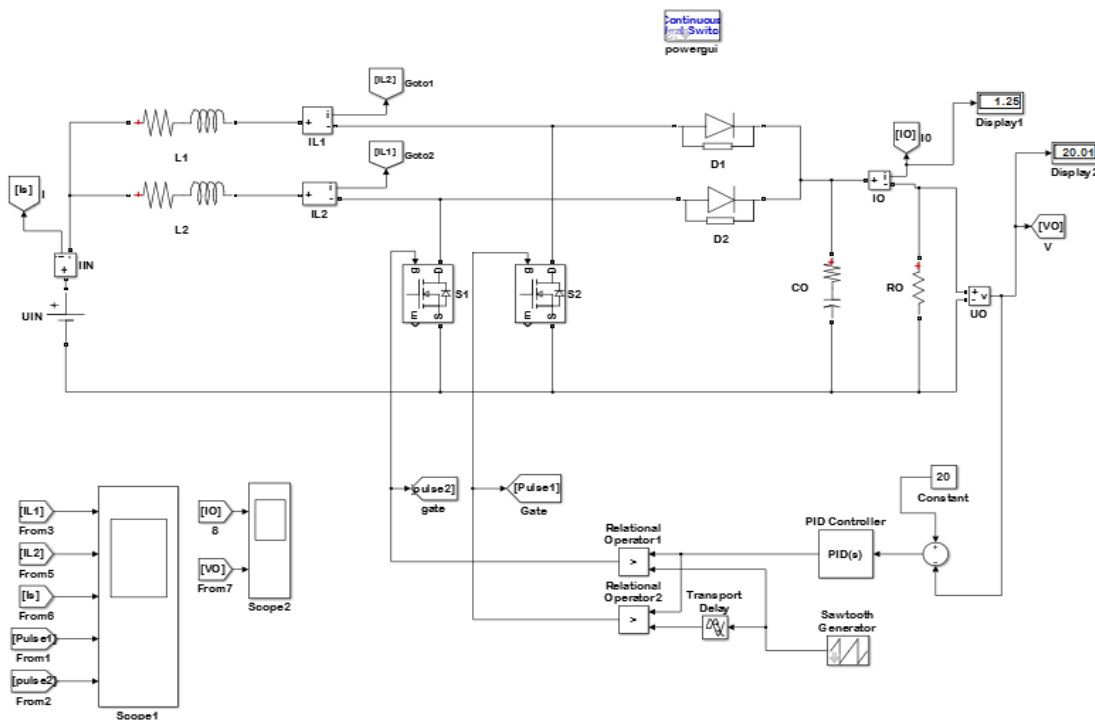


Figure 9. 2-phase IBC Closed loop circuit in Simulink

The figure 8 and figures 9 shows a closed loop simulation of 1-phase conventional boost converter and 2-phase IBC respectively in the Simulink software platform.

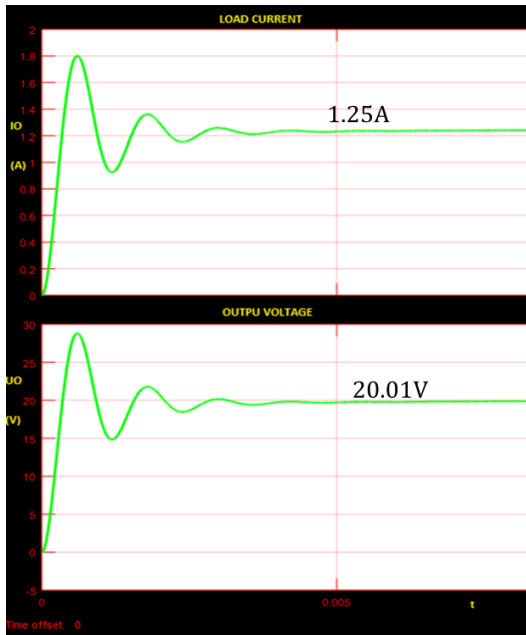


Figure 9. Voltage and current waveforms of closed loop circuit of 2-phase IBC

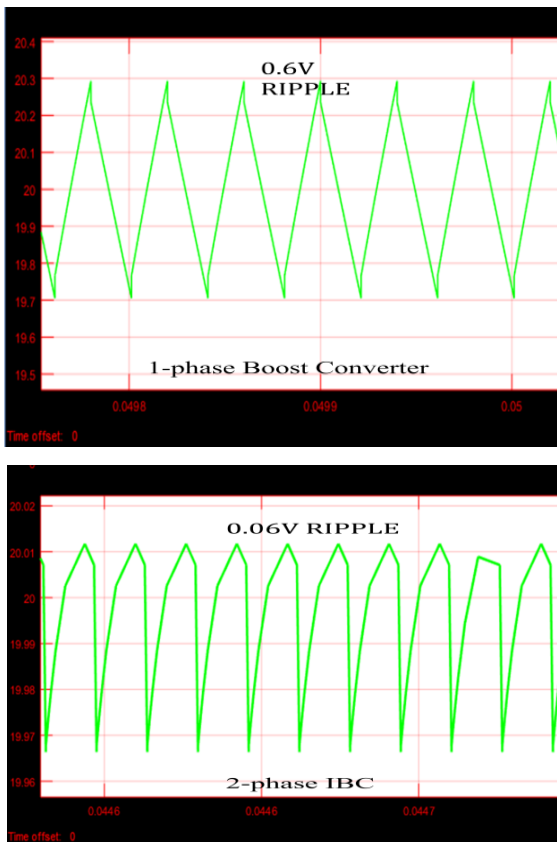


Figure 10. Ripple in voltage waveforms of closed loop circuits

From figure 9, it can be observed that there is an initial transients in the output waveform from 27V to 15 V, followed by an increase in voltage and it settles to 20 at 4ms. Figure 10,shows the ripple voltage present in the voltage waveforms, and it is observed the ripple is reduced to 0.06V.

Inductor current and gate pulse waveforms are shown in figure 11. It can be observed that the individual Inductor current has a peak-to-peak ripple of 0.3A and the peak-to-peak ripple in the total input current is nullified. The input current I_{IN} is the sum of I_{L1} and I_{L2} , as they are in phase opposition, there is the ripple cancellation in the input current and hence ripple gets reduced.

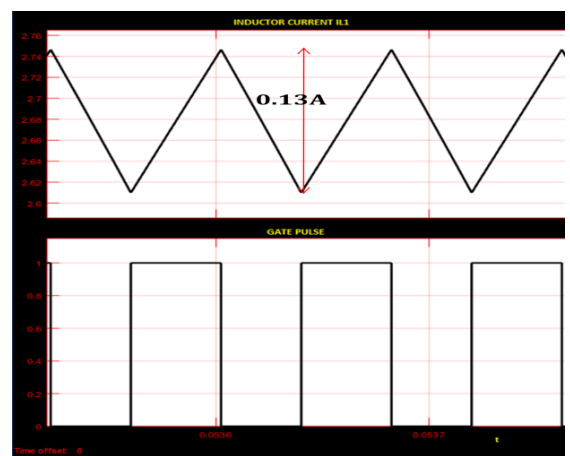


Figure 10. Inductor current and gate pulse waveforms of closed loop 1-phase boost converter circuit

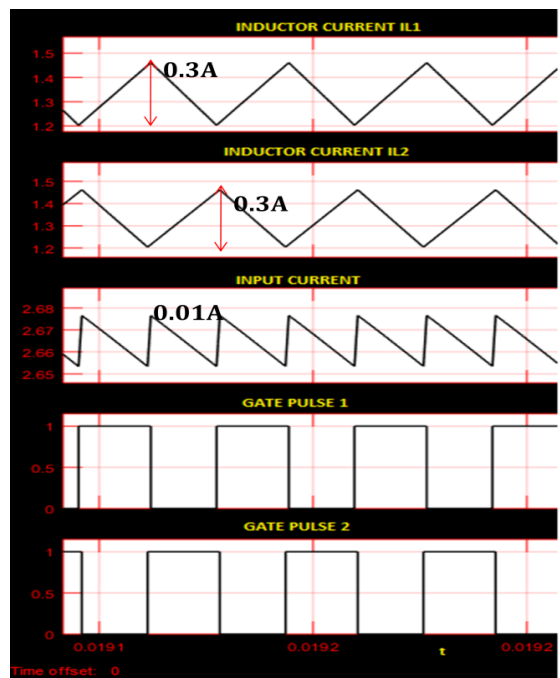


Figure 11. Inductor current and gate pulse waveforms of closed loop 2-phase IBC circuits

Voltage and Current Waveforms for 10% line regulation of 2-phase closed loop IBC is shown in figure 12.

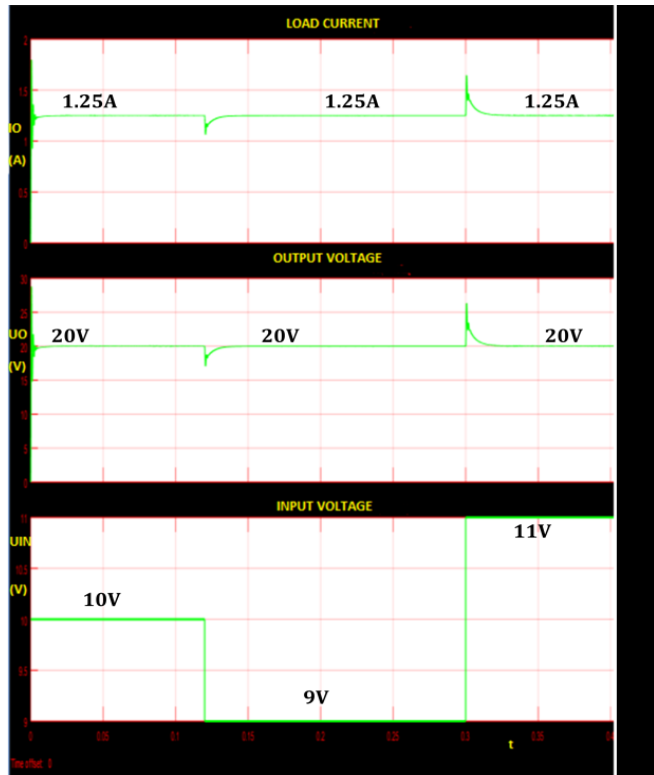


Figure 12 Line regulation waveforms

Table 3: COMPARISON OF SIMULATION RESULTS BETWEEN 1-phase Boost Converter AND 2-PHASE IBC

Parameter	1-phase Boost Converter	2-phase IBC
Input Ripple current	0.13A	0A
Out put Voltage ripple	3%	0.3%
Filter size	1.29mH	645μH
Output capacitor filter size	50.403μF	25.20μF

V. HARDWARE IMPLEMENTATION AND RESULTS

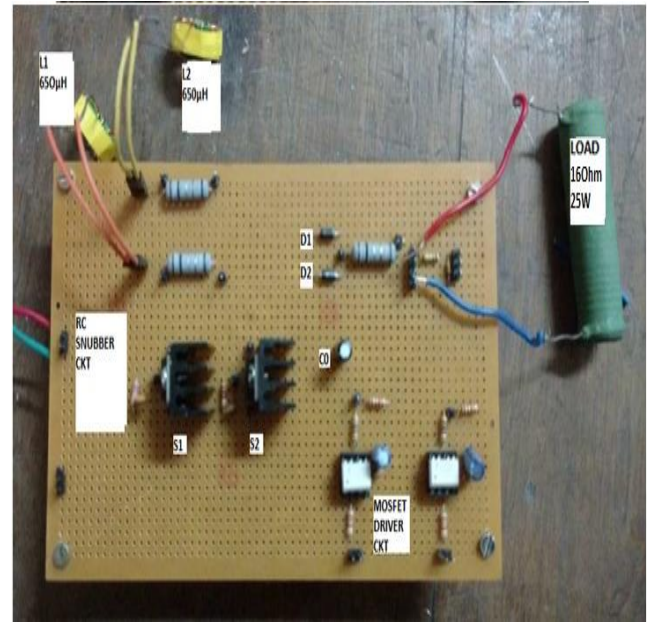


Figure 13. Hardware setup of 2-Phase IBC

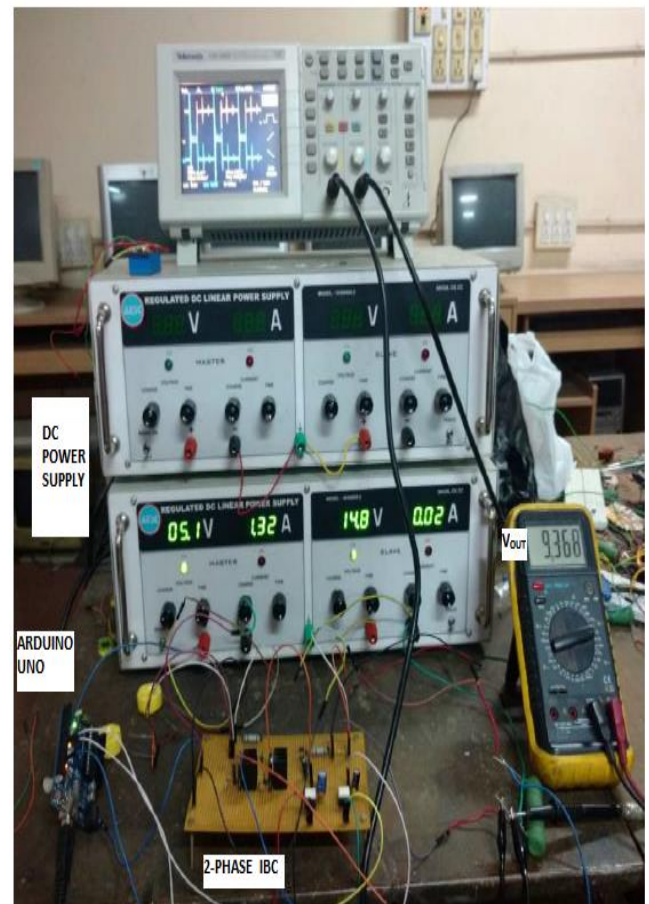


Figure 14 Complete hardware setup of 2-phase IBC

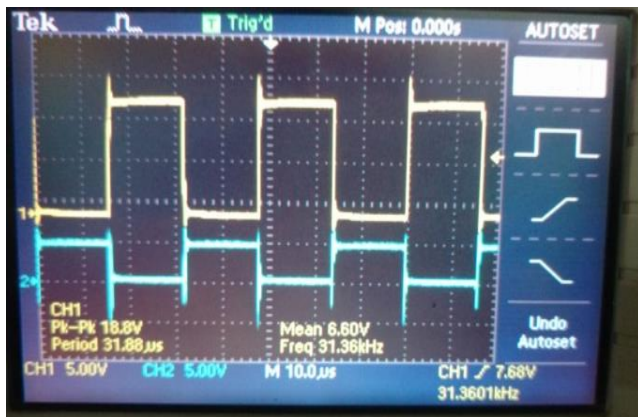
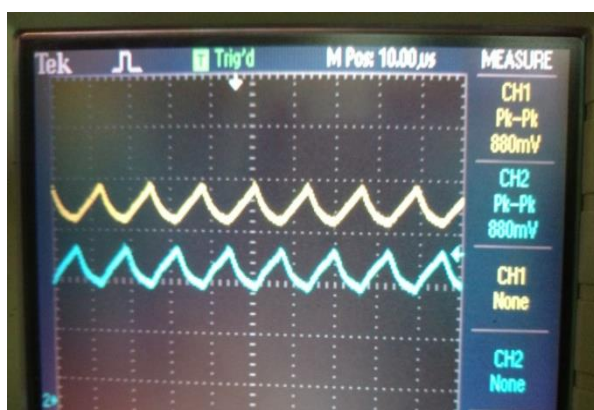


Figure 15 Switching waveform of MOSFET

Figure 16 Waveform of inductor currents I_{L1} and I_{L2} of 2-phase IBCFigure 17 Waveform of total Input current I_{iN} of 2-phase IBC

The waveform of the current measured across inductors $L1$ and $L2$ is shown in the figure 16. The peak to peak ripple in the current is observed to be 880mV.

The figure 17 shows the total input current which is equal to the sum of two inductor currents. From the figure it

is observed that the total current waveform is at a frequency of 66.01 kHz and the peak-to-peak ripple is reduced to 400mV.

VI. CONCLUSION AND FUTURE SCOPE

A. Conclusion

The conventional boost converter and 2-phase IBC is modelled using state space averaging technique considering all parasitic elements of the converter which gives the accurate modelling of the converter. And the modeling is analysed based on small signal analysis to find the transfer function output voltage to variations in duty ratio. The conventional boost converter and 2-phase IBC is designed, in which the size of passive components i.e., Input inductors and output side capacitor filter is halved.

Also Simulation is performed in Matlab-Simulink for the designed values and an expected output is achieved in both open and closed loops.

The hardware implementation is performed for the designed values and tested. The gate pulses for a duty ratio of 50% and at a frequency of 31 kHz are generated using Arduino Uno Microcontroller. Also from the hardware implementation, it can be seen that the ripple in the total inductor current is reduced by half, which is from 940m of ripple current of conventional boost converter to a peak-to-peak of 400m for the 2-phase IBC. Thus the 2-phase IBC is able to achieve the objectives of reducing the size of the passive components and decreasing the ripple in input current thus achieves a higher efficiency.

Also from the results the following conclusions can be drawn:

1. Interleaving techniques divides the current between the phases at a same frequency equal to the switching frequency.
2. As the input current is the sum of the two inductor current of the two phases, the frequency of the total input current is twice that of the switching frequency.
3. Also the frequency of the output voltage ripple is high.
4. The switching DC-DC power supply has inductor current ripple leading to output voltage ripple.

B. Future Scope

Methods discussed herein can be extended to other converter types like boost, buck boost and similar other derivatives. The closed loop control conventional boost converter and the 2-phase interleaved boost converter is simulated using PID controller and implemented using Arduino

microcontroller. As a future scope, a high step-up interleaved boost converter can be simulated with different types of feedback control like fuzzy logic[10]control, genetic algorithm ,artificial neural network and others[11] for power quality improvement or to get high efficiency advanced tuning and to check the constant output voltage with least ripple and to support different appliances with different voltage ratings.

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