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A Frame of Multiplier using Compactor

S.L.Bharathi
Assistant Professor
Dept. of ECE
Panimalar Engineering College
Chennai, India

N.Pritha
Assistant Professor
Dept. of ECE
Panimalar Engineering College
Chennai, India

G.Srividhya
Assistant Professor
Dept. of ECE
Panimalar Engineering College
Chennai, India

D.PadmaPriya,
Associate Professor
Dept. of ECE
Panimalar Engineering College
Chennai, India

Abstract:- In this paper, Multiplier is designed efficiently using compactor to make them suitable for diverse speed, low power and compact VLSI implementations. Mainly two conflicts absorbed in VLSI implementation are area and speed. Our proposed design contributes best tradeoff between area and speed. In this paper three steps involved namely generation, reduction and addition. Compactor structure considerably reduces the delay time of the overall system.

Keywords:-*Addition, Compactor, Generation, Multiplier.*

I. INTRODUCTION

Fast computing is an essential drive to achieve advancement in Digital world. To incorporate fast computing, an efficient design of Multipliers and adders are necessary. In modern day processors, addition and multiplication of two binary numbers are frequently used arithmetic operations and utilize more than 70 percent of the execution time. Importantly the key hardware block in most digital and high performance systems is the multiplier unit. This necessitates the need for high speed processing for expanding computer and signal processing applications. Diverse multipliers and adders such as Array Multiplier, Sequential Multiplier, and Combinational Multiplier, Half adder, Full Adder and Ripple Carry Adder are realized in [1-4]. Researchers upgrade these designs with the aim to scale down the complexity in the design and execution time.

Multiplier is one of the intensive hardware with various criteria of interest affecting overall circuit performance in terms of power consumption, cost, area and computation speed. Current architecture range from small, low performance shift and add multipliers, to large, high performance structure, but require large amount of silicon. Multipliers have become popular because of its low complexity and less power three phases - generation of partial products, reduction of consumption. Exact computing produces reasonable result, partial products and final stage addition. In approximate computing, the value products take much time and power in the multiplier.

Several Approximation methodologies were applied in generating the partial product phase [5]. A 2 × 2 bit approximate multiplier is designed by altering the one output combination. The probability of getting error in this multiplier is reasonably observed in the partial product generation phase. Adder tree (reduction tree) of this multiplier is same as accurate multiplier.

Several other approximation techniques were proposed in the partial product reduction stage [6]–[8]. The technique called row and column bypassing is utilized in [6]. In [7], some of carry-save adders are skipped in both horizontal and vertical directions based on the number of zeros in the multiplier input. In [8], partial product tree is divided into two parts. Accurate multiplier was used in MSB side of the multiplier. No multipliers were used in LSB side where approximation rule was applied.

In [9], ‘‘n’’ bit multiplier was implemented by two ‘‘n/2’’ bit sub-multipliers. Then, all partial products are accumulated by a Wallace tree. Every technique has its own merits and demerits. Getting lesser delay and better circuit performance are always challenging task.

By inculcating the challenge involved in the multiplier unit, efficient multiplier design using compactors are proposed in this paper. Compactors design in the multiplier unit structured in such a way to make it suitable for diverse speed, low power and compact implementations.

In this paper, Section II describes the conventional design and system design of proposed structure. Section III briefly describes the architecture and concepts of Compactors used in the design. Simulation results with schematic diagram and waveforms of overall structure and compactors used are listing in Section IV. Finally Section V conclude the report.

II. SYSTEM DESIGN

Multiplier architecture divides in three stages- generation, reduction and addition.

A. Conventional Multiplier Unit

The conventional array multiplier consists of various full adders and half adders. The carry generated by each stage in the adders is transversely propagated to the next stage. Maximum combinational path delay for the conventional multiplier is 35.096ns which is reduced in the proposed system.

B. Proposed Advanced Multiplier Unit

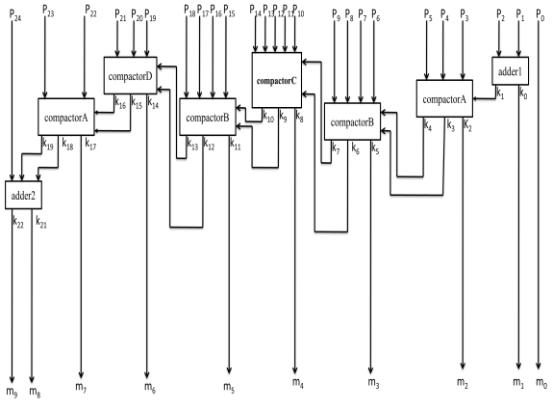

Fig.1:- Architecture of multiplier

- *Generation*

Using AND operation, the partial products are generated. The outputs of the partial products are introduced as the input to compactor involved in the Multiplier design.

- *Reduction*

In conventional multipliers, partial products addition stages introduce the large delay which increases the amount of power consumed.

- *Addition*

Addition is the final stage, using adder1 and adder2 along with the compactors to get the final result of the multiplier. Each compactor produce n bits, among that one bit output considered as perfect output and remaining carried over to next stage.

III. ARCHITECTURE OF COMPACTORS

Four compactors are used in the proposed design namely compactor A, compactor B, compactor C, compactor D.

A. Compactor A

The compactor A consists of four inputs and produces 3 outputs. The design of compactor A counts the number of 1's at the inputs and produces the output. If all the inputs of compactor A are 1, then its output in decimal equivalent is 4.

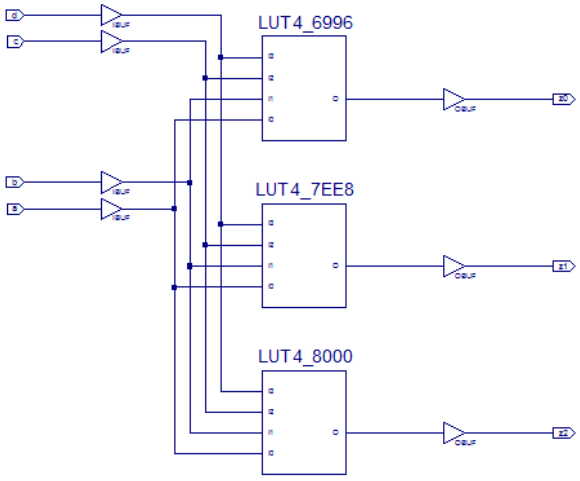

Fig.2:- Schematic Diagram of Compactor A

B. Compactor B

The Compactor B consists of six inputs and produce 3 outputs. The design of compactor B counts the number of 1's at the inputs and produces the output. If all the inputs of compactor B is 1, then its output in decimal equivalent is 6.

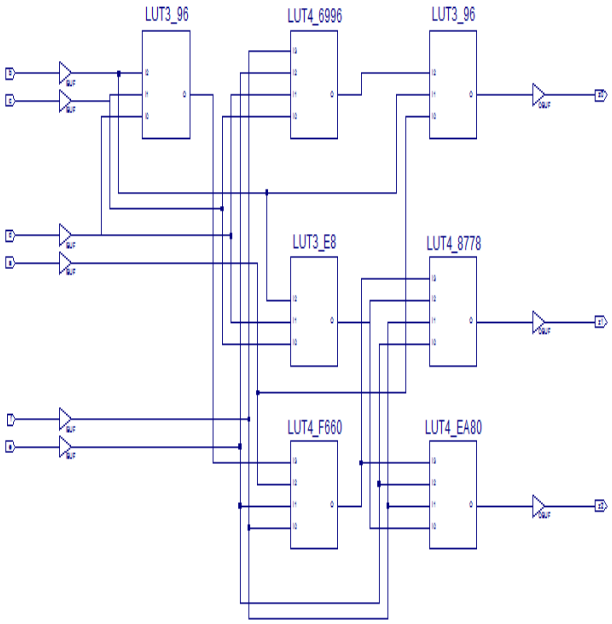

Fig.3:- Schematic Diagram of Compactor B

C. Compactor C

The compactor C consists of seven inputs and produces 3 outputs. The design of compactor C counts the number of 1's at the inputs and produces the output. If all the inputs of compactor C is 1, then its output in decimal equivalent is 7.

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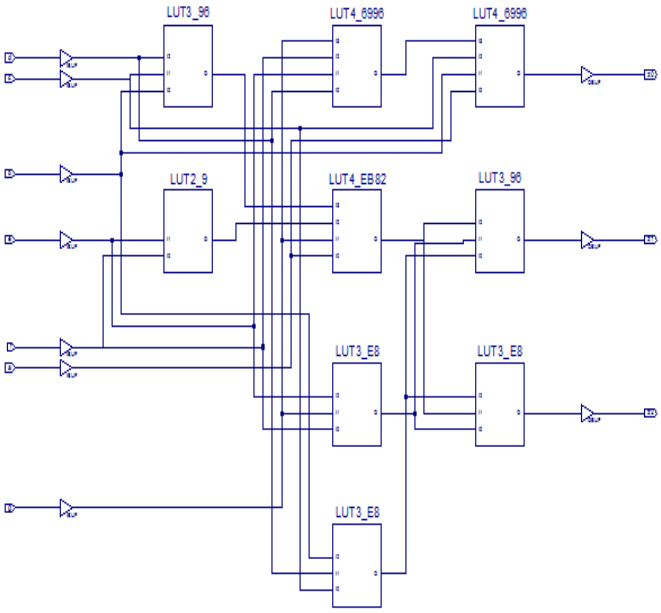

Fig.4: Schematic Diagram of Compactor C

D. Compactor D

The compactor D consists of five inputs and produces 3 outputs .The design of compactor D counts the number of 1's at the inputs and produces the output. If all the inputs of compactor D is 1, then its output in decimal equivalent is 5.

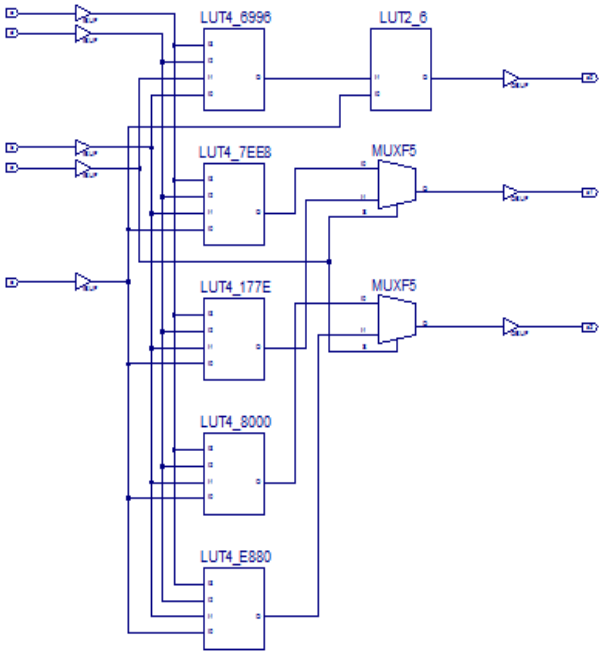

Fig.5: Schematic Diagram of Compactor D

IV. SIMULATION RESULTS

Simulation results of Compactor A, Compactor B, Compactor C, Compactor D and for overall Multiplier unit follows. From the simulation results, expected outputs are verified. Results of compactor show that addition of n-bits is possible using respective compactor circuit. The overall output of the system shows that expected output of the 5 bit Multiplier.

Fig.6:- Simulation result of Compactor A

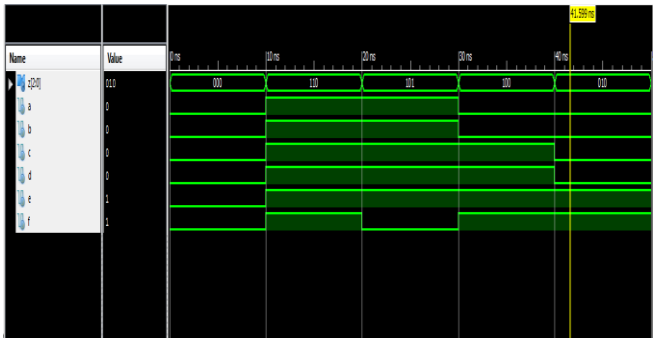

Fig.7:- Simulation result of Compactor B

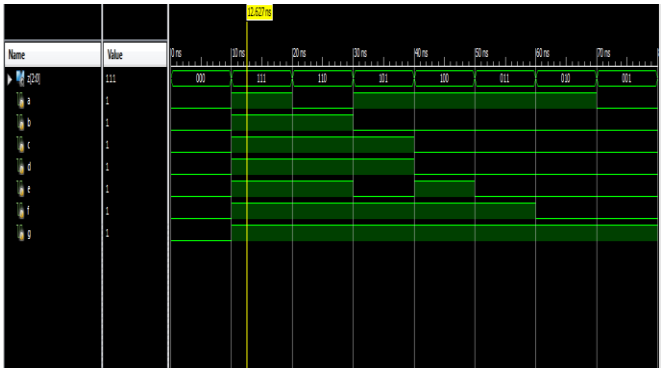

Fig.8:- Simulation result of Compactor C

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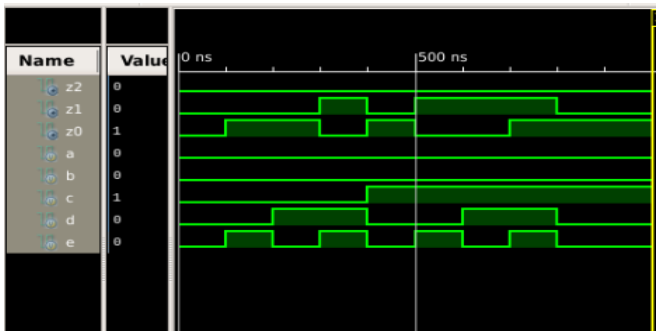

Fig.9:- Simulation result of Compactor D

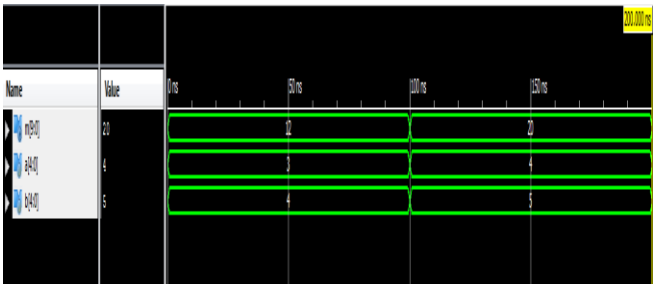

Fig.10:- Simulation result of Multiplier

V. CONCLUSION

In this paper, efficient multiplier is framed using compactor for the diverse speed, low power and compact VLSI implementations. Compactor structure considerably reduces the delay time of the overall system. The maximum combinational path delay for the conventional multiplier is 35.096ns which is reduced to 30.736ns.As the delay is reduced; speed is increased in our design. Hence there is a best tradeoff between speed and area.

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