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An Efficient Low – Power Viterbi Decoder using Dual Port Memory

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Abstract:- **Viterbi decoder is widely used for decoding of convolutional codes. The Viterbi algorithm is used in communication and data storage applications. Viterbi decoder is an inevitable module which determines the overall power consumption of TCM decoders. An efficient low-power Viterbi decoder using dual port memory is designed here pre-computation architecture using T-algorithm can reduce the power consumption without reducing the decoding speed. Dual ported RAM is used for improving the memory efficiency. Dual ported RAM (DPRAM) is a type of random access memory that allows multiple reads or writes to occur at the same time or nearly the same time, unlike single ported RAM which only allows one access at a time. A comparison of conventional VD parameters and VD designed using DPRAM shows the reduction in area and power consumption as well as in increase in speed too.**

Keywords:- *VD, TCM, DPRAM, Convolutional codes.*

I. INTRODUCTION

Viterbi algorithm is a well-known maximum-likelihood algorithm for decoding of convolutional codes. Convolutional codes are frequently used to correct errors in noisy channels. They have rather good correcting capability and perform well even on very bad channels. Convolutional codes are extensively used in satellite communications. Although convolutional encoding is a simple procedure, decoding of a convolutional code is a complex task. Trellis coded modulation (TCM) schemes are used in many bandwidth-efficient systems. Typically, a TCM system employs a high-rate convolutional code, which leads to a high complexity of the Viterbi decoder (VD) for the TCM decoder, even if the constraint length of the convolutional code is moderate. For example, the rate-3/4 convolutional code used in a 4-D TCM system for deep space communications [1] has a constraint length of 7; however, the computational complexity of the corresponding VD is equivalent to that of a VD for a rate-1/2 convolutional code with a constraint length of 9 due to the large number of transitions in the trellis. Therefore, in terms of power consumption, the Viterbi decoder is the dominant module in a TCM decoder. In order to reduce the computational complexity as well as the power consumption, low-power schemes should be exploited for the VD in a TCM decoder.

As a preliminary work an add-compare-select unit (ACSU) architecture based on pre-computation for VDs incorporating T-algorithm, which efficiently improves the clock speed of a VD with T -algorithm for a rate-3/4 code was proposed. A systematic way to determine the optimal pre-computation steps is presented, where the minimum number of steps for the critical path to achieve the theoretical iteration bound is calculated and the computational complexity overhead due to pre-computation is evaluated. In order to overcome the limitations a design using Dual ported RAM is presented here. DPRAM can read and write different memory cells simultaneously at different addresses.

In the second section the works related to VD design which existed earlier are presented. Section III describes the proposed design and its comparison with the previous works. Synthesis and power estimation results are presented in section IV. Conclusions are given in section V.

II. RELATED WORK

Power reduction in VDs could be achieved by reducing the number of states (for example, reduced-state sequence decoding (RSSD), M-algorithm and T-algorithm) or by over-scaling the supply voltage. Over-scaling of the supply voltage usually needs to take into consideration the whole system that includes the VD (whether the system allows such an over-scaling or not), which is not the main focus. RSSD is in general not as efficient as the M-algorithm, and T -algorithm is more commonly used than M-algorithm in practical applications, because the M-algorithm requires a sorting process in a feedback loop while T -algorithm only searches for the optimal path metric (PM), that is, the minimum value or the maximum value of all PMs. T-algorithm has been shown to be very efficient in reducing the power consumption. However, searching for the optimal PM in the feedback loop still reduces the decoding speed. To overcome this drawback, two variations of the T-algorithm have been proposed

A. Relaxed Adaptive VD

Relaxed adaptive VD[6] is a modified form of adaptive VD that completely eliminates the global best survivor path metric search operation. The adaptive Viterbi algorithm, which combines the Viterbi algorithm with the principle of T- algorithm, has a computational complexity which adapts to run time channel conditions. This approach has a great potential of realizing significant power savings.

In contrast to the Viterbi algorithm ,in the adaptive Viterbi algorithm ,the winner path at each trellis[5] state does not necessarily become a survivor path, i.e., only those whose path metrics are better than a global non-survivor purge

limit[9] will be fed to the next decoding depth as survivors. The non-survivor purge limit is determined b the overall best inner path at each decoding depth and varies from one decoding depth to the next. Due to its serial nature ,the search-for –the-best-winner-operation tends to have a much longer latency than the other operations within the recursive decoding loop. For a VLSI implementation of the adaptive Viterbi algorithm, the long latency due to such a search operation may be concealed by using state-serial decoder architectures or partially state-parallel decoder architecture at the cost of achievable decoding throughput .

When applied to high rate convolutional codes, the relaxed adaptive VD suffers a severe degradation of bit-error-rate(BER) performance due to the inherent drifting error rate between the estimated optimal PM and the accurate one. Computational overhead and decoding latency will be more. Hence it cannot be used in TCM decoders.

B. Limited search parallel state VD

A low complexity algorithm based on a limited search algorithm, which reduces the average number of the add-compare-select computation of the Viterbi algorithm[2],is proposed and seamlessly integrated with the SST-based decoder[8].The new decoding scheme has low overhead and facilitates low-power implementation for high throughput applications.

The SST [3] based scheme requires pre-decoding and re-encoding processes and is not suitable for TCM decoders. The computational overhead and decoding latency [7] due to pre-decoding and re-encoding of the TCM signal become high.

III. PROPOSED SYSTEM

Viterbi Decoder is the dominant module determining the overall power consumption of TCM decoders. We propose a pre-computation architecture incorporated with T-algorithm for VD, which can effectively reduce the power consumption without degrading the decoding speed much. To improve memory efficiency.

,Dual port memory based trace-back (TB) method to be used. This technique is used for path history management in the chip designs of decoders. Dual ported RAM(DPRAM) is a type of Random Access Memory that allows multiple reads or writes to occur at the same time, or nearly the same time, unlike single ported RAM which allows one access at a time. First, branch metrics (BMs) are calculated in the BM unit (BMU) from the received symbols. In a TCM decoder, this module is replaced by transition metrics unit (TMU), which is more complex than the BMU. Then, BMs are fed into the ACSU that recursively computes the PMs and outputs decision bits for each possible state transition. After that, the decision bits are stored in and retrieved from the SMU in order to decode the source bits along the final survivor path The PMs of the current iteration are stored in the PM unit (PMU). T -algorithm requires extra computation in the ACSU loop for calculating the optimal PM and puncturing states. Therefore, a straightforward implementation of T -algorithm will dramatically reduce the decoding speed. The key point of improving the clock speed of M –algorithm is to quickly find the optimal PM.

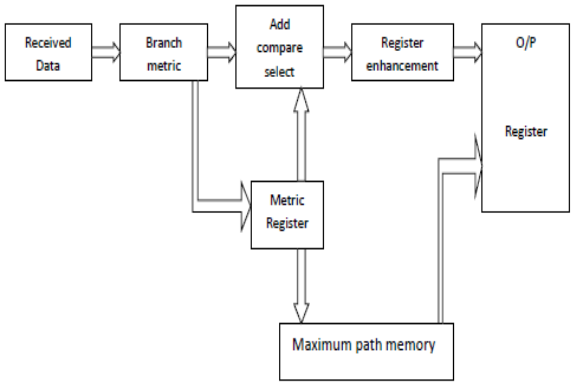

Fig 1:- Complete block diagram of VD

A. Branch metric calculation s

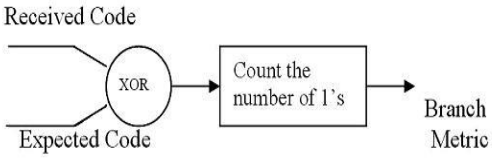

Fig 2:- Branch Metric Unit

A branch metric unit's function is to calculate branch metrics, which are normed distances between every possible symbol in the code alphabet, and the received symbol. There are hard decision and soft decision Viterbi decoders. A hard decision Viterbi decoder receives a simple bit stream on its input, and a Hamming distance is used as a metric. A soft decision Viterbi decoder receives a bit stream containing information about the reliability of each received symbol. For a soft decision decoder, a branch metric is measured using the Euclidean distance.

Let x be the first received bit in the pair, y – the second, x0 and y0 – the "ideal" values. Then branch metric is:

$$Mb = (x - x0)2 + (y - y0)2$$

Furthermore, when we calculate 4 branch metric for a soft decision decoder, we don't actually need to know absolute metric values – only the difference between them makes sense. So, nothing will change if we subtract one value from the all four branch metrics:

$$Mb = (x2 - 2\,x\,x0 + x0\,2) + (y2 - 2\,y\,y0 + y0\,2)$$

$$Mb^* = Mb - x2 - y2 = (x0\,2 - 2\,x\,x0) + (y0\,2 - 2\,y\,y0)$$

The second formula, *Mb* *, can be calculated without hardware multiplication: *x*02 and *y*02 can be pre-calculated, and multiplication of *x* by *x0* and *y* by *y0*

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Can be done very easily in hardware given that *x0* and *y0* are constants. It should be also noted that *Mb* * is a signed variable and should be calculated in 2's complement format. For instance, in a 3-bit encoding, this reliability information is encoded as follows.

value	Meaning
000	strongest 0
001	relatively strong 0
010	relatively weak 0
011	weakest 0
100	weakest 1
101	relatively weak 1
110	relatively strong 1

Table 1. Reliability information in 3-bit encoding

B. Path metric calculation

A path metric unit summarizes branch metrics to get metrics for paths, where K is the constraint length of the code, one of which can eventually be chosen as optimal. Every clock it makes decisions, throwing off wittingly non optimal paths. The results of these decisions are written to the memory of a trace back unit. The core elements of a PMU are ACS (Add-Compare-Select) units. The way in which they are connected between themselves is defined by a specific code's trellis diagram. The two adders compute the partial path metric of each branch. The comparator compares the two partial metrics. The selector selects an appropriate branch. The new partial path metric updates the state metric of state, and the survivor path-recording block records the survivor path. Path metrics are calculated using a procedure called ACS (Add-Compare-Select). This procedure is repeated for every encoder state.

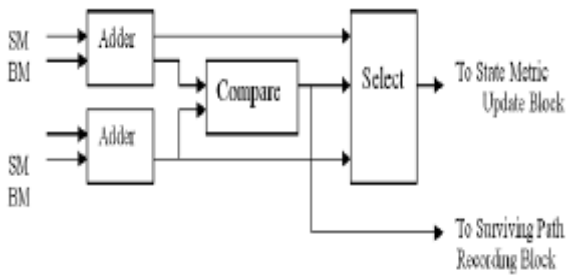

Fig 3:- Add Compare Select Unit

C. Trace Back Unit

Back-trace unit restores an (almost) maximum-likelihood path from the decisions made by PMU. Since it does it in inverse direction, a Viterbi decoder comprises a FILO (first-in-last-out) buffer to reconstruct a correct order. The general approach to trace back is to accumulate path metrics for up to five times the constraint length (5 * (K - 1)), find the node with the largest accumulated cost, and begin trace back from this node. However, computing the node which has accumulated the largest cost (either the largest or smallest integral path metric) involves finding the maxima or minima of several (usually 2^{K-1}) numbers, which may be time consuming when implemented on embedded hardware systems. DPRAM is a type of RAM that allows multiple reads or rites to occur at the same time or nearly the same time. Video RAM or VRAM is a common form of dual ported dynamic RAM commonly used for allowing CPU to draw the image at the same time the video hardware is reading it out to the screen DPRAM is a type of RAM that allows multiple reads or rites to occur at the same time or nearly the same time. Video RAM or VRAM is a common form of dual ported dynamic RAM commonly used for allowing CPU to draw the image at the same time the video hardware is reading it out to the screen.

Dual ported RAM can read and write different memory cells simultaneously at difference address. DPRAM consists of a left and right CPU, data and address IOs, control logic, RAM own to perform automated tasks that have been structured in to the program. DPRAM operates mainly in six modes. They are write first, read after write, read first, read before write, no change or no read or write mode, default mode. To assist in arbitrating between ports, a fully independent semaphore logic block is provided memory cells, busy lines and interrupt semaphore lines. The control logic responds to commands from the user, and also it acts on its

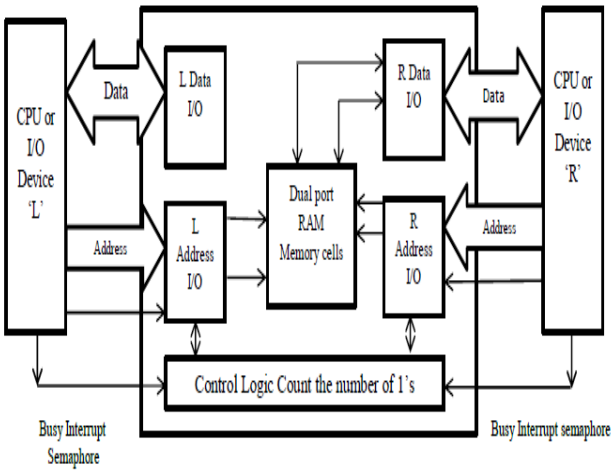

Fig 4:- Dual Ported RAM

IV. SYNTHESIS AND IMPLEMENTATION RESULTS

The Viterbi decoder using a pre-computation architecture incorporated with T-algorithm has been modeled using VHDL code. The proposed pre computation scheme using dual port RAM has got better performance.

	Conventional T algorithm		Pre-computation architecture with DPRAM	
Minimum period	7.80ns		6.077ns	
On chip power	0.020w		0.072w	
Resource Estimation	Register	69/1200 (6%)	Register	69/23324(1%)
	LUT	111/1200 (9%)	LUT	111/23324(1%)
	Block memory	2/12 (17%)	Block memory	2/172(1%)
	IO	5/32(4%)	IO	5/132(4%)

Table 2. Synthesis and Implementation Results

V. DISCUSSION AND CONCLUSION

A low power high speed Viterbi decoder design using Dual ported RAM has been proposed here. The pre-computation architecture using T-Algorithm can improve the speed of decoding by reducing the delay in decoding. This design has minimal power overhead and maximum clock frequency. A design is presented here where the SMU unit is replaced using a Dual Ported RAM which improves the memory efficiency of this decoder. Resource utilization in this design is less and hence the area required is small compared to conventional decoders

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