ISSN No:-2456-2165

Design of Carry Select Adder for Image Processing

Sriram k_1, Diviya KP_2, Vinothkumar T_3, Jeyaprabhu k_4, Kathirvel P_5
[1,2,3,4]UG Students, Department of Instrumentation and Control Engineering, INDIA
[5]Assistant Professor of Department of instrumentation and Control Engineering
Dr.Mahalingam College of Engineering and Technology, Pollachi, INDIA

Abstract:- Digital image processing is one of the extensively used techniques in real life application in the field of Very Large Scale Integration (VLSI). Digital image processing techniques help in manipulation of the digital images by using computer algorithms. The use of carry select adders in Image addition shows reduced propagation delay and fast addition. By modifying the basic design of CSLA will results in high accuracy and less power consumption for image processing applications. In this paper, different designs such as Normal CSLA, Modified CSLA and Conventional CSLA are done. On comparing these designs, the result analysis shows that Conventional CSLA is achieved with greater accuracy and less area, delay and power consumptions.

Keywords:- *CSLA, Adder, FPGA, Image Processing.*

I.INTRODUCTION

Digital image processing has wide applications and almost all of the technical fields are impacted by DIP. Digital Image processing is not just limited to adjust the spatial resolution of the everyday images captured by the camera. It is not just limited to increase the brightness of the photo, etc. Rather it is far more than that. Digital image processing is the use of computer algorithms to perform image processing on digital images. Digital image processing algorithms can be used to: Convert signals from an image sensor into digital images, Improve clarity and remove noise and other artifacts. As a subcategory or field of digital signal processing, digital image processing has many advantages over analog image processing. It allows a much wider range of algorithms to be applied to the input data and can avoid problems.

We have designed Conventional CSLA. The brief is structured as follow. Section I deals with Literature Survey. Section II (a), (b) presents the detailed structure and design of Prior Work of Normal CSLA and Modified CSLA respectively. Proposed Work is explained in Section III. Simulation Result is explained in Section V and Applications in section VI. Finally, the work is concluded in Section VII.

- *Literature Survey*

In the work of R.Jothin and C.Vasanthanayaki IEEE paper on high performance VLSI architectures for image processing applications, follows a different approximation strategy for designing carry select adder. This design approach reduces the number of gates in full adders. Minimum error tolerances are obtained by conventional full adder logic in the accurate part in order to increase the accuracy at the most significant level. The error tolerant adder is designed using approximate full adder cells with reduced complexity at the gate level in the accurate part. In the proposed approximation method, a potential solution for all range of input operands to get the high accuracy resolution image outputs for the image processing applications. Even by sacrificing an average accuracy more than 30% and minimum accuracy level of 50% are capable of attaining an improvement in both the power consumption as well as speed and area efficient performance.

In the work of K.Mariya Priyadarshini[2], Design of Area and Speed Efficient Carry Select Adder Using Fast Adders are the most important design objectives in integrated circuits. Among all the adders discussed CSA provides a good compromise between cost and performance. As, Conventional CSA is still area consuming due to dual RCA structures, modifications are done at gate level to reduce area. Modified CSA is designed using fast adders like CLA to increase the speed of operation. In this paper the presented Modified CSA are made between different adders in terms of logic levels and delay. The proposed full adders show good performance and among the proposed CSA, show much optimized results.

In the work of Peter Varman [3], High Performance Reliable Variable Latency Carry Select Addition. Speculative adders have attracted strong interest for reducing critical path delays to sub-logarithmic delays by exploiting the trade-offs between reliability and performance. Speculative adders also find use in the design of reliable variable latency adders, which combine speculation with error correction to achieve high performance for low area overhead over traditional adders.

II. PRIOR WORK

A. Normal Carry Select Adder

CSLA use multiple narrow adders to create fast wide adders. A CSLA breaks the addition problem into smaller groups. It is one of the fast types of adder. The adder consists of two independent units. Each unit implements the addition operation in parallel. One way to speed up the addition into several smaller groups, with each having N-bit, say 8-bit groups and then for each group four additions are performed in parallel, one assume carry in is‟ 0‟ (CIN=0) and the other assuming the carry in as “1‟ (CIN=1) .when the carry in is

ISSN No:-2456-2165

eventually known the correct sum is simply selected through a N-bit using 2-to-1 mux. The adder based on this approach is known as carry select adder (CSLA).The application CSLA is used in data processing processor to perform fast arithmetic function.

The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known.

The logical representations and truth table for normal carry select adder is shown in the figure 1 and Table 1 respectively. The number of bits in each carry select block can be uniform, or variable. When variable, the block size should have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The delay is derived from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of MUX delays.

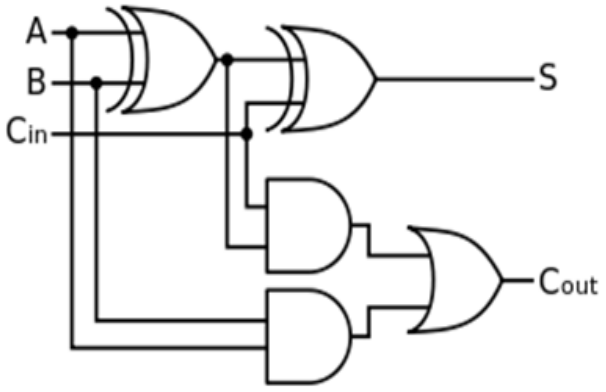

Fig 1:- Design of FA in Normal CSLA

Inputs			Outputs	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Truth table of Normal CSLA

B. Modified Carry Select Adder

In Modified CSLA, a small change is made in construction level. By this change the adder formed is with less number of gates, but produce same output. The modified design is made by just complimenting the carry output. This complimented carry output is accepted as the Sum output. This strategy is simply operating with less Area, Power, and Delay. Modified Full adder logic has 2 errors in sum output and no error in carry output, where all the input bits are either '0's or '1's. Whereas for all other sum and carry values, there is no change in outputs. In this modified design, modified logic of full adder is applied for each block of Ripple Carry Adder. When the modification is applied, only the two combinations (000 or 111) of inputs result in error, all the remaining combinations are correct. The logical representation and truth table of Modified CSLA is shown in the figure 2 and Table 2 respectively. For the Modified CSLA, when all the inputs are 1 then sum is an error (i.e., instead of 1 sum is 0) and when all the inputs are 0 then sum is an error (i.e., instead of 0 sum is 1). The Modified CSLA has 228 gates which are considerably less than conventional carry select adder.

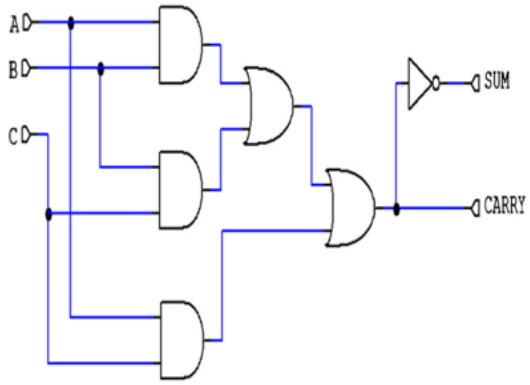

Fig 2:- Design of FA in Modified CSLA

Inputs			Outputs	
A	B	C	Sum	Carry
0	0	0	1(Error)	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	0(Error)	1

Table 2: Truth table of Modified CSLA

ISSN No:-2456-2165

III. PROPOSED WORK

As name suggests, Combinational CSLA is designed with the integration of both Normal CSLA and Modified CSLA. The Proposed system is implemented as follows. In 16 bit Combinational CSLA, the MSB part is constructed with Normal CSLA and LSB is constructed with Modified CSLA. While combining both designs in single system, the efficiency of the system gets improved. This design provides a perfect output for image processing. The motivation for using such devices is the related increase in effective yield, and hence lower cost parts.

The dividing strategy is chosen to design proposed Combinational CSLA with area efficiency and minimum acceptable accuracy to be 99 %. Having considered the above, the 16 bit adder is divided by 8 bit in to the Normal CSLA and 8 bit in to the Modified CSLA. If Normal CSLA has less than 8 bit, the minimum acceptable accuracy and the acceptance probability will be decreased. If Normal CSLA has more than 8 bit, the minimum acceptable accuracy and the acceptance probability will be 99 % and area will be inefficient. The addition of the higher order bits (Normal CSLA) of the input operands is performed from LSB to MSB and normal addition method is applied.

IV. EXPERIMENTAL RESULTS

- *Simulation Tools Used*

The Simulation tools used here are ISE design suite 14.7 and MATLAB with Xilinx. The Verilog coding for design of Normal CSLA, Modified CSLA and Combinational CSLA are developed and executed in ISE Design suite 14.7. The Internal Structure of the designed CSLA is obtained. In MATLAB, Xilinx System Generator is embedded with it. The programs which are executed in ISE platforms are then fed to the black box in present in MATLAB. The image processing boxes are compactly connected with Black box. The input images are provided and they are simulated as per the coding dumped in black box. The simulation result is shown in Figure 4. Furthermore, the simulated results are then verified by using FPGA-Spartan 6 hardware. The hardware output is obtained by Generating JTAG in MATLAB. The MATLAB block with JTAG is shown in Figure 3. This JTAG is then provided with same input images of 256*256 pixels. The Hardware output of Conventional CSLA is shown in Figure 5.

V. MATLAB SIMULATION BLOCK

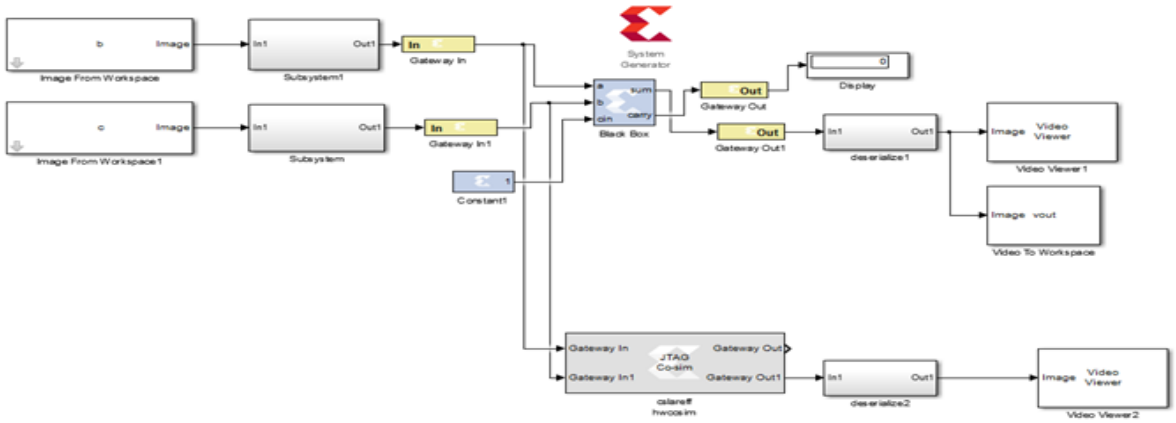

Fig 3:- MATLAB block with JTAG

ISSN No:-2456-2165

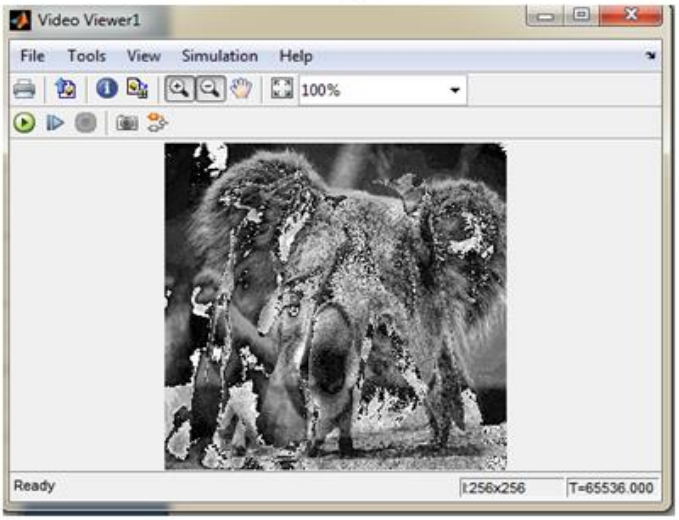

Figure 4: Simulation output of Conventional CSLA.

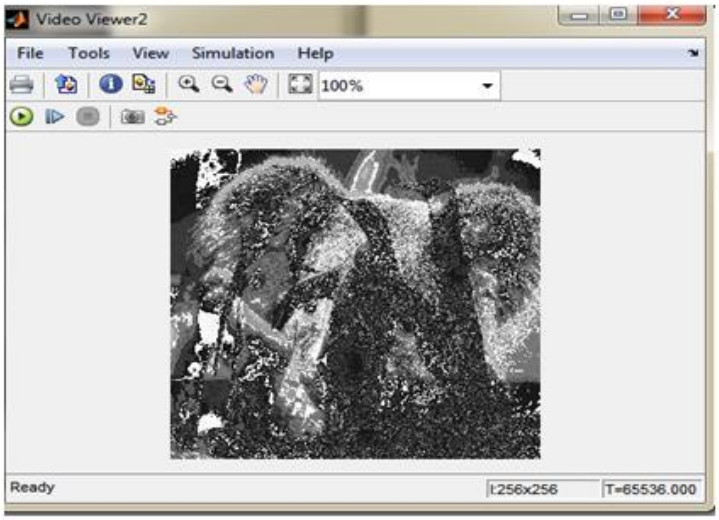

Figure 5: Output of Conventional CSLA in FPG Spartan 6

VI. CONCLUSION

In Overall, concluded that the adder we developed is more efficient in the sense of accuracy, power consumption, time delay on comparison with the Normal CSLA and Modified CSLA that already exist. It also occupies very less area and number of gates also progressively reduced. This proposed Combinational CSLA can be accommodated for high pixel images for more accuracy in industrial applications. For all possible 2^16 input combinations, performance analysis is done and the average error computed is less than 1 %. The error of the proposed adder can be reduced by analyzing the relation between the input bit patterns and approximation logic.

REFERENCES

[1]. R.Jothin and C. Vasanthanayaki IEEE paper on "High performance VLSI architectures for image processing applications".
[2]. Gupta V, Mohapatra D, Park SP, Raghunathan A, Roy K (2011) "IMPACT: imprecise adders for low-power approximate computing".
[3]. He Y, Chang CH, Gu J (2005) "An area efficient 64-bit square root carry-select adder for low power applications".
[4]. Jayanthi AN, Ravichandran CS (2012) "Design of error tolerant adder".
[5]. V Muralidharan, M Jagadeeswari (2012) "An enhanced Carry elimination adder for low power VLSI applications".