ISSN No:-2456-2165

Popular Case Studies of Various VLSI Test Scan Architectures

Madhura.R
Asst Professor, ECE dept
DSCE, Bangalore

Ravi Shankar J
Co-guide &Advisor
Govt. of Karnataka
Bengaluru, karnataka

Dr. Shanthi Prasad .M.J
Professor, ECE Dept.
KSIT, Bangalore

Abstract:- In today's world, good testing leads to better quality products and total customer satisfaction. This technical survey paper summarizes various important research works in low power VLSI test scan architecture.

Keywords:- *Low Power, VLSI Test, Scan Architecture, FPGA Test-bed.*

I. INTRODUCTION

This technical survey paper summarizes, various important research work in low power VLSI test scan architecture like-3-Weight Weighted Random BIST, Cyclic Redundancy Check Message Authentication Code architecture, Low power Illinois scan Architecture, Scan Forest based BIST, Scan Architecture for pseudorandom testing and deterministic BIST, 2-Dimensional pixel-block scan architecture, Low power scan architecture, DFT architecture for Low Power scan-based BIST, Weighted pseudorandom test generator for scan tree based low power BIST.

II. LOW POWER TEST SCAN ARCHITECTURE

A. Case Study-1 (CS-1)

During BIST, there are two important and critical parameters to be taken into consideration. While design and implementation of scan based BIST- 1) no of switching 2) length of test sequence. Special efforts must be put to reduce the switching activity in CUT else during BIST CUT may get damaged.

This author has proposed a BIST in figure 1 with LT-RTPG-easy to detect faults and WR-BIST TPG is used to detect random pattern resistant faults. This BIST architecture provides 100% fault coverage with less hardware overhead. Long term sequence provides high fault coverage and these pseudorandom test patterns have large number of pattern resistant faults. The overall objective is to reduce enormous switching activity.

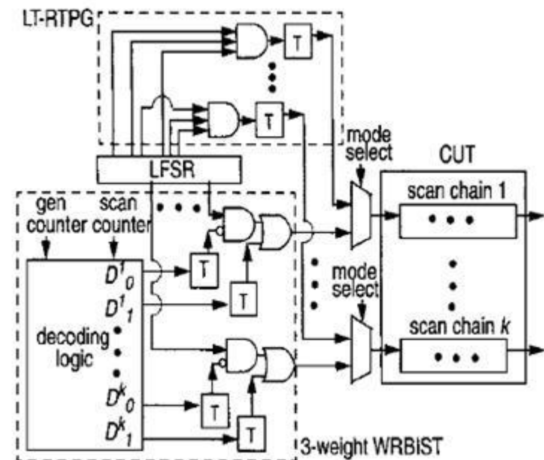

Fig 1:- 3-Weight Weighted Random BIST

B. CS-2

This paper explains a secured scan based DFT which maintains high test quality. There are two types of tests-factory test in device production environment and operation test during normal using of device. Boundary scan chain is most accepted testing procedure for digital circuits and this testing covers the whole life cycle of device (covers factory and operation test) and requires very simple hardware Cryptographic hardware won't allow BIST and boundary scan type of testing as the test port will be locked by the manufacturer to provide security to the device (to prevent accidental data corruption and intrusion or copying the design to provide design protection).

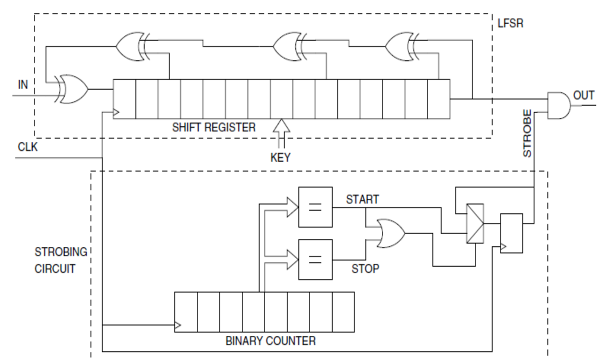

Fig 2:- CRCMAC Architecture

ISSN No:-2456-2165

This author has proposed CRCMAC architecture in figure 2 which consists of LFSR with key inputs and strobing circuit which has advantages like streamed I/O operation, simple hardware and high speed operation.

C. CS-3

This author has proposed a new architecture in figure 3 with two objectives called LPILS which will together achieve 1) low power (47%) 2) reduced volume of test data (10 times) as compared to normal test scan. The other important feature of this is 1) reduced hardware architecture 2) Independence from ATPG pattern. LPILS architecture achieves 30% power reduction in switching, broadcast scan mode without repeated synthesis of clock tree and without any dependency on ATPG.

This architecture with MTC algorithm can provide up to 47% of power reduction. MTC filling provides higher ratio of test compression to reduce volume of test data which will eventually reduce the memory/ hardware overhead.

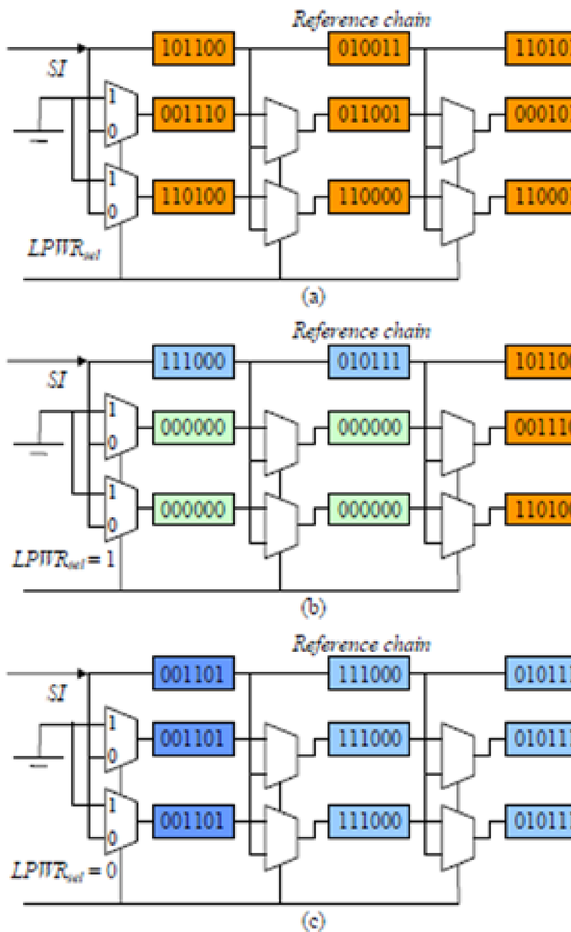

Fig 3:- Low power Illinois scan Architecture

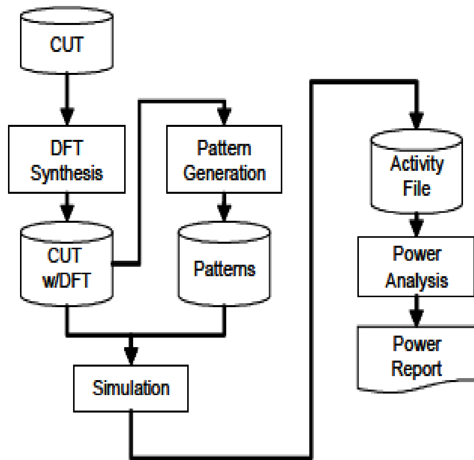

Fig 4:- Power estimation flow

D. CS-4

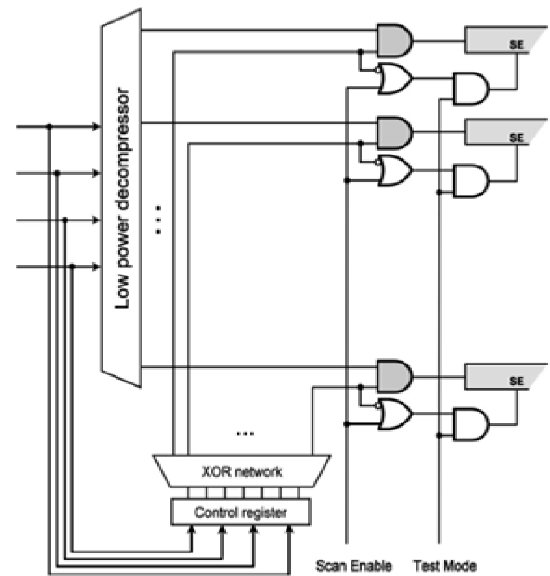

Fig 5:- Low power scan architecture

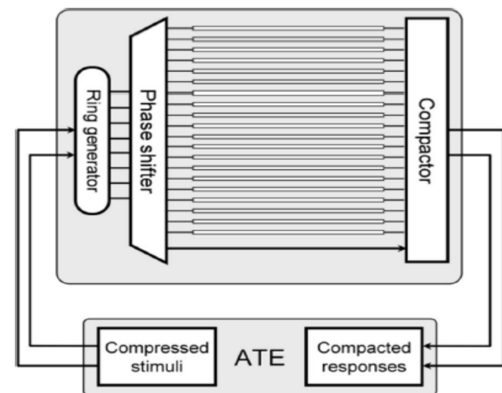

Fig 6:- EDT architecture

In this paper, the author proposes a novel low power test compression technique. Scan test has following embedded deterministic test (EDT) phases- 1) loading 2) capture 3) unloading. On chip continuous flow decompressor is used to reduce the no of switching in the above 3 scan phases. A power aware scan controller is used to reduce the toggling of decompressed test pattern into scan chains. Reduced switching activity lowers the power consumption. Here the flexible frame work is designed with modular decompressor and compactors. The author has claimed that the switching activity is reduced by 97% for scan loading, 93% for unloading and 85% for capture phase. Acceleration of scan shifting leads to short test application time. Design portioning also results in reduced test time leading to power reduction and temperature, else it will lead to overheating and degradation of readability.

C. CS-5

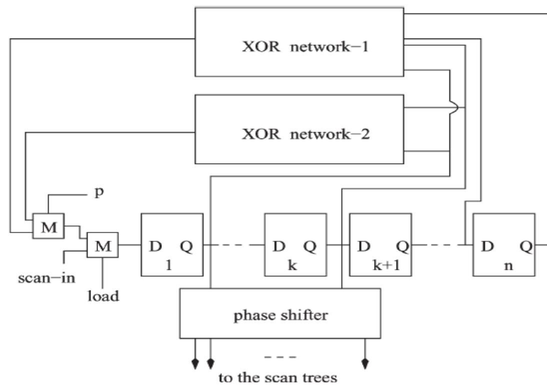

Fig. 3. LFSR design for the two phases.

Fig 7:- LFSR Design for the two phases

In this paper the author has proposed a new technique of scan forest based BIST with weighed scan enable signals. This technique reduces the volume of test data. Here the BIST works on two phases 1) pseudorandom 2) deterministic phase. In a scan based BIST, the test length is usually decided by hard to detect faults. BIST has two important parameters- 1) data compression 2) data compaction. The most popular techniques for reduction of test length are 1) weighted random testing 2) test point insertion 3) deterministic scan based BIST. Scan forest consists of large no of scan trees. Test application time also affects the overall performance of the BIST. In pseudorandom phase- weighted scan enable signals are used for test application. In deterministic BIST- scan forest is reconfigured into single scan tree. Size of LFSR required to encode all deterministic test vector is equal to maximum no of care bits.

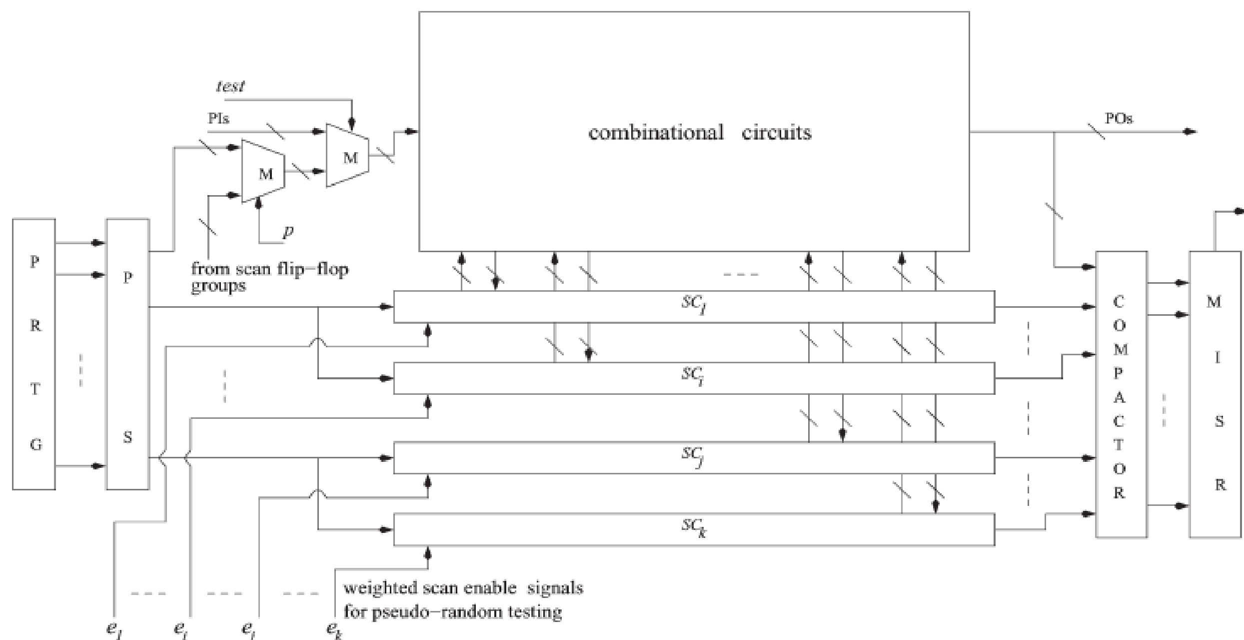

Fig 8:- Scan Forest based BIST

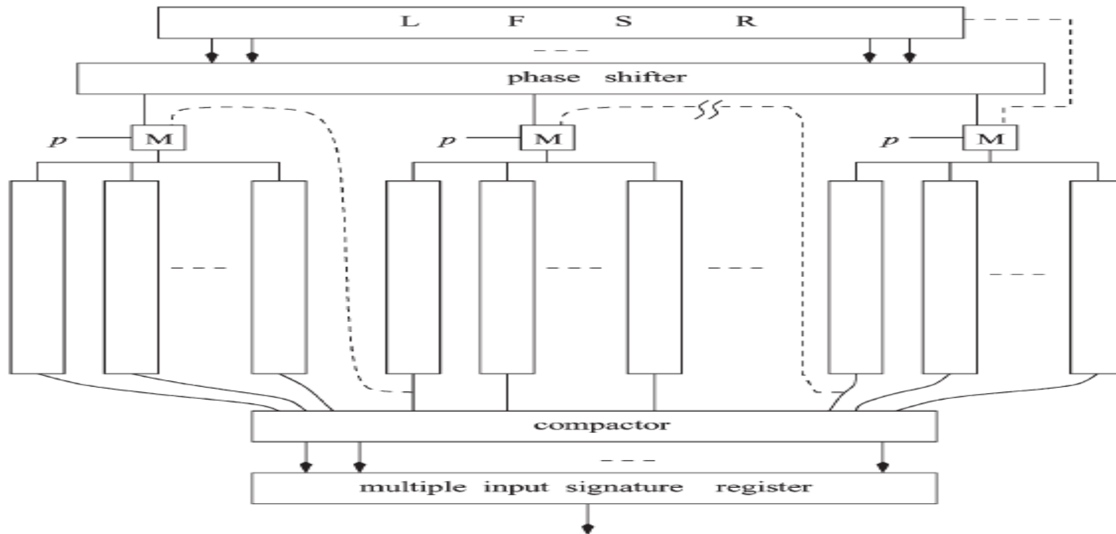

Fig 9:- Scan Architecture for pseudorandom testing and deterministic BIST

F. CS-6

In this paper, the author has proposed a new technique as in figure 11 and 12 for low power BIST based on weight pseudorandom test pattern and reseeding. This author has developed two algorithms to achieve low power in two phases-

- Disabling partial scan chains in PTP phase
- LFSR length is reduced to alter the DFT structure in BIST phase

The novel low power reseeding scheme proposed reduces on chip data thereby reducing the hardware overhead, test complexity and achieve low power.

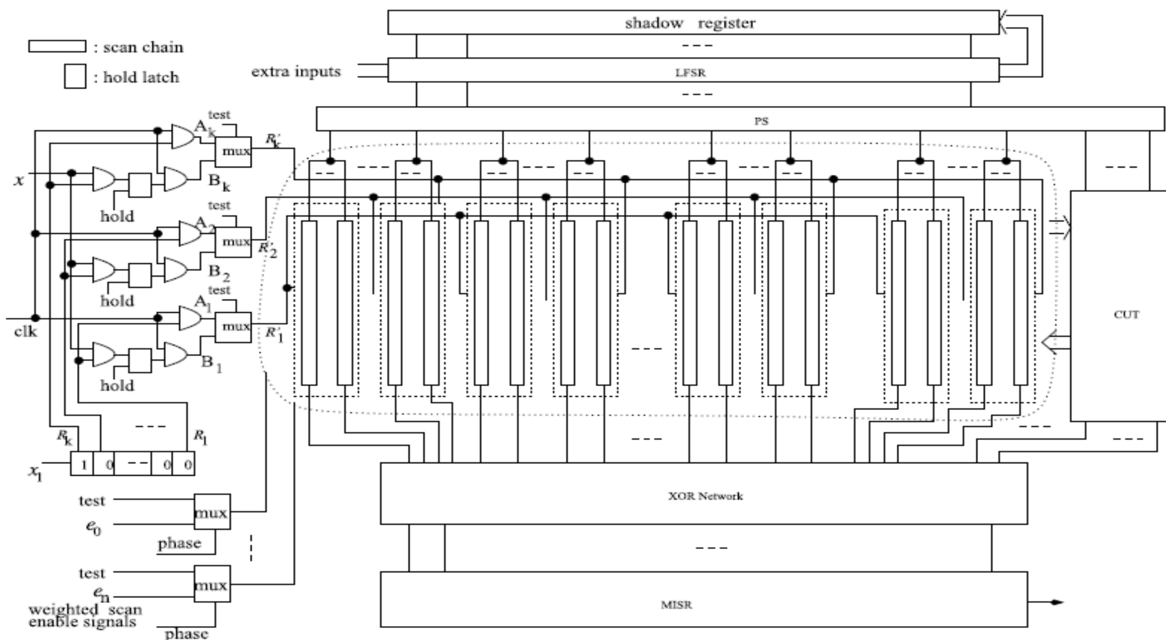

Fig 10:- DFT architecture for Low Power scan-based BIST

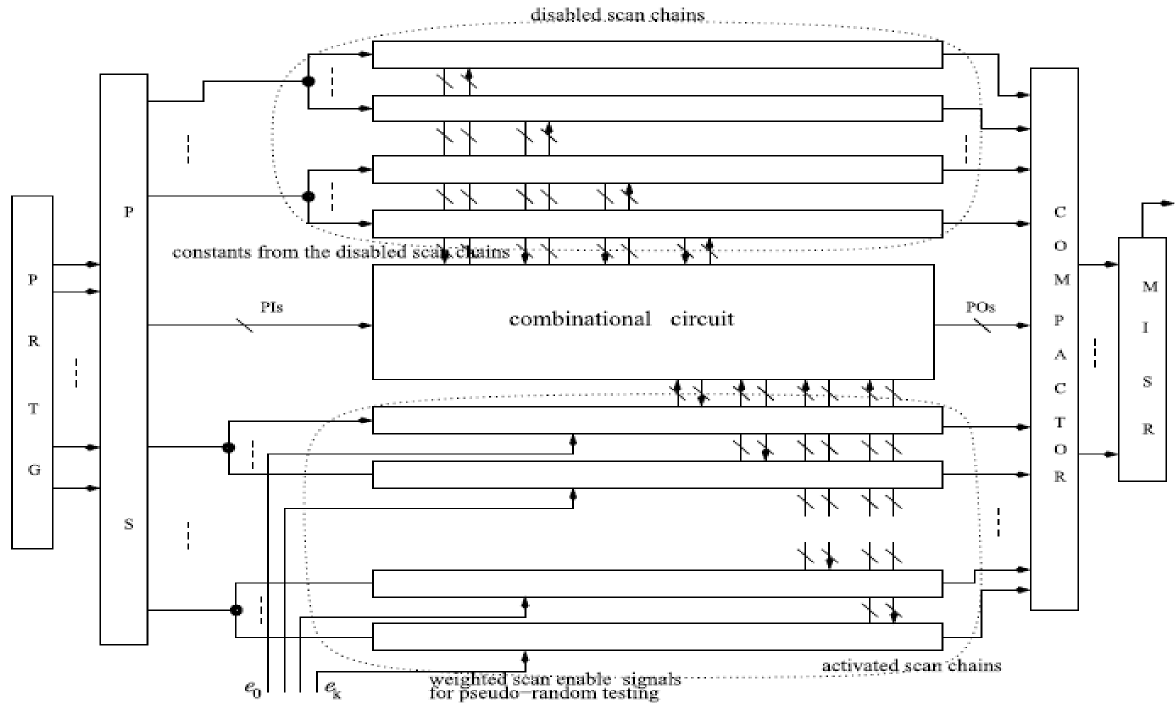

Fig 11:- Weighted pseudorandom test generator for scan tree based low power BIST

III. CONCLUSION

In this technical survey paper, several Researchers have proposed many VLSI Test Scan architecture having their own merits & limitations. But, these architectures need to be studied further, understood & experimented on a common FPGA test bed. This is one of the major objectives of my ongoing Research, wherein I am attempting to arrive at a novel UNIVERSAL VLSI TEST SCAN ARCHITECTURE, designed & simulated using Verilog HDL & later Proto type tested on Xilinx FPGA.

REFERENCES

[1]. Seongmoon Wang, “Generation of Low Power Dissipation and High Fault Coverage Patterns for Scan-Based BIST**”** ITC International Test Conference.

[2]. MarcinGomulkiewicz, MaciejNikodem, TadeuszTomczak, “Low-cost and Universal Secure Scan: a Design-for-Test Architecture for Crypto Chips” Proceedings of the International Conference on Dependability of Computer Systems.

[3]. Anshuman Chandra, Felix Ng and RohitKapur,“Low Power Illinois Scan Architecture for Simultaneous Power and Test Data Volume Reduction”

[4]. DariuszCzysz, Mark Kassab, Xijiang Lin, GrzegorzMrugalski, JanuszRajski, and Jerzy Tyszer, “Low-Power Scan Operation in Test Compression Environment” IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 28, No. 11, November 2009.

[5]. Dong Xiang, Yang Zhao, KrishnenduChakrabarty, and Hideo Fujiwara “A Reconfigurable Scan Architecture With Weighted Scan-Enable Signals for Deterministic BIST” IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 27, No. 6, June 2008.

[6]. “Low-Power Scan-Based Built-In Self-Test Based on Weighted Pseudorandom Test PatternGeneration and Reseeding” Dong Xiang, Xiaoqing Wen, and Laung-TerngWang,IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 25, No. 3, March 2017.