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Design and Implementation of Transient Secure Encoder and Decoder

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Abstract:- In this project, the aim is to protect the circuit from transient errors due to increase in rate of transient errors in logic circuits. This is done by designing a transient secure encoder and decoder using Verilog HDL. Project is divided into two parts. First is error detection module, which is used to detect error in the encoder circuit. if there is any error in the code word the encoder circuit does not allow the code word to pass further. RE-DO operation takes place and the new input is taken for the code word to pass through encoder circuit. Second part is the majority logic decoding in which corrector is used to correct the codes if there is any transient generated during decoding the code word. The result demonstrate that the method is effective for EG-LDPC codes which are one step majority logic decodable. This proposed method has reduced decoding time by detecting whether the code word has error in the first iteration of majority logic decoding and if the code is error free the decoding stops without completing the rest of the iterations. In this way decoding time will greatly be reduced. The design is implemented in board and performed coding in Verilog hardware description language and simulating in Xilinx ISE Simulator.

Keywords:- *Verilog HDL, EG-LDPC codes, majority logic decoding, Xilinx ISE simulator.*

I. INTRODUCTION

Error correcting codes are used to protect the circuit from transient errors. These errors does not damage the circuit but corrupts the data code word. Since devices become larger so more powerful codes are required. More advance has been proposed which can correct larger number of errors and require complex decoders. To avoid high decoding complexity one step majority logic decodable codes are proposed which can be implemented serially with very simple circuitry but require large decoding time. In order to reduce decoding time Euclidean geometry low density Parity check (EG-LDPC) codes are used. This method was proposed to accelerate the serial implementation of majority logic decoding. In this method the first iteration of majority logic decoding is to detect whether there is a error in the code word if the code word is error free then the decoding can be stopped without completing the rest of the iterations which results in reducing the decoding time.

We use transient secure detector to check the output of encoder and decoder circuitry and if there is any error in either of these units the units starts to do re-do operation to generate the correct output code word. Using this detect and repeat technique we can correct transients in the encoder or decoder output and provide a error or transient free supporting circuitry.

II. BASIC BLOCK DIAGRAM

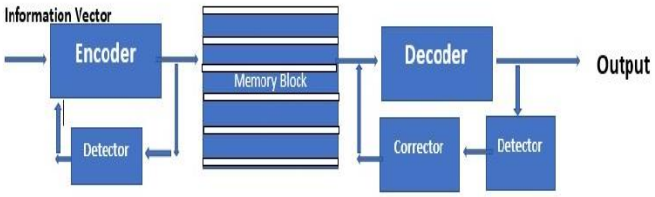

Fig 1:- Basic Block Diagram

III. PROPOSED CIRCUIT DIAGRAM OF MAJORITY LOGIC DECODER

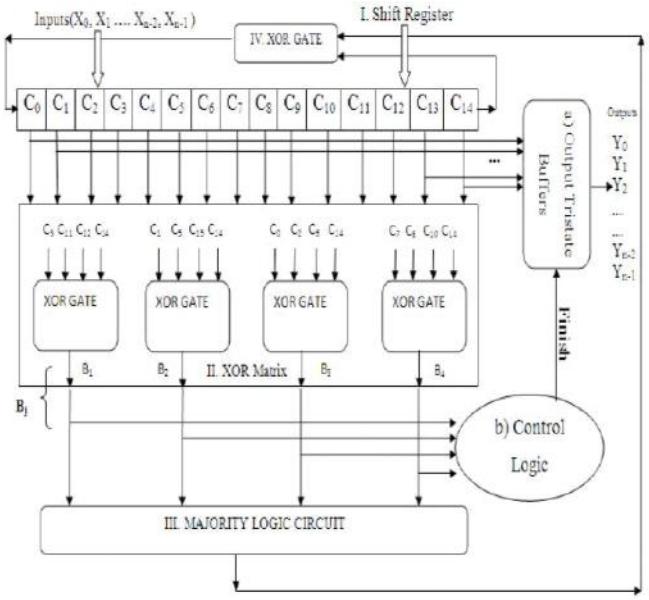

Fig 2:- Proposed circuit diagram of Majority Logic Decoder

IV. DESCRIPTION OF MAJORITY LOGIC DECODER

The majority logic decoder consists of five main components

- One cyclic shift register
- One Xor matrix

- Extra control logic unit
- One majority logic gate
- One Xor gate for correcting the bits

The main steps involved during decoding are :-

- The encoded information is stacked into the cyclic shift register and afterward registering the direct entireties of the encoded bits utilizing XOR matrix.
- Control Logic takes the contribution from XOR matrix and watches that whether the Matrix yield is giving outcome „0000" in first „3" clock cycles or not.
- Majority logic circuit calculates the majority values of the direct entireties of bits which are processed in stage 1.
- XOR gate is used to correct the bit when the ML gate output is 1.

The design flow for majority logic decoding is shown below:

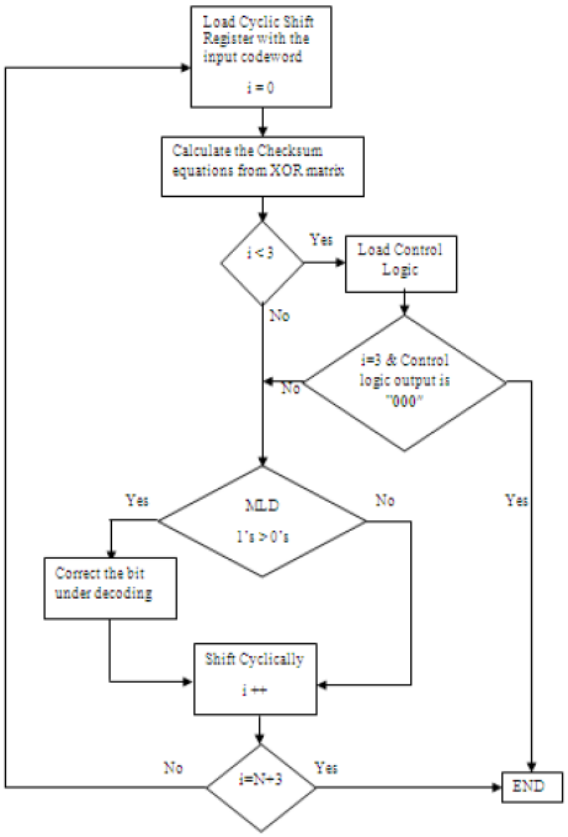

Fig 3:- Description of Majority Logic Decoder

With the help of control logic check the first three cycles to check the output of the XOR matrix is 0000 or not. If the output is zero then the encoded data will be sent to the output of the decoder and only 2 extra clock cycles will be used to load the input and give output. If the encoded data is not zero then the decoding process will take place for another 15 clock cycles it take two extra cycles for taking input and giving output.

V. ADVANTAGES

- Low power consumption.
- Take less decoding time.
- Corrects multiple error at a certain time.

VI. DISADVATAGES

- If the code word has more than four bit error then MLDD can-not correct the code word suitably.

VII. SIMULATION RESULTS

Simulation results of Transient secure encoder and decoder are shown below:

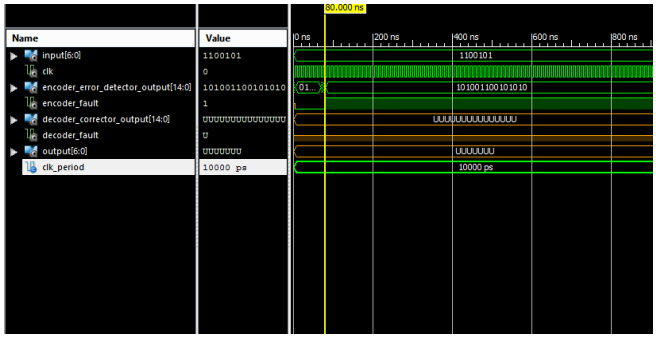

Fig 4:- Encoder Fault

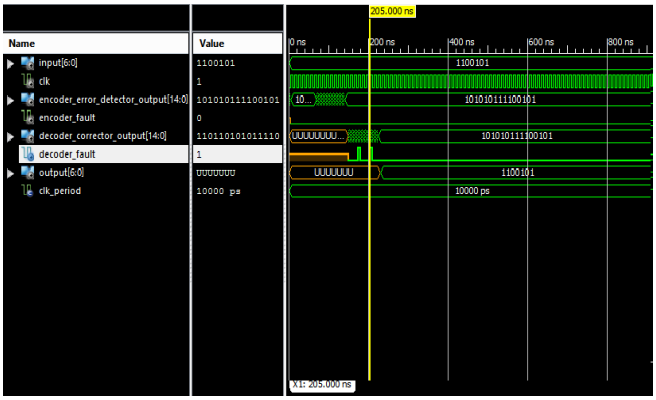

Fig 5:- Decoder Fault

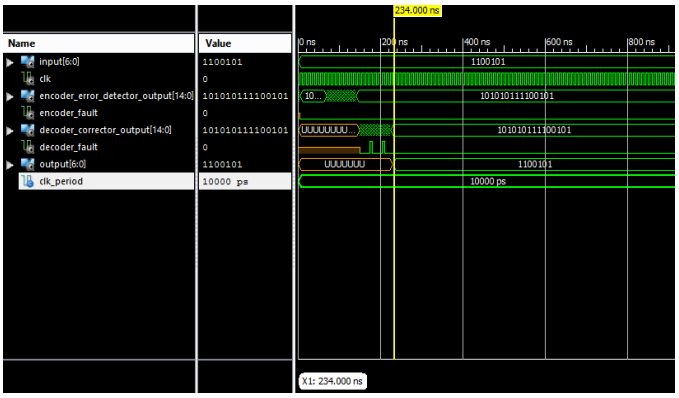

Fig 6:- Final Output

VIII. CONCLUSION

In this concise, the first iterations of serial one step Majority Logic Decoding of EG-LDPC codes has been studied. The goal was to lessen the decoding time by halting the coding process when no errors are distinguished. The result show that all tested combinations of errors affecting up to four bits are detected in the first three iterations of decoding.

IX. FUTURE SCOPE

The future scope for the project is to eliminate the silent error corruption which occurs when we have more than four bit error in the code word. In such cases MLDD is not perfectly suitable. To reduce such fault one more detection logic can be implemented after the completion of 15 iteration.

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