Implementation of Fault Tolerant FIR Filter

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Abstract:- This is the matter-of-fact that communication system is never free from noise. Therefore it is a requirement for every communication systems to have suitable means to recognize and correct the errors in the information which is received over communication channels. Digital parallel FIR(Finite Impulse Response) filters are very widely used in DSP application. To get the noise free system, there is a need to implement some techniques to achievethe fault tolerancein parallel filters. In this paper , the idea of implementing FIR Filter with the range of 1 bit to 6-bit Fault tolerance using BCH codes is addressed.This idea is very much effective in fault tolerance as well as comparatively less cost. Both features are evaluated for FPGA implementation.

Keywords:- *Error Correcting Codes (ECC); Finite Impulse Response (FIR) filter; Very Large Scale Integration (VLSI);HDL; FPGA.*

I. INTRODUCTION

In today's digital world, there are numerous DSP applications in different-different fields such as automotive, medical and space applications. These applications create the great demand of high performance and low power Digital circuits. But here the reliability becomes critical. So there is a need to achieve the fault tolerance in digital applications.There are various effective ideas to implement error-free systems and give the reliable performance. In this paper, idea of removing errors is toadd redundancy bits at the logic or system level. These redundancy bits are addedin order to ensure that they do not affect the system functionality. Here, the designing of digital parallel FIR filter and various Error Correcting Coding schemes are discussed. In traditional ECC scheme, inputs and outputs of filters are bits but here inputs and outputs of filters are not bits but the numbers.This provides the more efficient protection.Here number of redundant filters are independent of the number of digital filters. The reduced number of redundant filters reduces the implementation cost.The proposed scheme is first described and then illustrated with two casestudies.

II. OVERVIEW-ERROR CORRECTING CODES(ECC)

It is necessary for noise free communication systems,to implement some ECC for the detection and correction of errors in the information which is received over communication channels. ECC are binary codes that detect and correct the errors that occurred in transmission.Error correcting codes have been successfully implemented in both wired and wireless communication to offer error-free transmission. Basically ECC are categorized in two types-

1. Block Codes
2. Convolution Codes

Block code uses soft decision decoding algorithm for its implementation. Hamming codes, BCH (Bose Chaudhary Hocquenghem) codes, RS (Reed Solomon) codes and LDPC (Low Density Parity Check) codes are frequently used codes for ECC nowadays. Hamming codes are linear error correcting codes that can detect 2-bit error and can correct up to 1-bit error. These codes can achieve the highest possible rate for codes with their block length and minimum distance 3.LDPC codes are used in error correction with the help of sparse bi-parity graph. All these codes aredifferent from each other in their application mannerand implementation.all codes are good in the correction of one or two bits error but if we talk about multiple bit errors BCH code is perfect in the implementation.

Error correction can be applied in two different ways:

- *Automatic Repeat Request (ARQ):-* It is also called as backward error correction. In this an error detection scheme is combined with requests for retransmission of data which is affected by the error. Eachreceiveddata is checked using the error detection code which is applied. If the check shows failure, retransmission of the data is requested. This may be done repeatedly until the data can be verified.
- *Forward Error Correction (FEC):-* The sender encodes the data using an error-correcting code (ECC) before transmission. The (additional data) redundancy isadded to the code which is further used by the receiver to recover the original information.

In the current paper, Forward Error correction coding -BCH coding technique is used.BCH codes are cyclic codes that are designed on the basis of Galois fields.

The BCH codes are used to be defined by the code size *n* and the number of errors(t)which has to be corrected .

Block length can be defined by
$n = 2m - 1$, where m is any positive integer.
Number of information bits is k where
$k \geq n-m*t$
Minimum distance is dmin where
$dmin \geq 2t + 1$.

The generator polynomial of the code is specified in terms of its roots over the Galois field GF (2^m).

III. DIGITAL FIR FILTER

A discrete time filter can be described with the following equation:

$$y[n] = \sum_{i=0}^{\infty} x[n-l].h[l]$$

Where$x[n]$ is the input signal, $y[n]$ is the output, and $h[l]$ is theimpulse response of the filter. For a FIR FILTER the impulse response h[l] should be nonzero, only for a finite number of samples.

The memory elements of an FIR filter is related to the input sequence of FIR filter. this relationship between them is used to detect errors and to protect the filters residue number systems and arithmetic codes are used. This scheme works only for correction of one redundant module of FIR filter. In all these techniques which are described previously, the protection of a single filter is concerned. In the case of filter banks where several filters operate in parallel, there is a need of protection of more than one filter. For those modern communication systems, the protection of the more filters can be addressed at a higher level by considering the Digital filters as the block to be protected. This idea was explored in where two Digital filters with the same response that processed different input signals were considered. It was shown that with only one redundant copy, single error correction can be implemented. Therefore a significant cost reduction compared with another ECC scheme like TMR was obtained. In this brief, a general scheme to protect Digital filters is presented. As in Digital filters with the same response that process different input signals are considered. The new approach is based on the application of error correction codes (ECCs) using each of the filter outputs as the equivalent of a bit.This idea is used in ECC codeword. This is a generalization of the scheme presented which enables more efficient implementations when the number of Digital filters is large. The scheme can also be used to provide more powerful protection using advanced ECCs that can correct failures in multiples modules.

IV. PROPOSED BLOCK DIAGRAM

The figure 1shows the proposed structure for fault tolerant FIR filter. This figure gives the clear overview of low level overview of proposed fault tolerant FIR filter. FIR filter inputs are mixed with some error bits and fed to the designed fault tolerant FIR filter. Here FIR filter is designed with the help of MATLAB and HDLs. Error detection and correction is done by HDL using BCH coding techniques. The proposed structure gives the error free output and one notification signal which is high when the number of errors are more than the specified criteria.

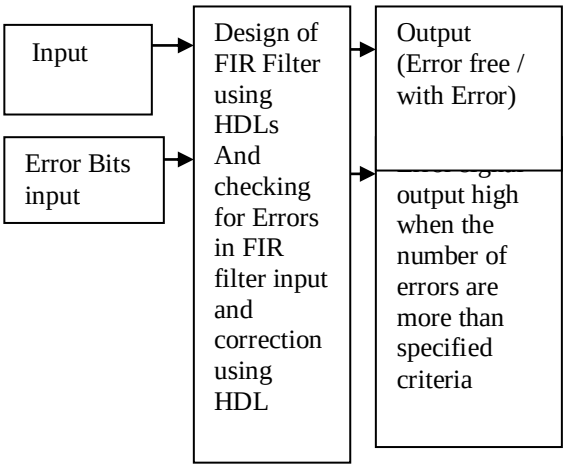

Fig 1:- Proposed Structure for Fault tolerant FIR Filter

V. SYNTHESIS & SIMULATION RESULTS

This section shows the various results obtained from the XILINX ISE Tool. The figure 2 shows the RTL view of our designed circuit i.e. Fault tolerant FIR Filter. As shown in the figure there are two inputs named as A , and error . The input A denotes the original message to be filter through the FIR filtration. While error signal are for stimulating the various number of errors.

Fig 2:- RTLview for Fault Tolerant FIR

The figure 2 shows only the input output ports which can be used as a physical interface for real world implementation.

The figures 3, 4 shows the cumulative result for the fault tolerant fir filter with different input conditions.

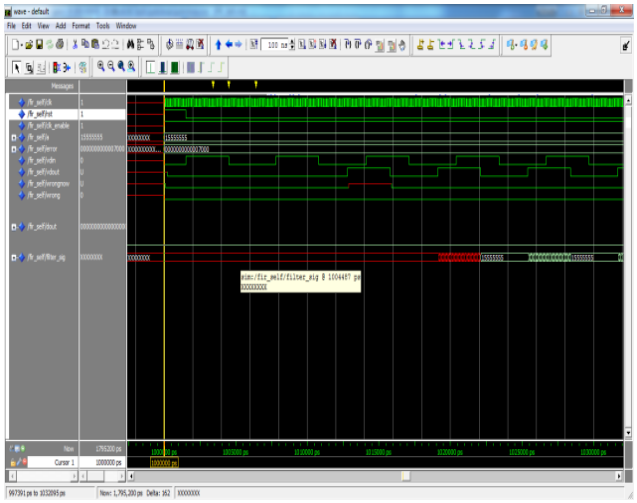

Fig 3:- Simulation Result with initial Conditions.

The figure3 shows the simulation results with initial conditions i.e. RST='1'. For initialization of all the registers, signals into its original states/values.

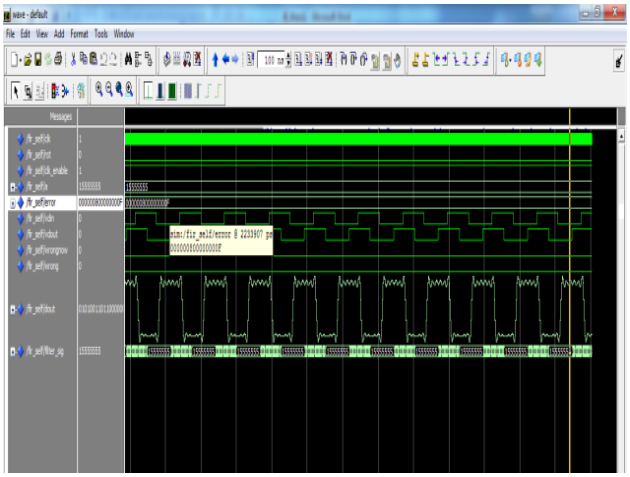

Fig 4:- Simulation result for 5 bit error

Figure4 shows the result with stimulation of 5 bit error valuesthrough error signal. And we can easily observe that there is not a slight change in the output waveform.

VI. CONCLUSION

Basically there are five primary criteria: area, speed, energy dissipation per bit, latency and error performance gap from the Shannon limit that must be considered in a BCH decoder design based on the application requirement. Current paper has focused on the decoding algorithm, code design and VLSI implementation to meet the required criterion e.g. Less error, hardware reconfigurability, very high-throughput and high efficiency. In this paper efficient coding scheme is used for fault-tolerant FIR Filter. FIR Filters can also be made using different structures i.e. Parallel, Serial but each design has the common feature i.e. the multiplication and shifting process which demands lots of hardware area. So it is a future challenge to reduce the hardware area by using. Distributed Arithmetic structure. The Synthesis has been done by XILINX Synthesis Tool and the simulation has been carried out by Xilinx ISIM and Modelsim.

REFERENCES

[1]. SashankShekharPujari , PrangyaParamitaMuduli , Am ruta Panda , RashmitaBadhai , Sofia Nayak , YougajyotySahoo ,Design and implementation of FIR filter using on board ADC -DAC & FPGA, IEEE- Information Communication and Embedded Systems (ICICES), 2014.

[2]. A. Sibille, C. Oestges and A. Zanella, MIMO: From Theory to Implementation, New York, NY,USA: Academic, 2010.

[3]. Yathiraj H U, Mahasiddayya R Hiremath,"Implementation of BCH Code (n, k) Encoder and Decoder for Multiple Error Correction Control",International Journal of Computer Science and Mobile Applications, Vol.2 Issue. 5, May- 2014.

[4]. M. Nicolaidis, "Design for soft error mitigation," IEEE Trans. Device Mater. Rel., vol. 5, no. 3, pp. 405–418, Sep. 2005.

[5]. C. L. Chen and M. Y. Hsiao, "Error-correcting codes for semiconductor memory applications: A state-of-the-art review," IBM J. Res. Develop.vol. 28, no. 2, pp. 124–134, Mar. 1984.

[6]. A. Reddy and P. Banarjee "Algorithm-based fault detection for signal processing applications," IEEE Trans. Computer, vol. 39, no. 10,pp. 1304– 1308, Oct. 1990.

[7]. T. Hitana and A. K. Deb, "Bridging concurrent and non-concurrent error detection in FIR filters," in Proc. Norchip Conf., 2004, pp. 75–78.

[8]. Takashi Mizuochi ," Recent progress in Forward Error Correction and its interplay with transmission impairments", IEEE Journal of Selected Topics in Quantum Electronics (Volume: 12, Issue: 4, July-Aug. 2006).

[9]. Yu-Chi Tsao and Ken Choi , 2012. "Area- Efficient Parallel FIR Digital Filter Structures for Symmetric Convolutions Based on Fast FIR Algorithm" IEEE transactions on very large scale integration (vlsi) systems, vol. 20, no. 2, feb. 2012.

[10]. Yu-Chi Tsao and Ken Choi , 2011. "Hardware-Efficient Parallel FIR Digital Filter Structures For Symmetric Convolutions "978-1-4244-9474-3/11/$26.00 ©2011 IEEE.