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Wideband Digital Receiver using Halfband Filters for Weather Radars

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Abstract:- This paper describes different challenges related with the design and operation of a multi-channel wideband receiver. Radar signal parameters are measured with high precision and accuracy using wideband digital receiver. For radar data processing the digital Intermediate Frequency (IF) signals are down converted using filters. The paper puts forward the traditional implementation of wideband receiver which should perform subsampling of the input data at Analog to Digital Converter (ADC) level. The major focus of the paper is to design a system compatible for solid-state radars.

Keywords:- *Multi-channel wideband receiver, Digital receiver, IF, ADC, Solid-state radar.*

I. INTRODUCTION

Radar is a contraction of word Radio Detection and Ranging. Radar is a remote sensing technique or an object detection system that detects the presence of any target using radio waves. It also determines the direction, distance and velocity of the object. The basic radar includes a transmitter used for transmitting an electromagnetic waves and a receiver which can be used both as transmitter as well as receiver and a processor. Transmitted electromagnetic waves are reflected back to the receiver which determines the distance and velocity of any object located. These reflected energies are in small portions and is called as an Echo. Different polarizations such as horizontal, vertical, linear and circular are used in radars to detect reflections.

Radar systems have been using digital techniques for a long time. Digital receivers used in radars are highly reliable, processes high speed data and also has programming flexibility. These properties of digital receivers are cause to replace the use of analog receivers. Another advantage of using digital receiver is that the parameter measured by the receiver is highly precisie and accurate. Today's digital receiver comprises of both analog and digital modules. The received Radio Frequency (RF) signal from the antenna is converted by analog module and is translated into IF signals. The signal is later digitized using a digital receiver and processed to provide meaningful information. ADCs must operate at very high sampling speed in order to digitize signals in wideband receiver. High speed digital circuits are used for processing high speed ADC outputs. Two identical analog receiver channels can be replaced by single digital receiver in polarization diversity systems.

II. DIGITAL RECEIVER

The digital receiver designed earlier carried out down conversion of IF signals prior to ADC sampling. However, nowadays increase in the use of Field Programmable Gate Array (FPGA) has simplified the process of down conversion as well as improved digital signal processing techniques on baseband signal. Programmable digital receivers have superseded several analog components thereby reducing the cost and real-estate.

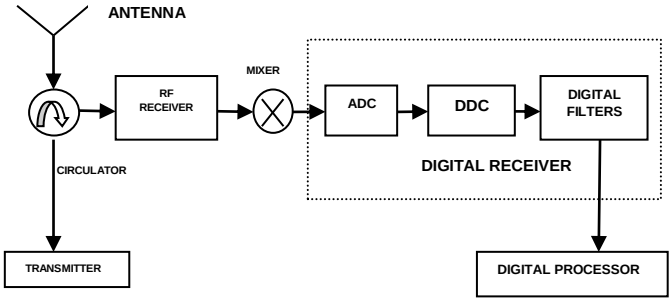

Fig 1:- Block diagram of generic digital receiver in a radar system

A generic digital receiver in a radar system is shown in Fig. 1. A digital receiver consist of an antenna that receives the RF signals that is further provided to three port device known as circulator where, signal entering any port of a circulator is transmitted to the next port in rotation. The modulated RF signal is transmitted to RF receiver block in order to demodulate it. The digital receivers also perform functions such as channel filtering and frequency translation. Two different signals are applied to RF mixer to generate IF signals. For further processing IF signals are digitized by the ADCs used in the digital receiver. A fundamental part of generic digital receiver is Digital Down Converter (DDC). A digitized band limited signal is converted to a lower frequency signals by DDC. The down conversion process is followed by a cascade of digital filters which decimates the received data and also performs anti-aliasing.

A. Digital Down Converter

A DDC converts the band limited signal into a lower frequency signal using lower sampling rate. This may also reduce the subsequent radio stages. The counter component of Digital Up Converter (DUC) is DDC and is therefore, equally important as these components are in the same application systems. The function of DDC is to translate a passband signal to baseband channels for demodulation. The passband signal comprises of one or more RF signal or IF signal. Fig. 2 shows the block diagram of DDC.

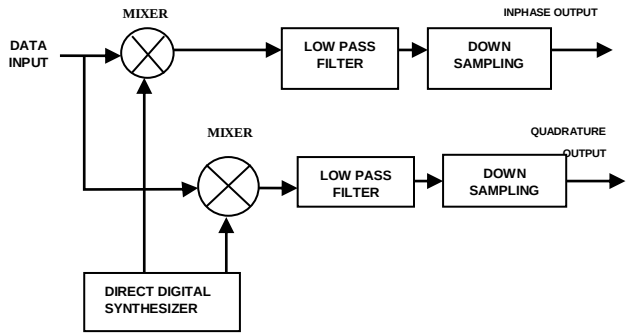

Fig 2:- Block Diagram of Digital Down Converter (DDC)

A Basic DDC consists of three major components a Direct Digital Synthesizer (DDS), a Low Pass Filter (LPF), and a down sampler. ADC sampled output along with the DDS generated output is given to the mixer element. The DDS generates the sinusoidal IF signal. The output obtained from the mixer is filtered using a low pass filter. Low pass filters rejects the sum frequency allowing difference frequency. Further the signal is down sampled using a down sampler.

B. Digital Down Converter with CIC, CFIR and PFIR

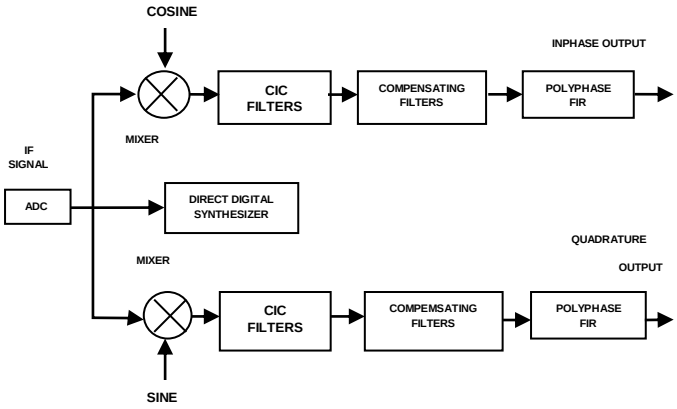

Fig 3:- Block Diagram of DDC with CIC, CFIR and PFIR

Fig. 3 shows block diagram of DDC with Cascaded Integrated Comb filter (CIC), Compensating filter (CFIR) and Polyphase filter (PFIR). Block diagram of DDC consist of cascade of three different filters to perform decimation. DDS present in the DDC block generates arbitrary waveform from fixed frequency signal. Mixer output is achieved by mixing the signal with DDS to shift the signal spectrum from selected carrier frequency to baseband frequency. With the two complementary structures involved CIC can easily perform decimation as well as interpolation. CFIR is cascaded with CIC filters to further eliminate pass band droop. The third stage of decimation is carried out by PFIR obtaining in phase and quadrature phase output.

III. PROPOSED METHODOLOGY

The DDC designed using CIC filters are efficient and does not require any memory for storage of the coefficients. The filter does not use multiplication operation as required in FIR. The major drawback of using CIC filters is the pass band droop. This pass band droop can be eliminated by using CFIR cascaded with CIC filters but it may increase the resource consumed. In order to compensate for this disadvantage, CIC filters are replaced with half band filters.

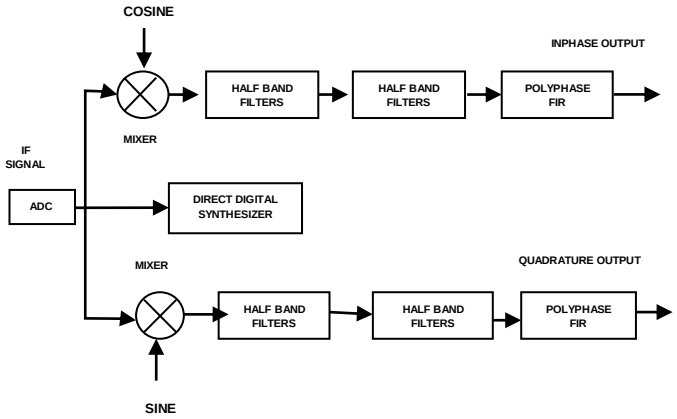

Fig 4:- Block Diagram of DDC with Half band filters

The block diagram of DDC with half band filters is shown in Fig. 4. The three multirate filters are cascaded together in DDC. The first and second stages are decimated by using two half band filters followed by a polyphase decimator. The two half band filters along with decimator decimates three different stages without decreasing dynamic range of digitized signal. Configuring CIC filters as polyphase filters are advantageous as they require fewer multipliers. Half band filters reduce the bandwidth of sampled data by a factor of 2. The concept of DDC is to sample the input signal and to reduce the data using digital techniques.

IV. RESULTS AND ANALYSIS

A. Output of DDC with CIC, CFIR and PFIR Filters

MATLAB code for DDC is written with the filters such as CIC, PFIR and CFIR filters. The time scope and system analyser object enable to analyse the various stages of DDC. Along with real sine and imaginary sine output, NCO output and desired decimated output is generated. Fig. 5 and Fig. 6 show the output of real sine and imaginary sine respectively.

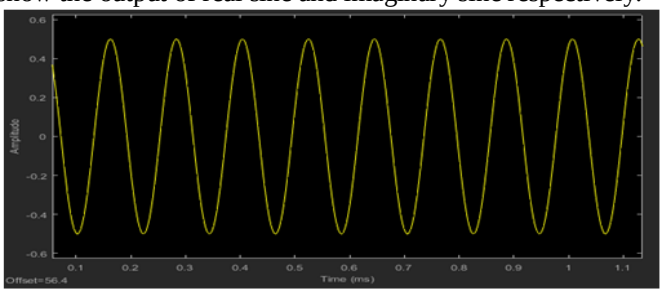

Fig 5:- Output of Real Sine

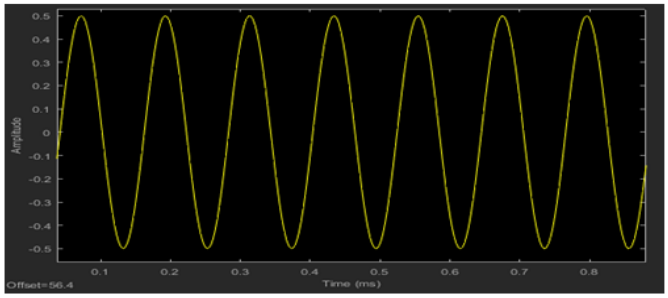

Fig 6:- Output of Imaginary Sine

Theoretical Calculations:
Sampling Frequency (Fs) = 64.5MHz
Input signal= 64.4MHz
Decimator factor of CIC (M1) = 64
Decimator factor of CFIR (M2) = 2
Decimator factor of CPFIR (M3) = 2

- NCO= Fs *(5/24) (1)
  NCO= 64.5e6*(5/24)

NCO= 13.43MHz

- Decimator output = $\frac{NCO}{(M1*M2*M3)}$ (2)

Decimated Output = $\frac{13.43}{64*2*2}$

Decimated output= 0.053MHz

The output of NCO and decimator is calculated theoretically as shown in equation 1 and equation 2. Output generated from the Matlab code is approximately equal to the theoretical calculations with NCO output of 13.33MHz and decimated output of 0.1MHz. Spectrum analyser object is created and configured to plot the power spectrum of NCO output as well as decimated output. Fig. 7 shows the output for NCO. Difference between the sampled frequency and input frequency provides the decimated output frequency. Fig. 8 shows the decimated output.

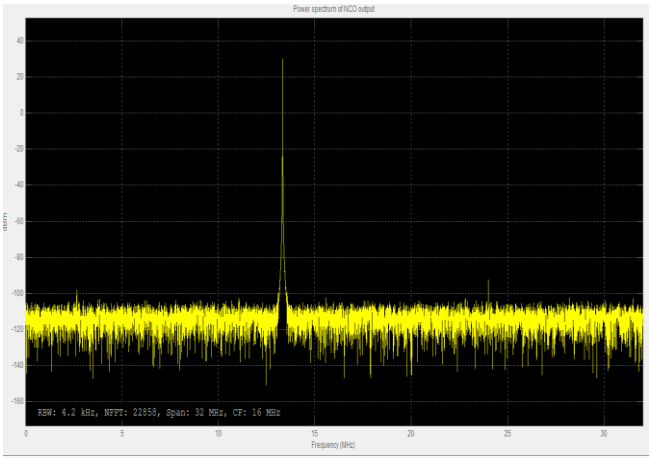

Fig 7:- Output of NCO

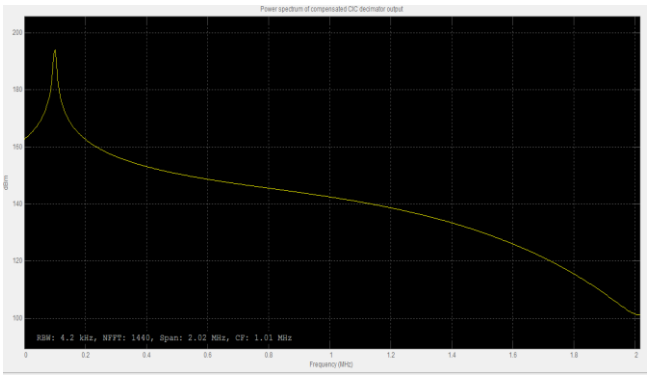

Fig 8:- Decimated Output

B. Output of DDC with Half band Filters

MATLAB code for DDC is written by replacing low pass filters with half band filters. The time scope and system analyser object enable to analyse the various stages of DDC. Fig. 9 and Fig. 10 show output of Real Sine and Imaginary Sine respectively. Rate converters are used to obtain sine waves. FIR rate converter is created to resample the final output. The difference between real sine and imaginary sine is that imaginary sine generated has a phase shift of 90 degree. Along with the sine output, NCO output and decimated output is generated. Spectrum analysers object is created and configured to plot the power spectrum of NCO output as well as decimated output.

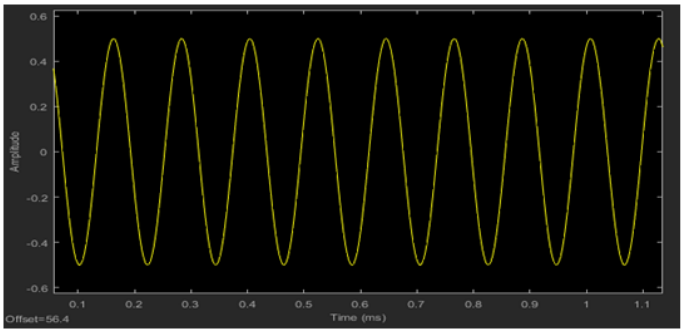

Fig 9:- Output of Real Sine

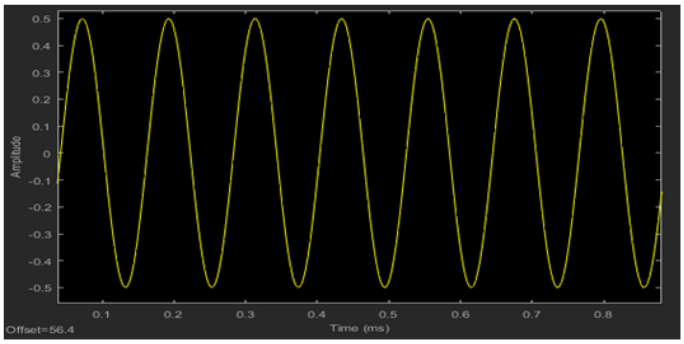

Fig 10:- Output of Imaginary Sine

Theoretical Calculations:
Sampling Frequency (Fs) = 64.1MHz
Input signal= 64MHz

Decimator factor of HB1 (M1) = 2
Decimator factor of HB2 (M2) = 2
Decimator factor of PFIR (M3) =32

- NCO= Fs *(5/24) (3)
  NCO= 64.5e6*(5/24)

NCO= 13.4MHz

- Decimator output = $\frac{NCO}{(M1*M2*M3)}$ (4)

Decimated Output = $\frac{13.43}{32*2*2}$

Decimated output= 0.1MHz

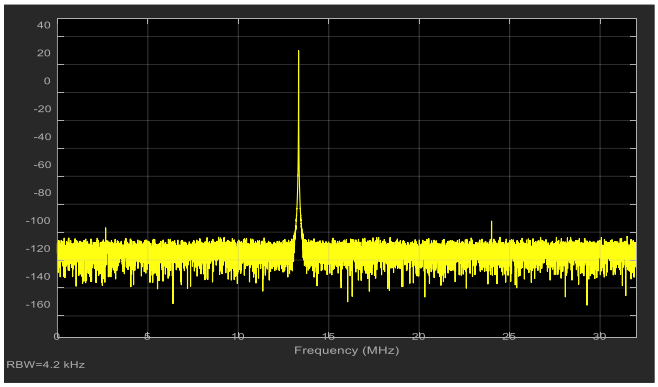

Fig 11:- Output of NCO

Fig. 11 shows Output of NCO and Fig. 12 shows the Decimated Output. Matlab code is provided with an input frequency of 64.1MHz and sampled frequency (Fs) of 64MHz. The difference in the frequency of both the signals forms the decimated output. The output for NCO is obtained by creating a NCO system object to mix and down convert the GSM signal. Thus the decimated output obtained is 0.1MHz and NCO output is 13.33MHz which is approximately similar to the theoretical calculations as shown in equation 3 and equation 4.

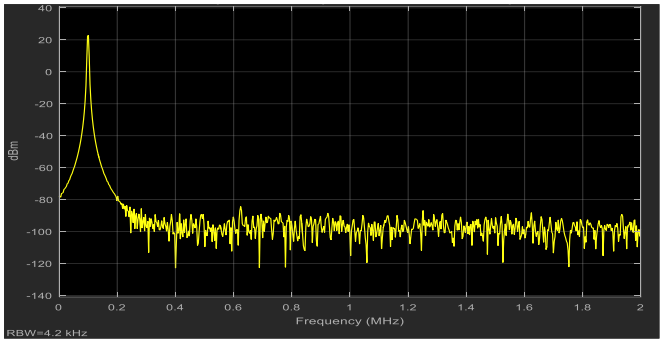

Fig 12:- Decimated Output

V. CONCLUSION

DDC is verified with set of filters such as CIC, CFIR and PFIR. One of the most common DDC filter implementation is the CIC filter. CIC filters eliminate the multiplication operations and use only delays and summation units as required in FIR filter. Storage of filter coefficients does not require any memory. The “passband droop” in its frequency response is the major disadvantage of using the CIC filters. This also shows the number of stages is too large. To overcome the magnitude droop compensating filter are used along with CIC filter, as magnitude response of compensating filter is inverse of the CIC filter. Use of CIC filter and FIR filters cascaded together may eliminate passband droop factor but will increase the resource consumption. In order to overcome these drawback half band filters replaces the cascaded filters. The multi-channel digital receiver therefore reduces the use of CIC stages and instead utilizes half band implementations. As half band filters consumes less resources as well as signal strength is increased after decimation.

VI. ACKNOWLEDGMENT

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