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Capacitor Voltage Stabilization in Neutral Point Clamped Multilevel Inverter

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Abstract:- Multilevel inverter are used in various applications in recent times for medium/low voltage and high power. The main reason behind use of multilevel inverter it has better total harmonic distortion (THD) and attain high values of voltage. Main issue in multilevel inverter diode clamped topologies is dc link capacitor voltage balancing. In this paper, method for dc link capacitor voltage balance for three level neutral point clamped inverter using level shifted multicarrier sinusoidal pulse width modulation is considered. Proposed method not only balances capacitor voltage but also reduces harmonics in load voltage and current. The performance of proposed topology is verified by simulation and experimental results.

Keywords:- *Bias value(B),Diode clamped inverter(DCI)/Neutral point clamped inverter (NCI),Multicarrier sinusoidal pulse width modulation(SPWM),Multilevel converter, Total harmonic distortion(THD).*

I. INTRODUCTION

Now –a-days high power conversion system demanded highly, but these system needs high output voltage and low harmonic distortion in output. Hence multilevel inverter is suitable and best candidate. Multilevel inverter has very high quality output voltage and current therefore it is receiving very high attention in high power application such as traction, industrial drives, etc. The diode clamped inverter (DCI), flying capacitor and cascaded H-Bridge topology of multilevel inverter are highly used topologies [1]. One of this topology diode clamped it is also called as neutral point clamped topology is proposed in this paper. However in diode clamped three level inverter voltage is divided in equal ratio across two capacitors. The main problem with three level inverter is fluctuation of neutral point voltage and it is because of positive/negative current flowing in/out of neutral point. The unbalance of neutral point potential is one of the severe problem in neutral point clamped inverter. The main reason for neutral point unbalance is non-uniform dc link capacitors and load type which we are used. Due to neutral point unbalance increase in output voltage harmonics and it may drift output voltage to unacceptable level and may damage switching devices, filter capacitors used to reduce harmonics. Various neutral point balancing techniques are proposed in literature [2]-[4]. Zero sequence voltage balance method has a drawback that it needs analysis of power factor of load current and it is difficult to implement under transient condition. The most popular space vector pulse width modulation (SVPWM) can be used but it is very complex and difficult to implement than proposed scheme of SPWM. In this paper level shifted multicarrier sinusoidal pulse width modulation technique is developed for neutral point clamped inverter. The proposed method requires measurement of capacitor voltage difference and load current which can be shown in simulation and experimental results in further sections.

A. Diode Clamped Inverter/Neutral Point Clamped Inverter

For an n level inverter (n-1) number of DC link capacitorsand same number of carrier waveforms required. The schematic for NPC three level inverter is as shown in Fig 1. Each arm can create the three voltage levels $V_{dc}/2$, 0, $-V_{dc}/2$ hence it is called as three level inverter. The diodes shown are called as clamping diodes and connected to the midpoint of the series capacitors, marked as '0' in Fig. 1. The diodes and capacitors are rated to block voltage $V_{dc}/(n-1)$. In NPC as a level of inverter is increases voltage steps becomes smaller and similar to a sinusoidal waveform and smoother. In the proposed paper, a three level neutral point clamped inverter is briefly discussed and controller is designed for capacitor voltage balancing with multicarrier Sinusoidal PWM scheme associated with phase shift of 120° in sine wave.

For an output voltage of $+V_{dc}/2$ in any phase arm, all the upper half Switches are turned ON i.e. Switches S_1, S_2 are ON and switches S_3, S_4 are OFF for phase-A. For an output voltage of $-V_{dc}/2$ in any phase arm,all lower half switches are ON i.e. Switches S_3, S_4 are ON and switches S_1,S_2 are OFF state and for an output voltage is 0 in any phase arm, middle two switches are ON i.e. Switches S_3, S_4 are ON and switches S_1, S_2 are in OFF position.

Table 1 shows the different voltage levels and their corresponding switching states for phase A.From the table I it is observed that the switches S_1, S_3 and S_2, S_4 are the complimentary switches i.e. when the switch S_1 is in ON state S_3 will be in OFF state and vice versa. In the same way S_2 and S_4 are complimentary switches. The level of the inverter can be verified with the help of pole voltages only, which is measured between any one phase and midpoint of the dc link capacitors.

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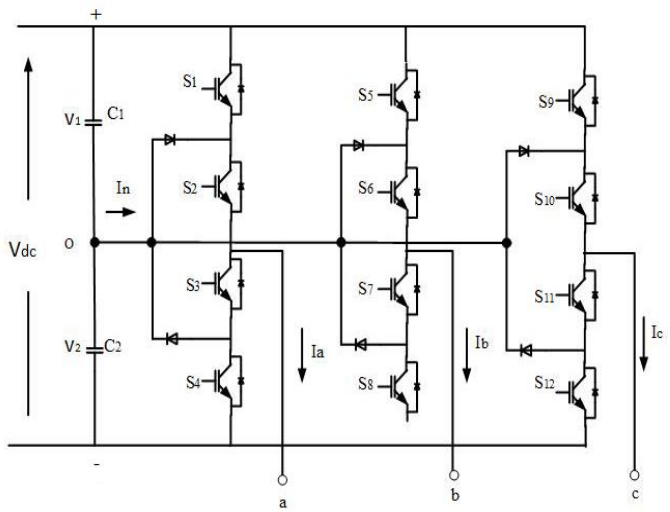

Fig 1:- Schematic of NPC three level inverter

Sr. No.	S_1	S_2	S_3	S_4	Output
1	ON	ON	OFF	OFF	$+V_{dc}/2$
2	OFF	ON	ON	OFF	0
3	OFF	OFF	ON	ON	$-V_{dc}/2$

Table 1. Switching States For Phase-A.

II. PROPOSED SPWM SCHEME FOR NEUTRAL POINT VOLTAGE BALANCING

Various modulation schemes are used to generate gating signals for switches operation such that applied DC voltage will gets converted into an AC voltage. Mostly used scheme to generate gating signal is SPWM because this scheme is very easy to implement as compared to other scheme such as space vector pulse width modulation (SVPWM), etc. It can also be extended to higher level converter topologies. In proposed SPWM topology high frequency carrier wave is compared with low frequency sinusoidal reference wave and used carrier waveforms are vertically shifted. There are three modes of PWM strategies with different phase relationship for level shifted multicarrier modulation i.e. In phase disposition, Phase opposition disposition, alternate opposite phase disposition In phase disposition; in which all the carrier wave forms are in phase. In proposed scheme SPWM scheme with In phase disposition is used.In the proposed scheme of SPWM, in phase disposition of carrier waves for NPC three level inverter are as shown in Fig. 2 and the corresponding switching pulses are as shown in Fig. 3.

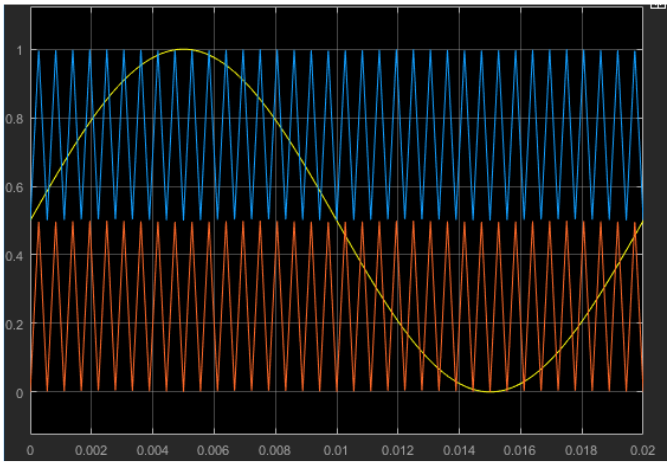

Fig 2:- SPWM scheme for NPC three level inverter.

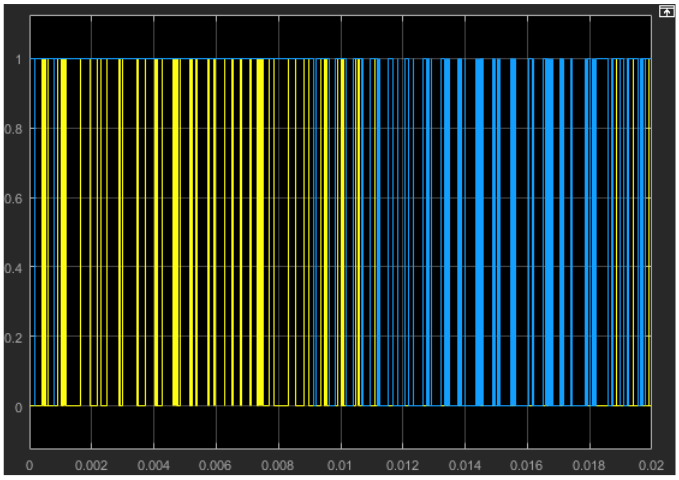

Fig 3:- Pulses generated in the SPWM In Phase Disposition scheme.

Switch S_1 is ON and S_3 is OFF during reference wave is greater than upper carrier wave. Switch S_2 is ON and S_4 is OFF when reference wave is greater than lower carrier wave. Sinusoidal reference wave is compared with level shifted carrier waves and gating signals for inverter switches are generated.Three phase sinusoidal reference wave is shifted by 120°. During steady state operation, load current (I_a+I_b +I_c) is always zero. But under transient condition Dc link capacitors are unbalance and voltage difference ($V_1 – V_2$) may or may not be zero. It may be positive or negative value and cause neutral point shift up and down regarding to reference value. This unbalance can cause damage of equipment's connected in circuit and could also damage the operating switches which may leads to malfunctioning of switches and inverter operation. To balance neutral point voltage it is necessary to shift reference wave in such a way that it will neutralize cause of unbalance. Appropriate bias value (B) is added to carrier wave to neutralize effect. The following flowchart shown in fig(4) shows proposed scheme for selection of bias (B).

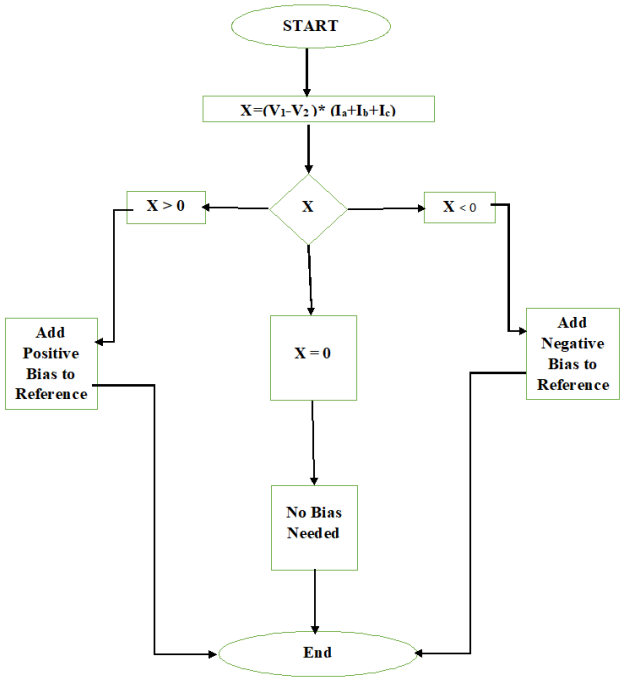

Fig 4:- Flow chart for switching of devices in proposed neutral-point voltage Topology.

Where X is a product of capacitor voltage difference ($V_1 – V_2$) and sum of load current ($I_a+I_b+I_c$). If capacitor voltage difference i.e.$V_1 – V_2$is positive/ negative and neutral current i.e. $I_a+I_b+I_c$is also positive/negative then we need to add negative bias to reference wave for neutralize effect of unbalance. Similarly, if capacitor voltage difference i.e.$V_1 – V_2$ is positive/ negative and neutral current i.e. $I_a + I_b + I_c$ is also negative/positive or vice-versa then we need to add positive bias to reference wave for neutralize effect of unbalance.If capacitor voltage difference i.e.$V_1 – V_2$ is zero and neutral current i.e. $I_a + I_b + I_c$ is also positive/negative and vice-versathen no bias needed to be added to reference wave.

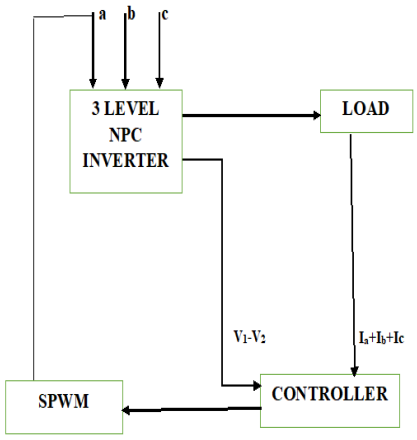

Fig 5:- Complete scheme of voltage balancing.

III. SIMULATION AND EXPERIMENTAL RESULTS

The feasibility of proposed converter is evaluated experimentally. Here control strategy developed for three level inverter and results are verified by using MATLAB SIMULINK software. The dc voltage is taken as 400V and two capacitor values are sets at 4900µF. Fig (6) and fig (7) shows unbalanced and balanced neutral point voltage. Form fig (6) and fig (7) it is cleared that time required for balancing i.e. to make neutral point voltage ($V_1 – V_2$) to zero is quite larger in unbalance method as compared to balance method it shows that our control strategy working properly.

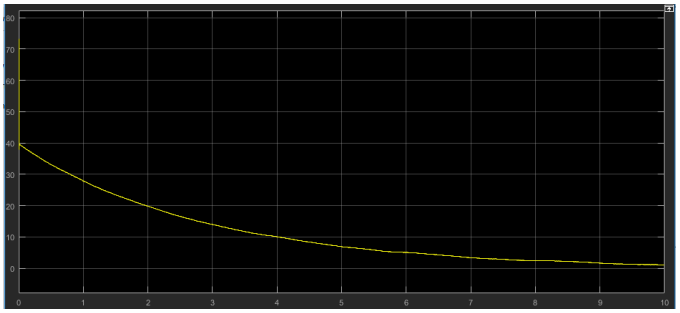

Fig 6:- Unbalanced Neutral Point Voltage.

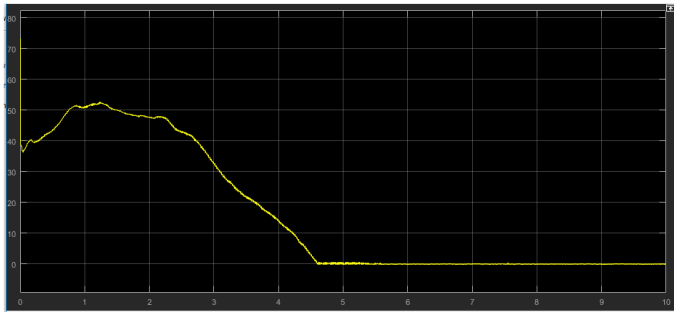

Fig 7:- Balanced Neutral Point Voltage.

Fig 8 and fig 9 shows line to line unbalanced and balanced voltage respectively.

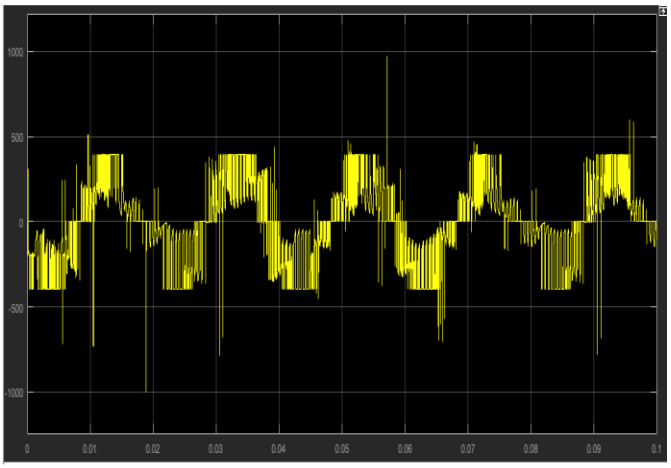

Fig 8:- Line to Line Unbalance

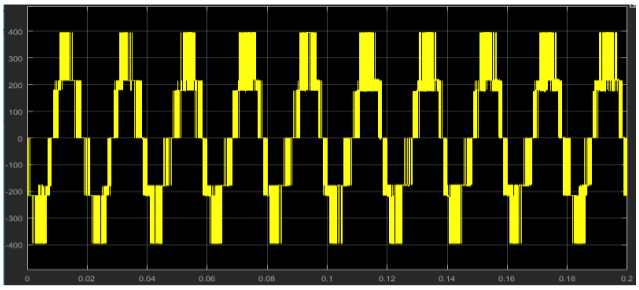

Fig 9:- Line to Line balanced voltage.

By comparing results from fig (8) and fig (9), it is cleared that Without balancing harmonics are quite high as compared to with balancing.

IV. CONCLUSION

The neutral point voltage balance scheme is developed for NPC three level inverter and analyzed. By the use of proposed balancing technique reduction in total harmonics distortion (THD) and along with it significant reduction in harmonics, minimization in loss and effective voltage balancing is achieved. Higher level NPC inverter would give more significant reduction in THD in output voltage and current.

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