Determination of Various Performance Parameters using CMOS and CNT via 4T Schmitt Trigger

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Abstract:- Schmitt trigger is used to augment noise protection of a circuit of broaden delay and power consumption. The main function of Schmitt trigger is used to decreasing noise issue in the circuit. In this current paper, the comparison of two techniques, CMOS and CNT based transistors of Schmitt trigger in 32nm technology is compared regarding various performance factors being power consumption, delay, hysteresis loss, leakage current etc. In this paper the Schmitt trigger is used in such a method that via making an adjustment in the voltage its premature is enhanced by the output as the time conversion and the consumption of the power is less thus decreasing the output delay. The complete circuit functioning of Schmitt Trigger is replicated and performed on the Spice tool for both CMOS and CNT transistors in 32nm technology. The results exhibit that CNT 4T Schmitt Trigger reduces the consumption of power, leakage as well as output delay thereby obtaining better efficiency and results over CMOS based circuit.

Keywords:- *4T Schmitt Trigger, CMOS, CNT, Power Consumption, Leakage, Delay, Hysteresis loss, SPICE Tool.*

I. INTRODUCTION

The digital signal cannot be defined directly by the digital circuit; there are several reasons behind it being the time of rise and fall, they also exhibit a little bit of noise sense because of the proceeding circuitry, so for maintaining all the critical conditions and signal, there is a need of a specified clean up device which is known as Schmitt trigger [3]. When level of input crosses the predetermined threshold level, then the output level is changed. This directly indicates that the output level is dependent over the input level. For solving mainly the problem of noise, the device named as Schmitt trigger is used in the circuit of analog and digital in the form of wave shaping device [4]. The main function of this drive is driving or converting load with fast switching the low loss and supply of power. This Schmitt trigger is basically used to decrease the noise sensitivity and enhance the control state i.e. on/off state [5]. Conversion of a slow differentiating analog signal voltage into the maximum possible binary states is the main working of Schmitt trigger. But, this conversion is dependent over the voltage; earn that whether this type of voltage is above or below the recommend threshold voltage. On comparing the conventional Schmitt trigger circuit (6T) with the inverter, it was determined that the former exhibited better noise sensitivity than the later. The reason behind it being that they are exhibited better transition threshold voltage [6]. Further, the threshold voltage of Schmitt trigger (6T) circuit is VH during the input signal from VDD to GND and the same i.e. the conventional Schmitt trigger threshold voltage is found to be VL when the input signal travels down from GND to VDD [7]. The comparison of the same with comparators is indicated using the DC transfer characteristics. In the comparators, they are able to exhibit only one switching threshold but on the contrary, Schmitt trigger exhibits various and different switching threshold value for both types of input signal edges being positive and negative both. This aforementioned property is known as hysteresis. The Schmitt trigger can be work as a comparator providing positive feedback in the circuit [9]. Therefore, to acquire these approaches, Schmitt trigger modifications in the structure are to be made and then this technology can be completely implemented at the level of circuit. The parameters of Schmitt trigger have been examined through spice tools in the circuit. Further, the feature of hysteresis, in Schmitt trigger, masks some of the unwanted transient pulses over the input. On based over the above, there was a requirement of the effective and efficient designing of the hardened memory elements which were based on Schmitt trigger. In this circuit when we increased the input capacity of the critical nodes, then the power consumption was also increased [11][12].

According to the property of hysteresis, Schmitt trigger is to remove noisy signal and gives reliable signals in the circuit. The aforementioned can be well-defined for those systems exhibiting high performance and low power. The former is the one in which when the input is rising and finally reaches the UTP voltage and the latter is the point at which the input which is falling finally reaches LTP voltage. And when the input lies amongst these two pints then its value is retained by output. The hysteresis thickness is too determined between gap of UTP and LTP voltage. If, the CMOS technology feature size is scaled down in nanometer scales, then the channel effects which are short will become more critical as the dimensions of the device and the supply voltage cannot be similarly scaled. There are several limitations also which further creates foundations regarding the scaling of the CMOS technology as demanding high intensity and the applications which are energy efficient. The limitations for the aforementioned are being power density and the current

leakages which are high and the issues which are related to reliability. To overcome these limitations, some of the successful innovations being MOS/SOI structures have already been suggested and implemented. But at the nanolevel or the nanoscale, for overcoming these serious issues, there is a requirement of alternative materials and nano devices. There are several emerging nano devices which are and can be used for resolving these serious issues being CNTFET, which is exactly similar to MOSFET; they both share similar structures and electrical features of the devices. In this new era of CNTFET, the existence of CMOS is still prevailing in the current technology. There are several designs which are being used amongst them is robust circuit design which is becoming popular and crucial in this nano-scale technology era, and is further counted as one amongst the most promising alternative technology being CNTFET [14][15][16].

There is a lot of ongoing research worldwide to accomplish the novel design of Schmitt triggers with improvised performances within the limited sizes. The main suffering with the conventional Schmitt triggers is the design challenges regarding the op- amp and the consumption of power is high. So, for reducing these two issues the Schmitt triggers were synthesized using the CMOS technology. The mostly used Schmitt trigger was constructed by Dokic in 1984. He designed the four transistors amongst or in between the grounds and the power rails. But, these designs failed their working for the low voltage applications. So, in 2001 change et.al constructed multilayer Schmitt trigger, involving large and huge variations of voltage amongst the two threshold voltages. Instead the main requirement of the structure was as before, the 4T between the power rails and the ground. Thus, if failed again working for low voltages applications. In 2005 Chen and Ming constructed a Schmitt trigger which was basically based on the design of Dokic working below 3.3V in enmity of high voltage gates bearing more stress. Further, now the research work started for the reduction of weights and size of transistor technology with efficient analog processing of the signal. These circuits were of the digital and the analog types. Digitally, the implementation and the designing of the circuits is easy as compared to the same in the analog domain, it is quite risky and challenging too. So, for the further formulation of the structures and task several technologies have been utilized being TTL, CMOS, Bi-CMOS etc. being one of the efficient technologies also, they exhibit some limitations and drawbacks regarding the ranges of the frequency, signal disturbances due to minor current, the tunneling effect, as the existing CMOS technology could not attain the satisfying results when specifically behavior was concerned. Therefore, these types of limitations and drawbacks were improved in CNTFET that can be accepted worldwide as an analog and digital signal circuit. This technology named as CNTFET exhibits the ideal and efficient response of circuits within a transistor with 32nm range. The better results can also be obtained via this technology keeping the ranger low than 32 nm also. This technology has illustrated excellent and efficient results and is functioning as a boon for the electronic industry regarding the performances at low consumption and reducing the leakage issues also within this 32nm ranges [17].

II. LITERATURE REVIEW

Mogaddham et.al stated in 2017 that the buffer of Schmitt trigger via carbon nanotube FET for the applications of low power consumption. According to them, the susceptibility of the transient faults or the soft errors was more possible in the nanoscale circuits as they had the charge already stored in their nodes which were sensitive. Therefore, they stated that it is really challenging to design low-cost designs of the circuits when it is concerned with nanoscale storage cells. It can be further described low power hardened latch design circuit using Schmitt trigger. They did not enhanced up sizing or enhancing the input capacitance instead they determined the hysteresis mechanism of proposed Schmitt trigger buffer. The simulations results can be determine Stanford CNTFET model in 16 nm technology. Their results dictated that their proposed technology lowered the power delay product by 90% and enhanced the robustness compared to the PVT variations with most effective and efficient CNTFET based counterparts. There proposed hardened latch tolerance was also considerable for multiple node upset, the results were confirmed by the simulations. There was 68% higher critical charge found for the proposed hardened latch, therefore enhancing the reliability and further decreasing the 16 of the smaller areas when compared to all its counterparts [1].

Saxena et.al in 2016 stated the designs of Schmitt trigger which was based over the sink logic. The authors presented the paper using 3 COMS and CNT transistors in 32nm technology. The comparative analyses were investigated. The circuit used by them was 6T. The tool used by them was H Spice and the technology used was 32 nm nodes. They investigated some common parameters for evaluation. They analyzed the circuits for various separate inputs being pulse, waveform, damped, inputs which were triangular and exponential. They calculated and investigated about the average power, propagation delay and the consumption of the power. They also analyzed the sensitivity of the temperature. Finally they evaluated the hysteresis curves of Schmitt trigger based over the sing logic with all inputs. The results displayed higher gains when compared to the inverters which were actively loaded [18].

Saxena et.al in 2015 stated that for acquiring the better consumption of power, magnitude, speed, reliability and hysteresis was attained by CMOS device. The main aim of the Schmitt trigger according to the authors was lowering the power dissipation and enhancing the compatibility with the supply of power accommodating with the low voltage, and the capable result was to decrease the power dissipation which was counted to the device. The authors have compared the presentation of 6T and 4T Schmitt trigger. The 6T is the conventional six transistors and the 4T is the four transistors. This is further performed in such a way that as its voltage is

adjusted, the premature is increased and the output is ended. Thus the delay of the output is reduced because of the less consumption of power and conversion of time. It can performed and reproduced the circuit using MATLAB tool in 180 nm and 90 nm technology exhibiting the results of delay reduction by 12.3% and power to reduce by 24% in 6T Schmitt trigger [8].

III. CMOS SCHMITT TRIGGER

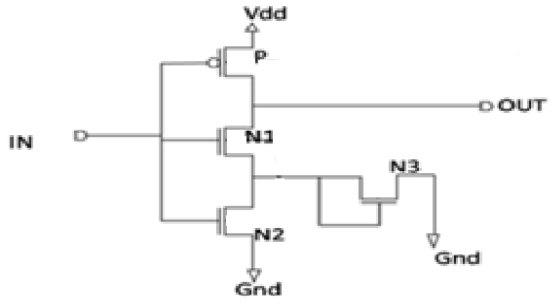

Fig 1:- CMOS 4T Schmitt trigger circuit

CMOS based Schmitt trigger as seen in figure 1. In this kind of Schmitt trigger contains of four CMOS based transistor to be used then it is called 4T Schmitt trigger. CMOS based Schmitt trigger contain of two part first one is PMOS and second one is NMOS. In this circuit PMOS device is connected to voltage (Vdd) and NMOS device to the ground (Gnd). Schmitt trigger can work as inverting comparator when we applied low input signal to get high output and vice-versa throughout the circuit. The schematic representation of 4T Schmitt trigger in figure 2.

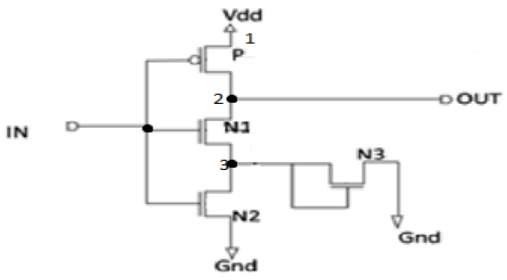

Fig 2:- Schematic design of 4T Schmitt trigger with net listing

IV. PROPOSED DESIGN

As given in figure 2 represent schematic design of 4T Schmitt trigger in CMOS, transistor P is connected between point (1) and point (2). Point 1 is supply voltage (Vdd) and Point 2 represents output of the circuit, transistor N1 is B/w point 2 and 3, N2 and N3 is between point 3 and ground (Gnd) of circuit. CNT based transistors technology to replace MOSFET into CNTFET. There is lot of drawbacks in CMOS based transistor to overcome this limitation through CNTFET in this paper. This type of transistor is cylindrical form whose length (L) and width (W) dimension is 32nm. Working principal of both MOSFET and CNTFET technology can work in 32 nm The Schematic design of CNT based 4T Schmitt trigger as shown in figure 3.

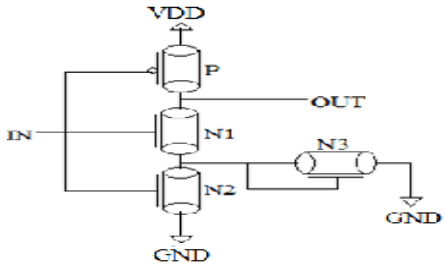

Fig 3:- CNT 4T Schmitt trigger circuit

Power supply voltage and threshold voltages both are condensed to the mount of CMOS technologies. When trimming in threshold voltage results in a mount of sub threshold to run current in the circuit. In fashionable physical science style, high performance integrated circuits (ICs), quite five hundredth of the whole on mode energy is dissipated because of the run power, with additional transistors integrated on-chip, run currents will speedily govern the whole power consumption of high performance ICs. Relation between leakage current and power is given by

$$Pleak = Ileak.Vdd \quad (1)$$

In this relation we have to determine leakage power as well as leakage current. When supply voltage is 1V then leakage power and leakage current are same but in opposite direction. Hysteresis is the characteristics of the Schmitt trigger to improve quality of given circuit, in which threshold voltage changed when the input is going to rise or fall of circuit [2]. Physical phenomenon breadth is given by ΔH; on the other way physical phenomenon is that the differentiate between the sign level at that a Schmitt trigger is standby mode and active mode (OFF and ON) state

$$\Delta H = VH - VL \quad (2)$$

Table 1 represents Comparative performance parameters of Schmitt Trigger with CMOS and CNT transistor in 32 nm.

Performance parameters	Schmitt Trigger CMOS based	Schmitt trigger CNT based
Technology	32 nm	32 nm
Supply voltage	1 V	1 V
Leakage power	149.82pW	107pW
Leakage current	149.82pA	107pA
Average power	49.07nW	32.67nW
Hysteresis loss	360mV	130mV
Propagation Delay	65.93ns	62.31ns

Table 1.

V. SIMULATION RESULTS AND DISCUSSIONS

The simulation waveform result of 4T Schmitt trigger using CMOS and CNTFET at 32nm technology with the help of spice tools as seen in figure 4 and figure 5.

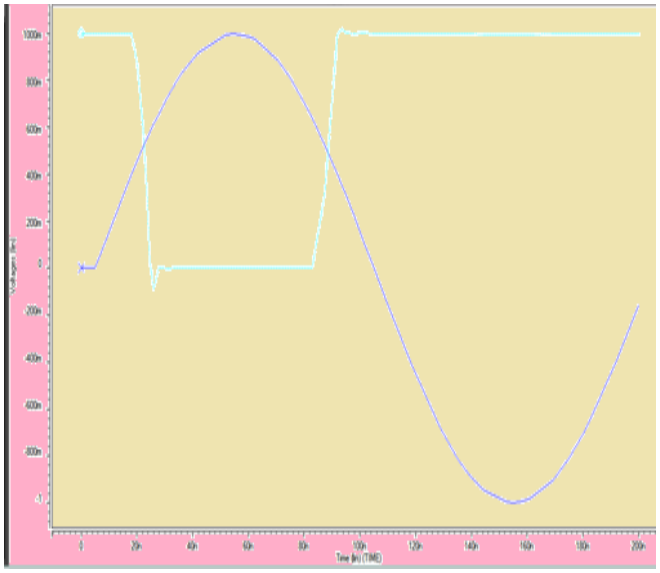

Fig 4:- 4T Schmitt trigger waveform in CMOS technology

Simulation waveform result of 4T Schmitt trigger using CNTFET technology noise immunity of signal and hysteresis loss to be reduced in comparison of CMOS technology as clearly seen in the waveform of CNTFET technologies in figure 5.

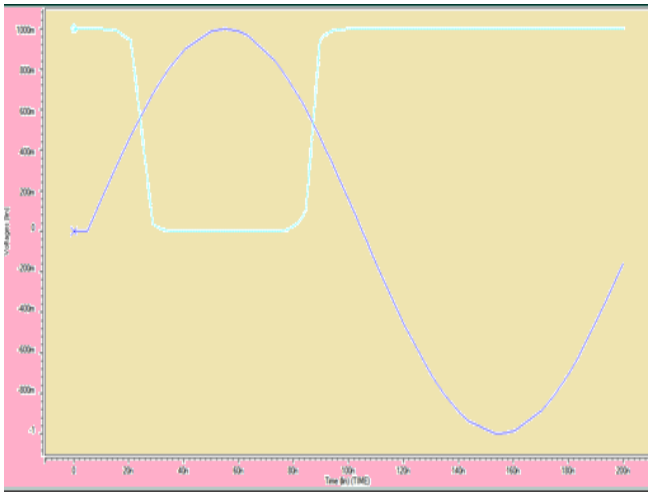

Fig 5:- 4T Schmitt trigger waveform in CNTFET technology

Efficiency is the fraction of output value to the input value of any circuit. High efficiency means that fewer power drains and also the input provide and fewer temperature buildups, granting little lighter power provides and structure enclosures. Potency is meanly measured as

$$Efficiency = \frac{Output}{Input} * 100 \quad (3)$$

Efficiency of 4T trigger Schmitt to be better in CNTFET in comparison of CMOS based technology because decrease in power consumption and hysteresis loss. The simulation result to be determined with the help SPICE device.

VI. CONCLUSION

In this paper to compare both CMOS and CNT transistors at 32nm technology in 4T Schmitt trigger design for performance parameters like the power consumption, delay, hysteresis, leakage current etc. The complete circuit work of 4T Schmitt trigger is performed on the SPICE Tool for both CMOS and CNT transistors. The results of CNT 4T Schmitt trigger reduces the power consumption is 28.51% and hysteresis loss is reduce to 63.88% over CMOS based technology. From the inferences made the idea of the research have been integrated through the CNT based transistors concept gives more efficiency than the CMOS based transistors technology because the planned Latch are designed victimization Schmitt trigger arrangement such the physical phenomenon property is used to induce higher performance against clanging input signals. Additionally the look is benefited with the distinctive properties of CNTFETs at an optimized nanometric vary of sixteen nm. Proposed circuits have easy structure with solely half-dozen transistors which ends up into less delay and less power consumption throughout the operation.

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