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Influence of Fiber Weave Effect on Controlled Impedance and Signal Skew

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Abstract:- Data rate need to be transmitted in PCB trace is increasing day by day. Because of that terms like skew, jitter is becoming critical and its margins are getting narrow. Also, tolerances of copper and dielectric in PCB fabrication is getting strictly precise. In the scenario, relevance of the non-linearity of dielectric is getting important, Fiber Weave Effect (FWE) which can cause a devastating effect on signal integrity (SI) in high-speed circuit boards. This paper is discussing the analysis of FWE on design consideration of the modern high-speed digital board.

***Keywords*:-** *Skew, Jitter, Fiber Weave Effect, Signal Integrity.*

I. INTRODUCTION

Dielectric Material in a printed circuit board is made of majorly two constituents, Fiber glass and resin. Fiber glass is long and slender and used as clusters. It reinforces the dielectric material. For better structural integrity fibers are woven fashion. Ie. Fibers are interlaced by horizontal and vertical fibers. Based on the number of yarns per unit area and pitch of yarn, strength of dielectric will be changed. Based on this parameters fiber weaving is categorized into different cloth styles. Resin is filled to the woven fibers to hold it together and forms the bulk of material. Resin can be made of different materials like, epoxy, acrylic and so on. After the fill of resin, the substrate undergoes heat press under controlled temperature and pressure forms solid dielectric with desired thickness.

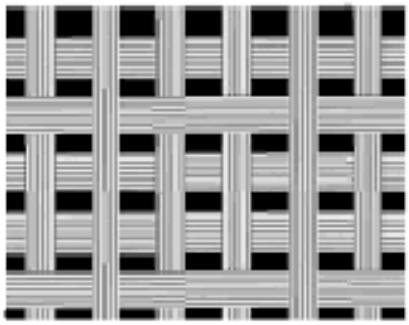

Fig 1:- Construction of dielectric with woven glass fibers.

Due to the woven nature of fiber glass and impregnated resin, there is unavoidable existence of void of glass fiber in dielectric. This voids are completely filled with resin only and without fiber. The dimension of void will be vary depending on cloth style and fabrication process. Since the fiber glass and resin are entirely different substances mostly, their dielectric constant (Dk) will be different. Here starts the problem of FWE. This introduces different dielectric constant for different points on PCB. Which in turn causes non ideal behaviour to the signals propagation. These effects are explained in detail later part of paper.

Because of the demand for compact board area and better Eye diagram, conventional parallel interfaces are replacing by high speed serial differential pair interfaces. Differential pairs are superior in improving the signal integrity, provided both lines have signals path physically same. Because of that, propagation delay offered by physical media will be same for positive and negative lines, and both signals arrived at receiver with same phase and efficient signals recovery. By good PCB layout practice, a designer can ensure the identical physical path for differential pairs by maintaining equal trace width, trace length and continuous reference plane. But Fiber Weave Effect can deprecate the these good results. FWE can introduce different signal skew to differential lines, due to variation of Dk in the individual path. The EIA JEDEC Standard JESD65B defines skew as “The magnitude of the time difference between two events that ideally would occur simultaneously” [1].

Providing controlled impedance of PCB traces is now a common practice. It is crucial in matching impedance of source and load and hence avoid reflection of signals. Due to FWE, variation of impedance arises and signal integrity reduces.

II. EFFECTS

Fabrication Facilities will be prepare PCB stack up information based on the impedance, number of layers, strength of PCB and so on. One of the major consideration for the required calculations are dielectric constant. From Fig 2, it is clear that Dk will be denoted as a constant value. But this assumption will be can be invalid when FWE has considerable effect in PCB. Due the void created by woven glass fibers creating variation in Dk (ΔDk), a two dimensional profile of ΔDk on the PCB surface can be formed. Signal trace going over the dielectric with ΔDk profile, will face following issues.

Objects		Types >>		Thickness	Physical >>		Signal Integrity >>	
#	Name	Layer	Layer Function	Value mil	Layer ID	Material	Conducti mho/cm	Dielectric Constant
*	*	*	*	*	*	*	*	*
		Surface						1
1	TOP	Conductor	Conductor	1.4	1	Copper	595900	4.5
		Dielectric	Dielectric	6.88		Fr-4	0	4.5
2	L2_GND	Plane	Plane	0.6	2	Copper	595900	4.5
		Dielectric	Dielectric	44.88		Fr-4	0	4.5
3	L3_PWR	Plane	Plane	0.6	3	Copper	595900	4.5
		Dielectric	Dielectric	6.88		Fr-4	0	4.5
4	BOTTOM	Conductor	Conductor	1.4	4	Copper	595900	4.5
		Surface						1

Fig 2:- PCB Stackup showing Dk value of each layers..

It is known that the average Dk of the substrate material changes as a function of the volumetric contents of the glass fibers and epoxy resin[4].

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A. Signal Skew

Consider a transmitter of a differential pair with line data_p & data_n. It is transmitting a pulse train of frequency 1Ghz, through a 10 inch copper trace to receiver circuit, Provided that, identical electrical path for both lines. Assume the Dielectric constant to be, Dk. Then propagation velocity (Vp) of the signal on two signals;

$$\text{Velocity of data\_p, Vp1} = \frac{c}{\sqrt{Dk}} \quad (1a)$$

$$\text{Velocity of data\_n, Vp2} = \frac{c}{\sqrt{Dk}} \quad (1b)$$

Where c is the velocity of light.

But due to influence of FWE, eq (1a) & (1b) is not completely valid, because the dielectric constant seen by data_p and data_n are different. Say that to be, Dk1 and Dk2 respectively. Which results,

$$\text{Velocity of data\_p, Vp1} = \frac{c}{\sqrt{Dk1}} \quad (2a)$$

$$\text{Velocity of data\_n, Vp2} = \frac{c}{\sqrt{Dk2}} \quad (2b)$$

In general the time required to travel signal from transmitter to receiver is time of arrival (TOA) [2].

$$\text{TOA} = \frac{l}{Vp} \quad (3)$$

Where the l is the total length of copper trace.

As discussed above, effect of FWE will result in different propagation velocity for data_p and data_n, causes the signals reach receiver at different times, fig x. As operating data rate of signals in the order of GHz, even small change in phase among differential pairs will create loss of information at receiver.

Ie. Change on time of arrival, ΔTOA,

$$\Delta\text{TOA} = |\text{TOA1} - \text{TOA2}| \quad (4)$$

Where TOA1 and TOA2 are time of arrival of data_p and data_n lines.

ΔTOA is the factor which signal integrity determined. Slight change in its value will be reflect in eye diagram. If ΔTOA too large eye closure happens.

Hence FWE can result in effects in skew and thus signal integrity, even geometrical identity is present in differential pair.

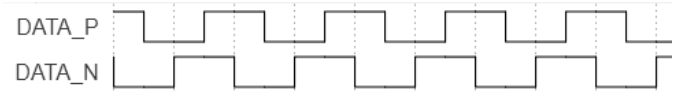

Fig 3:- Differential pair with considerable amount of skew.

B. Controlled Impedance

A critical task in high speed design is to transmit a signal from sender to receiver over lossy channel without compromising predefined eye mask. Major challenges in are ISI, reflection, radiation and jitter. Controlled impedance is the measure adopted in order to nullify reflection occur in a PCB trace by the concept of impedance matching. By revisiting traditional maximum power transfer theorem, to avoid reflection from load to source the impedance of load and channel are to be matched. There are standard impedance value we have to follow for certain interfaces like USB. In other cases either designer have to calculate or will provided by IC manufacturer. The integrity of transmitted signal through the interconnect at the receiver is affected by the impedance discontinuities and by the losses of the dielectric and conductive materials [3].

Value of controlled impedance is a function of thickness and width of PCB trace and Height and Dk of dielectric material.

$$\text{Zo} = \frac{87}{\sqrt{Er + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right) \quad (5)$$

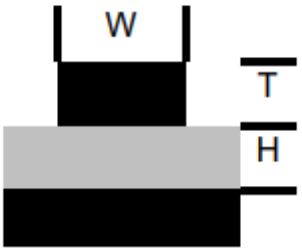

Fig 4:- Required measurements from PCB for Zo calculation.

Where Zo is controlled impedance of a microstrip, Er is the permittivity, and Er is product of Dk and vacuum permittivity. From eq (5) it is clear that controlled impedance is depend upon Dk of material. So while taking FWE into account, variation in Zo is obvious.

Practically, Dk is frequency depended quantity, which become important when board need to operate in wide range of frequencies. But the scope of this paper is not discussing this scenario.

III. ANALYSIS

Elimination of FWE can be done in two ways. First one is to make an alteration in the fabrication process of the dielectric material. Such as arrangement of glass fibers not in vertical or horizontal, but in a slight angle. This can help to minimize the probability of FWE for traces comes in 90° vertical or horizontal traces. The second method is in PCB layout level. While routing makes a zig-zag pattern which results in lesser FWE. These methods have lots of practical issues such as board area limitation, cost of material.

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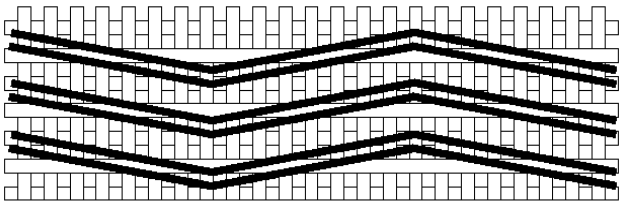

Fig 5:- zig-zag routing approach to minimize FWE.

Limiting the circuit specification, such as trace length, Frequency of operation is another method to minimize FWE. Still, this approach is challenging in most cases. Here, analysis of some parameters, which affected by FWE is going to be discussed.

A. Datarate

The maximum data rate supported by a PCB with known ΔDk can be computed with following inputs.

- Maximum differential pair length, L.
- Allowable signals skew, S (% of bit period).
- Change in Dk, ΔDk.

If D_{max} is the maximum feasible data rate without affecting SI by FWE can be equated as,

$$D_{max} = S\frac{c}{L\,\Delta Dk} \qquad (6)$$

B. Length of trace

Maximum signal trace length used to route a differential pair on PCB with FWE is given by,

$$L = c\frac{\Delta TOA}{\Delta Dk} \qquad (7)$$

Where L is the trace length and c velocity of light. From the equation, it is confirmed that Greater the FWE (ΔDk), less trace length is only possible. Time of arrival and skew are inter related. Both are relative among the two lines in the differential pair.

Analysis on FWE is never being straight forward. Due to inconsistency in specification and availability issue of accurate data is making the study challenging. Also mathematical modelling and analysis of FWE is time consuming process. Speedy method is to analysis based on broad margins of specifications. This will reproduce approximate results.

IV. CONCLUSIONS

Fiber Weave effect (FWE) is a fabrication level anomaly, which practically unavoidable. It has unfavourable effect on different design specifications like, skew, controlled impedance etc. Major remedy to use advanced material like rogers, megaron series. If design need to be cheap, take proper layout guideline which minimize the effect of FWE.

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